TOKYO ELECTRON

Tokyo Electron IR Day

February 26, 2025

Forward Looking Statements

- Disclaimer regarding forward-looking statements
  Forward-looking statements with respect to TEL's business plan, prospects and other such information are based on information available at the time of publication. Actual performance and results may differ significantly from the business plan described here due to changes in various external and internal factors, including political and economic situation, semiconductor market conditions, intensification of sales competition, safety and product quality management, intellectual property-related matters and impacts from COVID-19.
- Processing of numbers
  For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.
- Foreign exchange risk
  In principle, export sales of Tokyo Electron's products is denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of exchange rate fluctuations on profits is negligible, unless extreme fluctuations occur.

Agenda

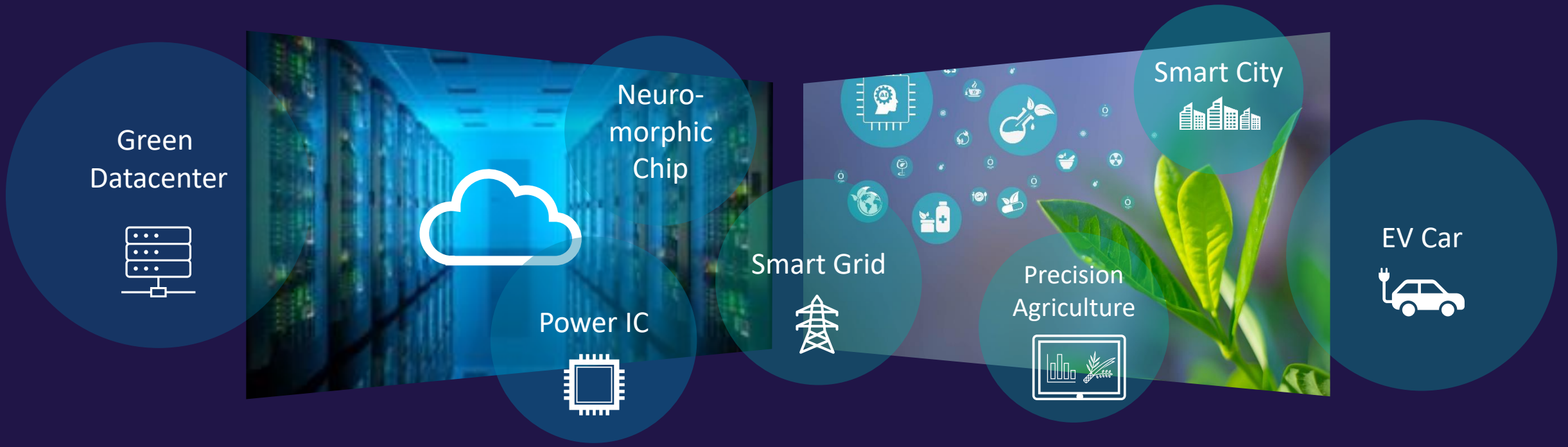
1. **Opening** **3:30pm - 3:35pm**
2. **Presentation** **3:35pm - 5:05pm**
   - Market Outlook for Semiconductors and TEL's Growth Strategy — Toshiki Kawai
   - Elevating Financial Position and Points for Future Growth — Hiroshi Kawamoto
   - Opportunities in Frontend Process Business and Activities in Digital x Green — Jack Ishida
   - Activities in Coater/Developer and Cleaning System — Yasuhiro Washio
   - Latest Technological Challenges and Activities in Etch — Tetsuya Nishiara
   - Business Strategy in Thin Film Deposition — Shigeki Nakatani
   - Diverse Systems and Solutions — Kan Ishida
   - Technology Trends and Business Opportunities in Assembly Processes — Keiichi Akiyama
   - Product Strategy in Assembly Processes — Yohei Sato

   <Short Break>
3. **Q&A** **5:15pm - 6:00pm**

Market Outlook for Semiconductors and TEL's Growth Strategy

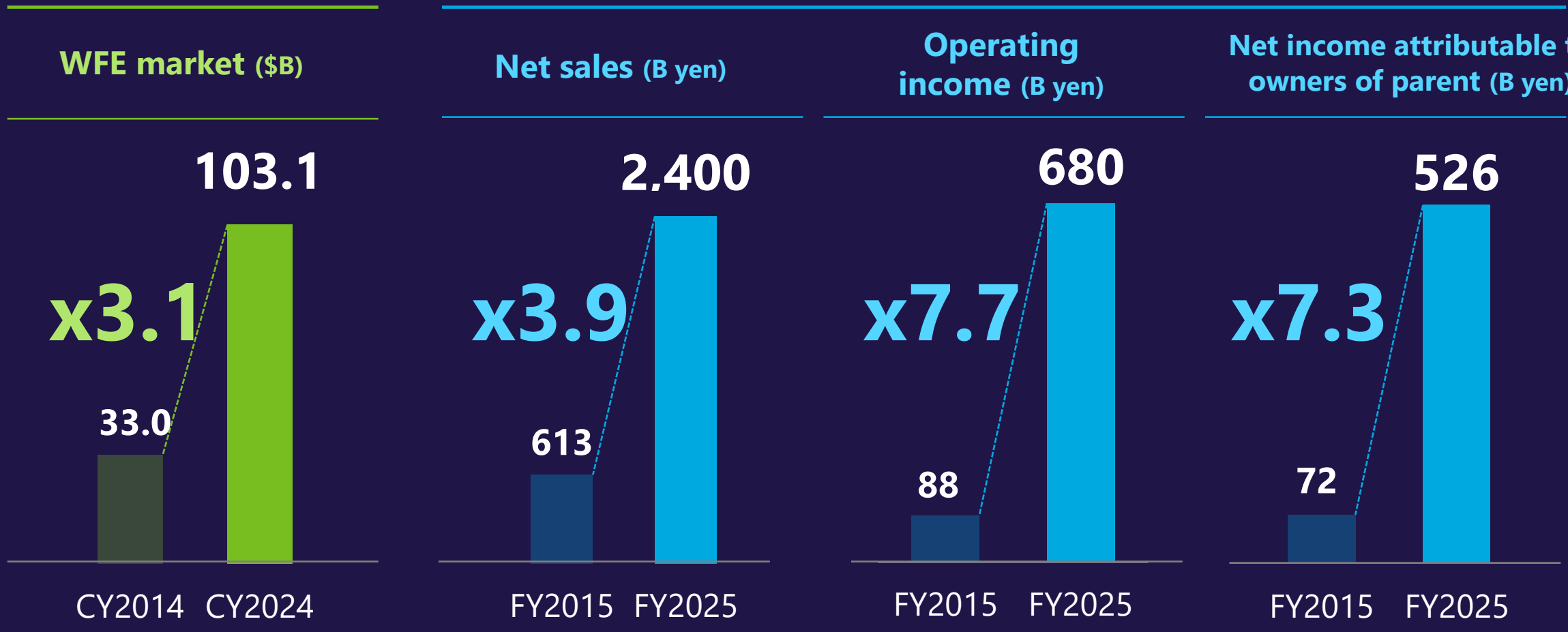
Tony Kawai
President & CEO
Tokyo Electron Limited

Digital & Green



"Green by Digital" & "Green of Digital"

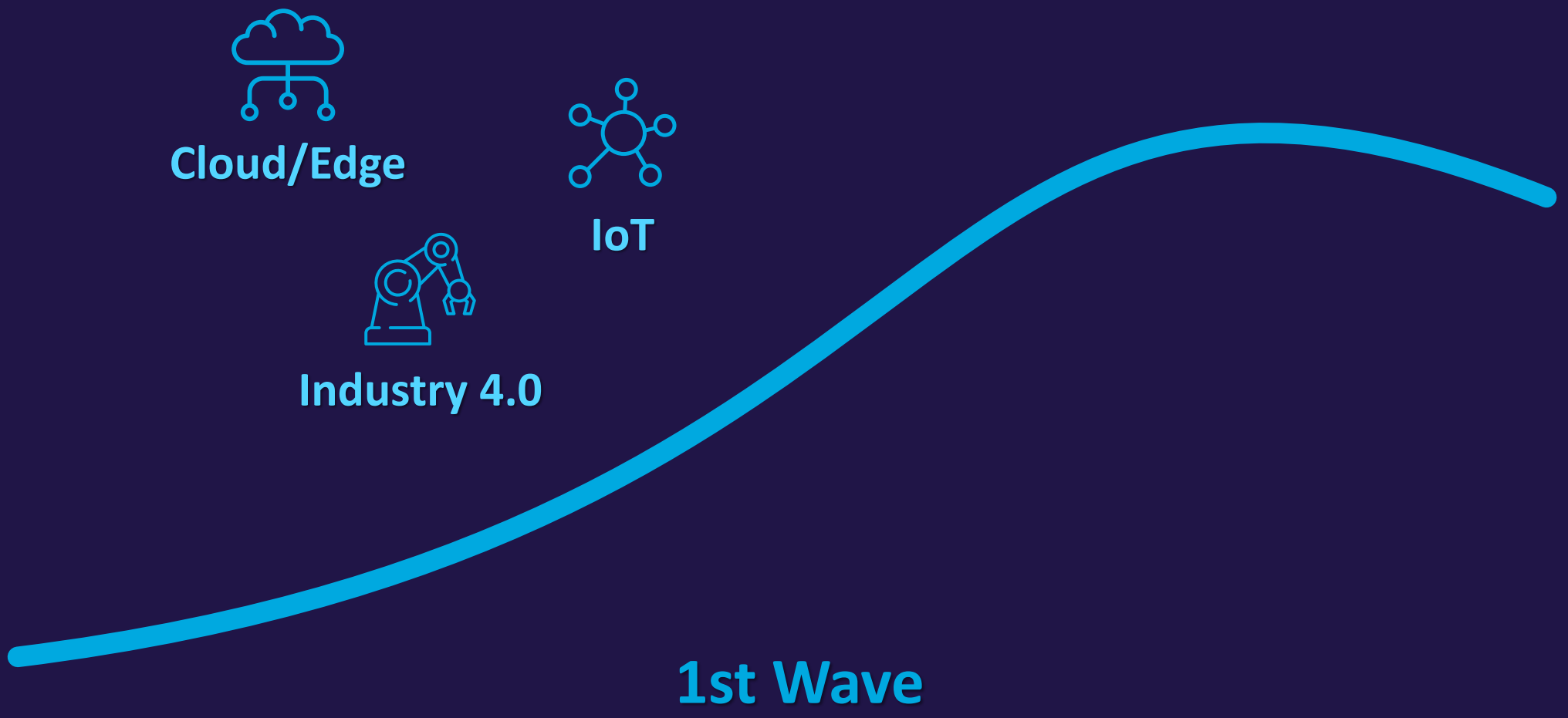
Comparison of FY2015 vs FY2025 Forecast



Expected to significantly outperform market growth

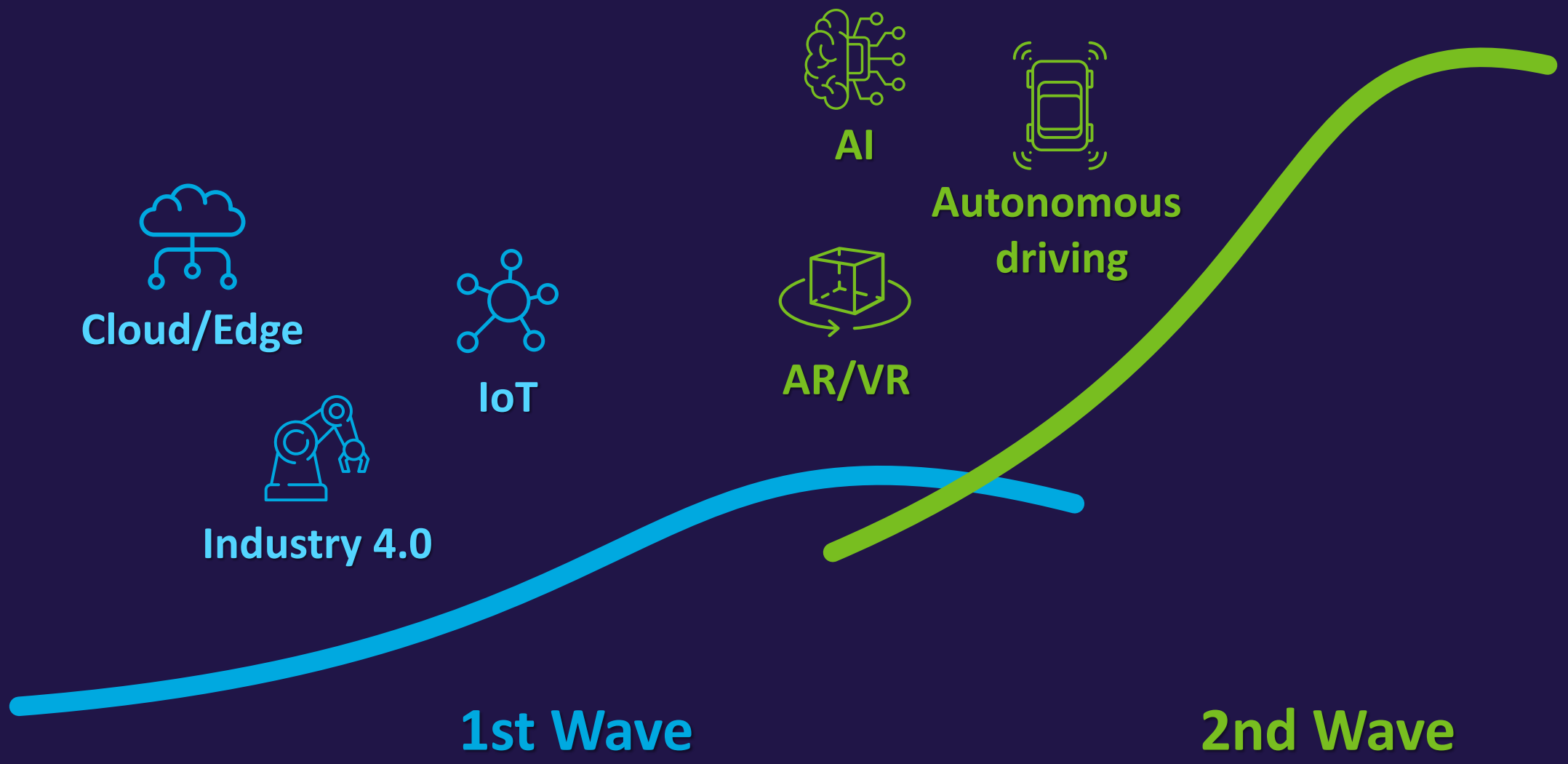
Source : TechInsights Manufacturing Analysis Inc. (VLSI)

Semiconductor Business Outlook



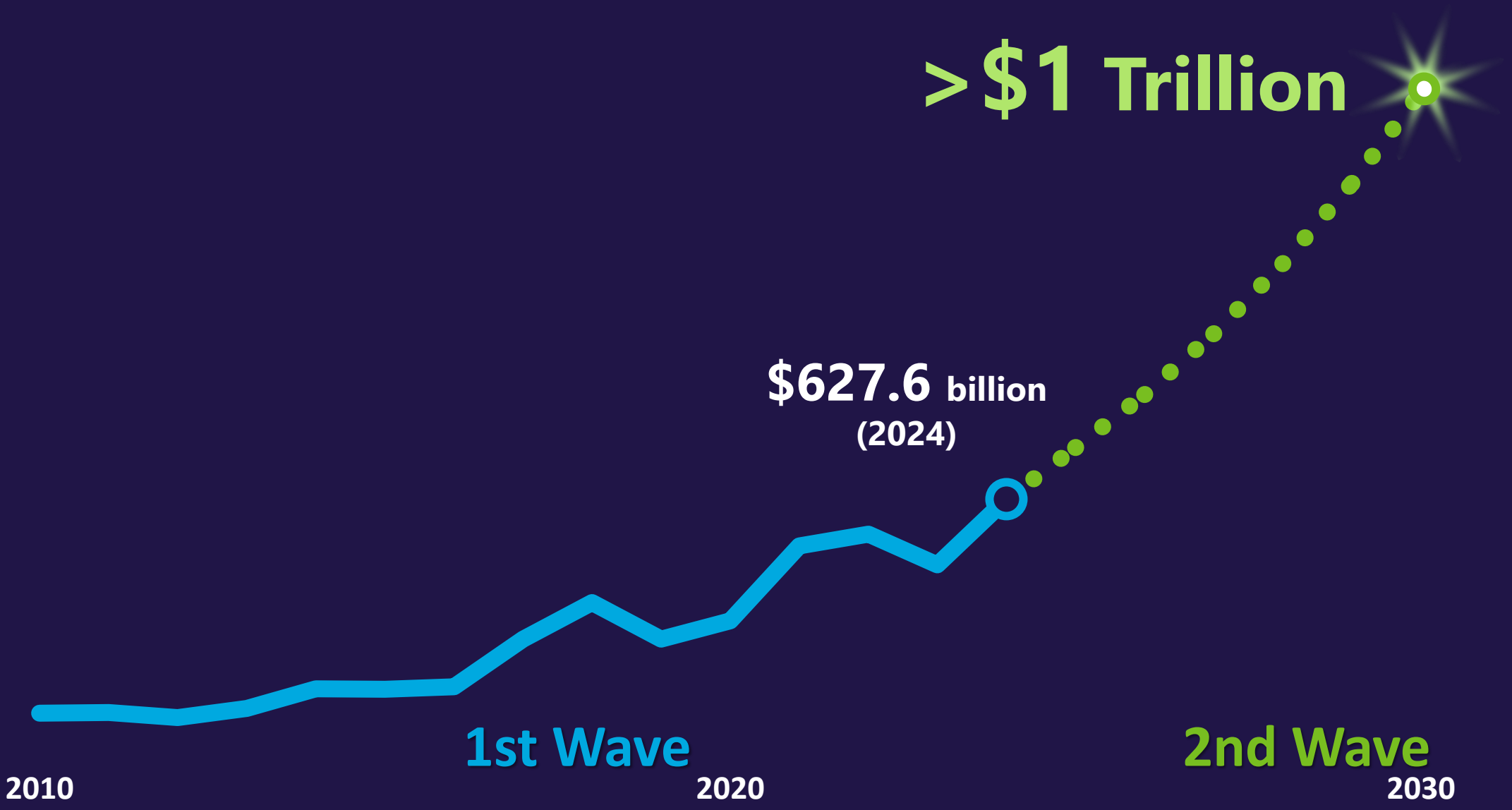
Source: SEMI 2024

Semiconductor Business Outlook



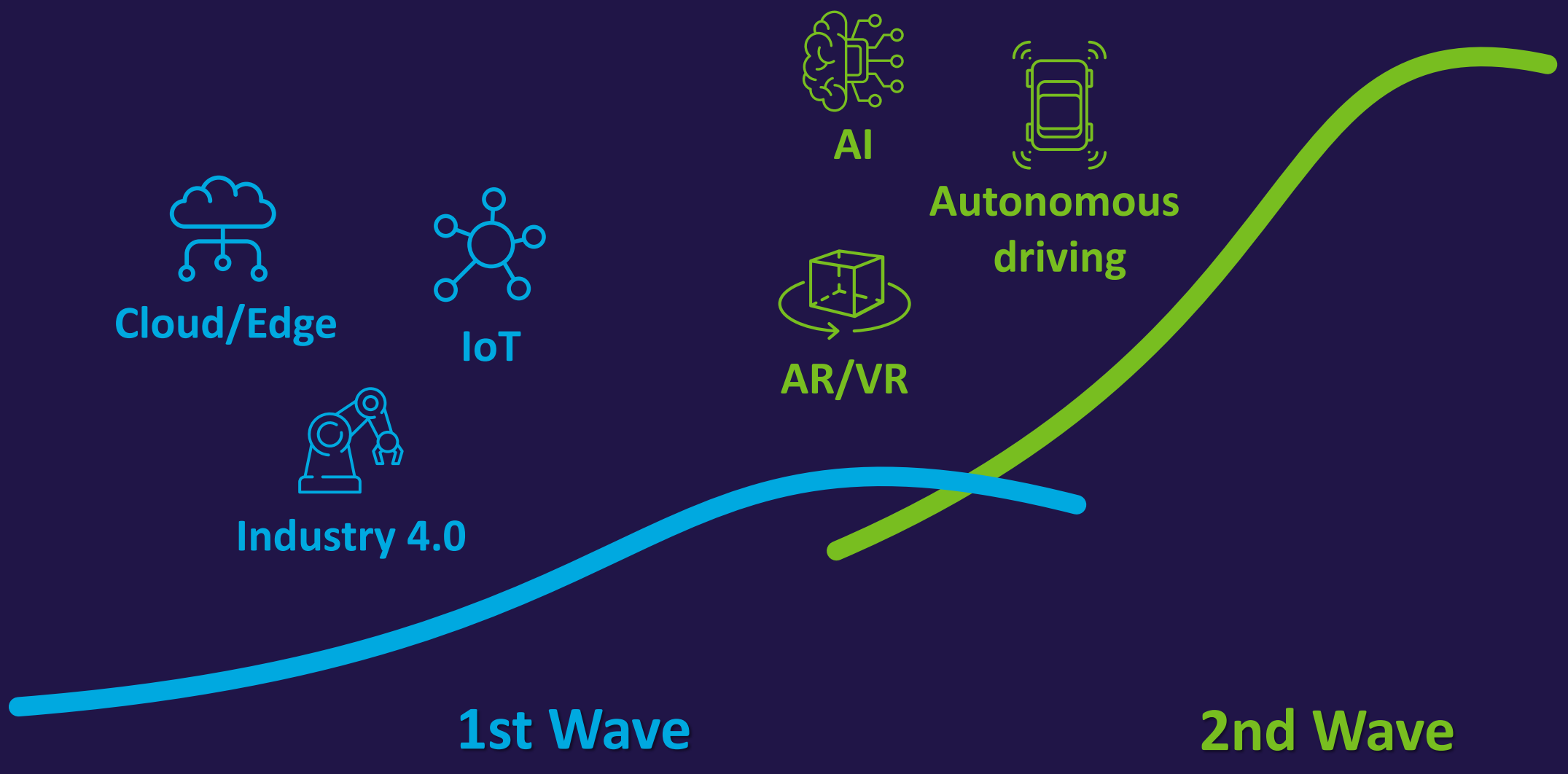
Source: SEMI 2024

Semiconductor Business Outlook



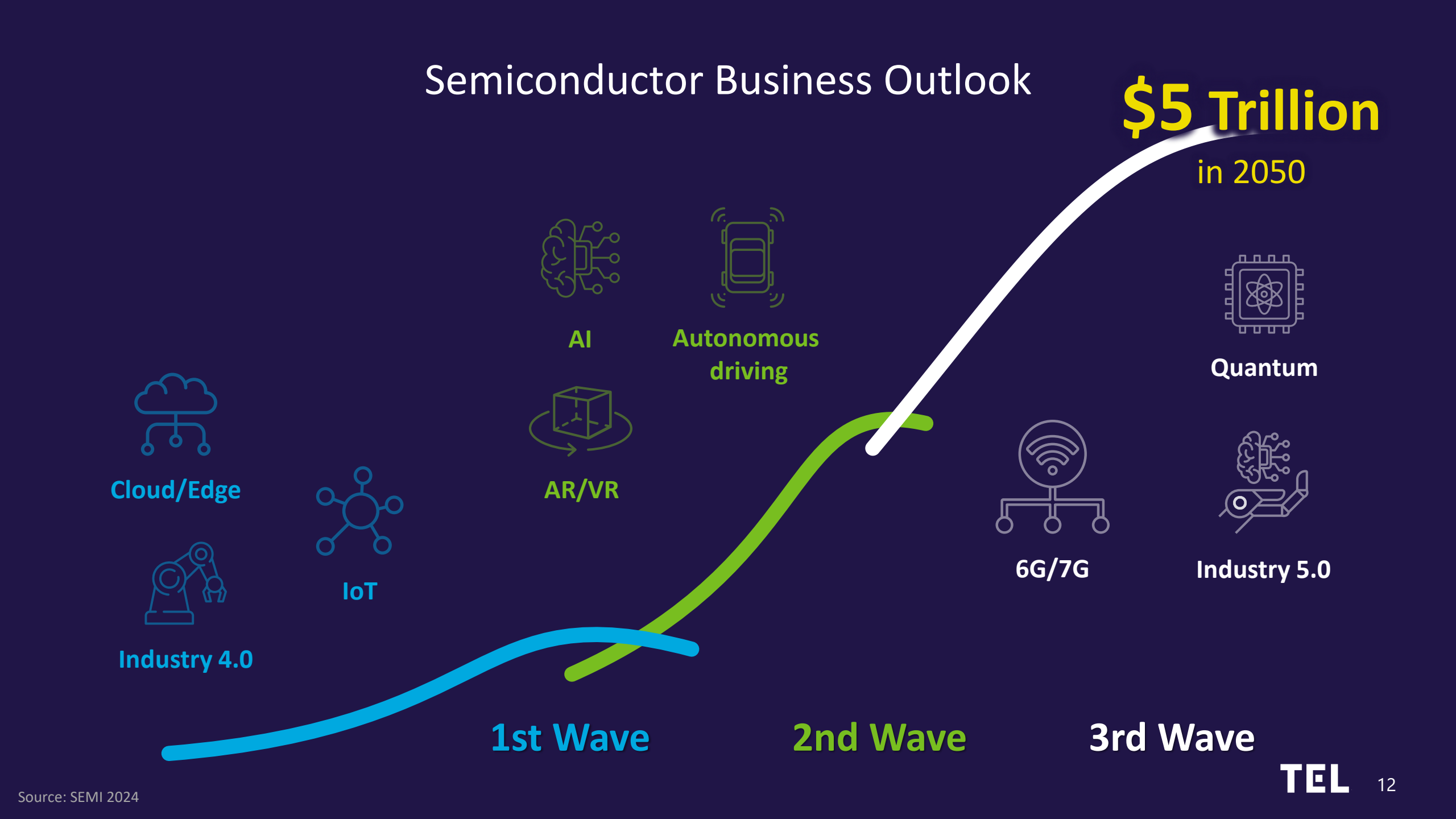
Source:1990-2024 (WSTS)／2025-2030 (IBS, January 2025)

Semiconductor Business Outlook



Source: SEMI 2024

Semiconductor Business Outlook



Source: SEMI 2024

TEL's Vision

A company
filled with dreams and vitality
that contributes to
technological innovation
in semiconductors.

Innovation

Contributing to technological innovation in semiconductors

Profitability

Creation of social and economic value

People

People are at the center of everything

TEL is Technology Enabling Life

CSV

Creating Shared Value

Creation of social and economic value

TSV

TEL's Shared Value

Achieving digitalization and global sustainability

"Technological innovation in semiconductors is essential"

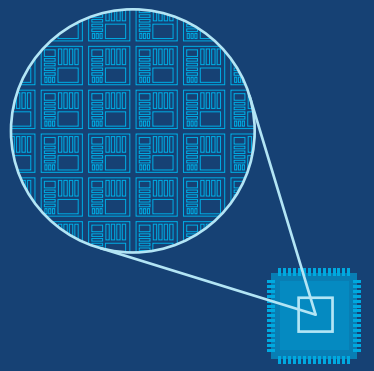
Financial Targets (by FY2027)

Net sales	**≧ 3 Trillion Yen**
OP margin	**≧ 35%**
ROE	**≧ 30%**

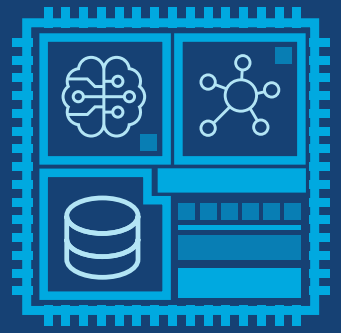
Green Future Through Semiconductor Evolution

Digital & Green

- Higher Speed
- Larger Capacity
- Superior Reliability
- Lower Power Consumption



Physical Scaling



Heterogeneous Integration

Physical Scaling x Heterogeneous Integration

Frontend

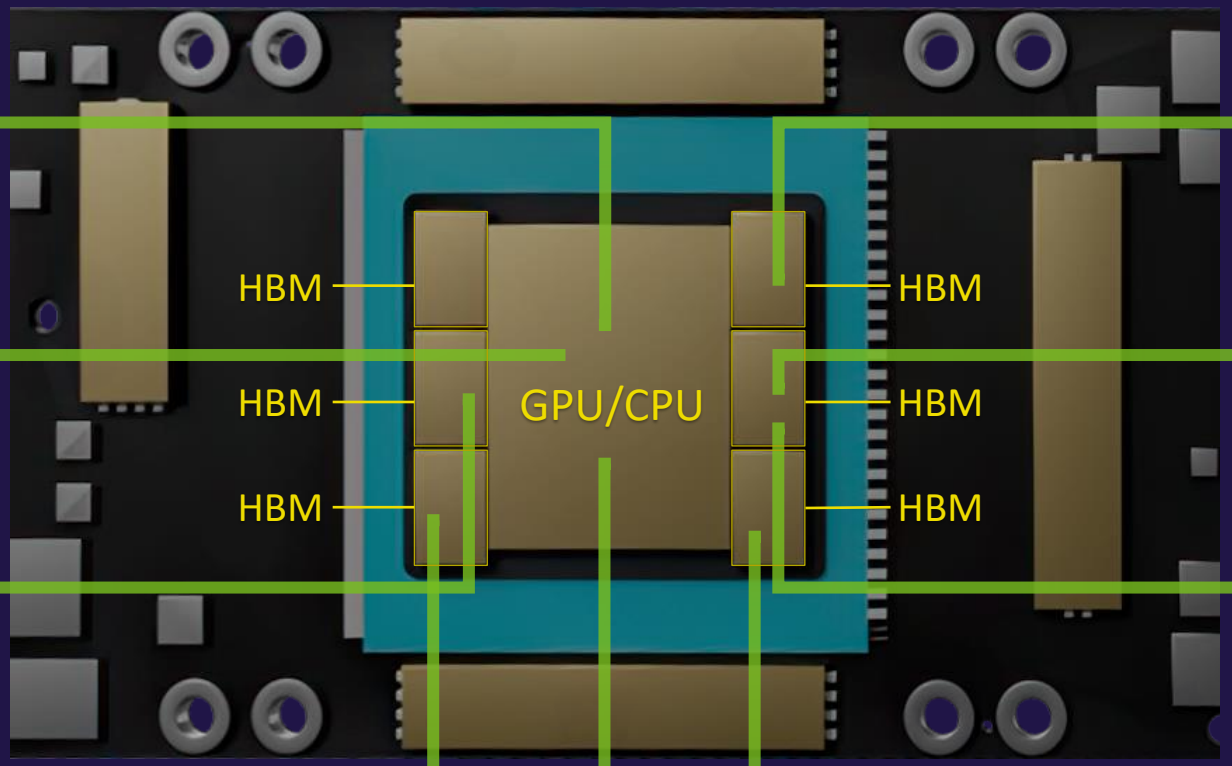
Logic
GAA / CFET

Logic
Backside PDN

DRAM
VCT $4F^2$ / 3D DRAM

Super Flat Wafer

AI Semiconductor



Advanced Packaging

Heat Spreader

3DIC
Chiplet Integration

Stack Memory
HBM, etc.

Known Good Die

* GAA : Gate All Around
* Backside PDN : Backside Power Delivery Network
* VCT : Vertical Channel Transistor

Expanding Opportunities : Wide Product Portfolio

Frontend

Advanced Packaging

Deposition

Lithography

Etch

Cleaning

Test

3D Integration

Batch Deposition

Semi-batch Deposition

Single Deposition

Coater/ Developer

Plasma Etch

Gas Chemical Etch

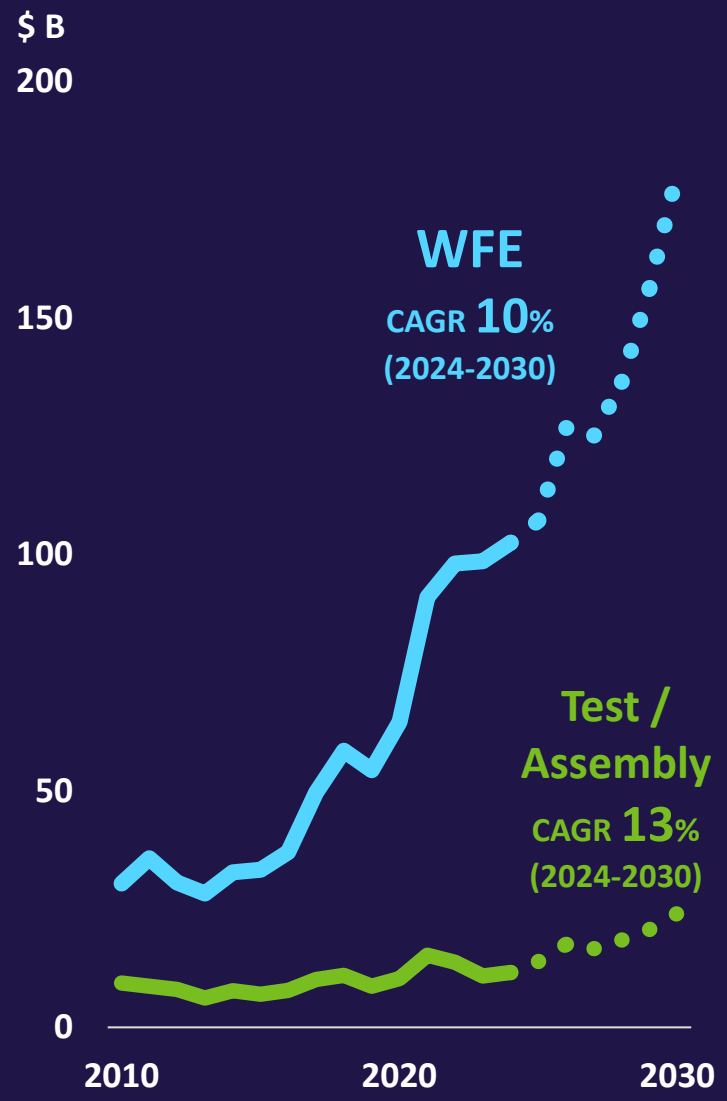
Cleaning

Prober

Wafer Bonder/ Debonder

Wafer Edge Trimming

The Equipment Market Will Grow with the Dual Engine

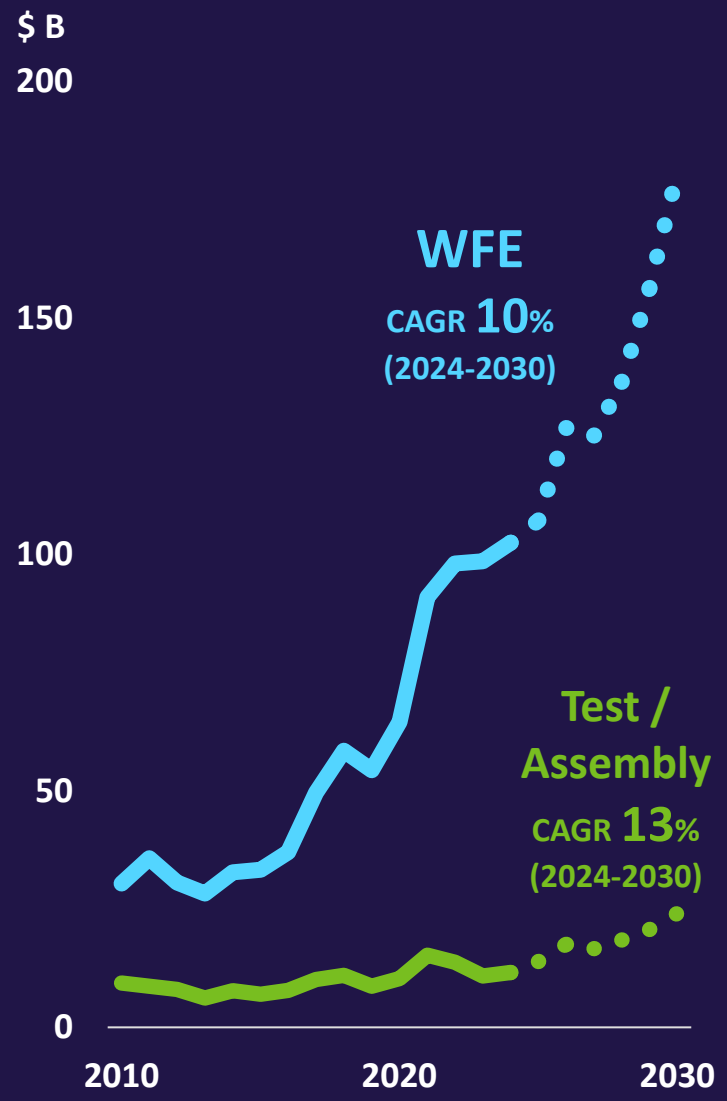


Source : TechInsights (December, 2024)

Market forecast in the next 6 years

WFE	x 1.8
Test / Assembly	x 2.1

The Equipment Market Will Grow with the Dual Engine



Source : TechInsights (December, 2024)

Frontend

Logic : GAA, BSPDN

- EUV Coater/Developer
- Gas Chemical Etch
- Conductor Etch
- PVD Metal Overburden
- CFET/Inner Spacer Plasma CVD for filling film
- Double-sided scrubber
- Backside/bevel cleaning
- Pattern Shaping
- Wafer Bonder
- Laser Tool

DRAM: DDR5, 3D DRAM

- EUV Coater/Developer
- Capacitor Mold Etch (major monopoly)
- Batch High-k Capacitor deposition
- PVD Metal Hardmask
- Supercritical Cleaning
- Backside/bevel cleaning
- Wafer Bonder
- Laser Tool

NAND: beyond 4xx

- Slit Etch (major monopoly)
- Channel Hole Etch (Plug)
- Batch Mo deposition
- Batch cleaning WL Separation
- Wafer Bonder
- Laser Tool

Advanced Packaging

Logic Packaging

- Interposer, Polyimide, PR Coater/Developer
- TDV Etch
- Batch High-k Capacitor depo
- Wafer Bonder
- Laser Tool

HBM Packaging

- Polyimide, PR Coater/Developer
- Metal Etch for HBM
- Aerosol Cleaning
- Temporary Bonder/Debonder

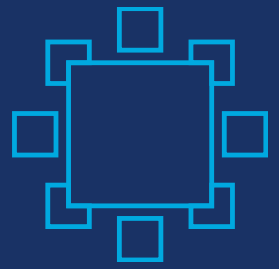
Advanced Logic / Memory Test

- Prober sales expected to double compared to last year

Investment for Future Growth (FY2025 to FY2029)

R&D Investment

1.5
Trillion Yen



Capex

700
Billion Yen

Recruitment

10,000
People

2,000 people / year

Planning proactive investments for further growth

Video : Manufacturing DX with AI and robotics

Aiming for the Next Generation Production

New Production Building Construction at Tokyo Electron Miyagi

TEL's Ingredients for Success

- Respect for Human Rights
- Climate Change and Net Zero
- Product Energy Efficiency
- Best Products with Innovative Technology
- Best Technical Service with High Added Value
- Customer Satisfaction and Trust
- Supplier Relationship

- Employee Engagement
- Safety First Operation
- Quality Management
- Compliance
- Ethical Behavior
- Information Security
- Enterprise Risk Management

Semiconductors Are The Future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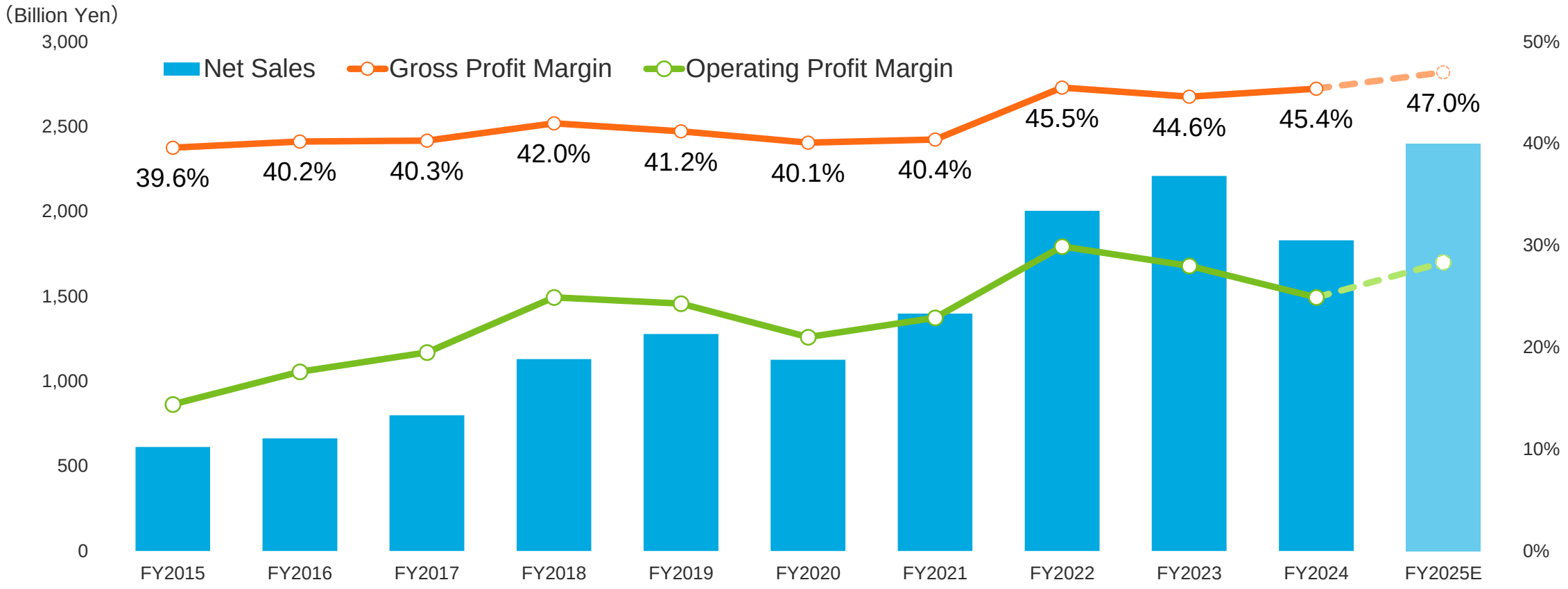
Elevating Financial Position and Points for Future Growth

February 26, 2025

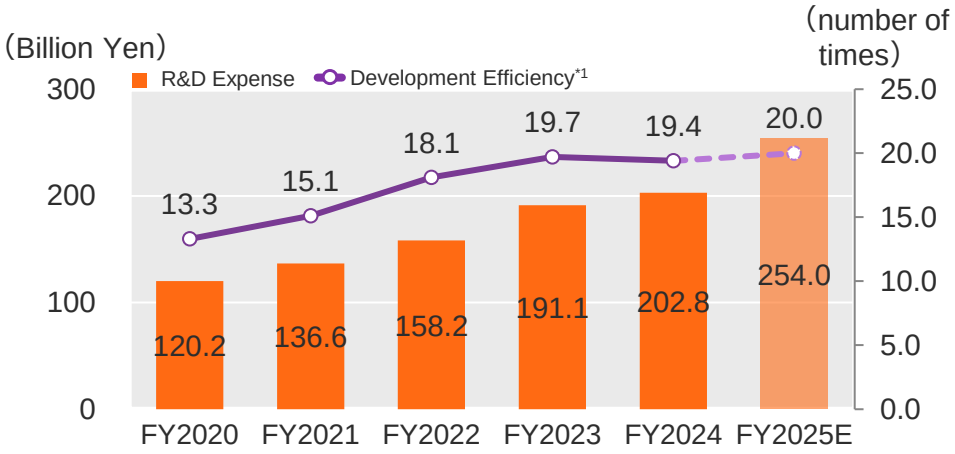
Hiroshi Kawamoto
Division Officer, Finance Division
SVP & GM

Net Sales and Gross Profit Margin Trend (FY2015 – FY2025)

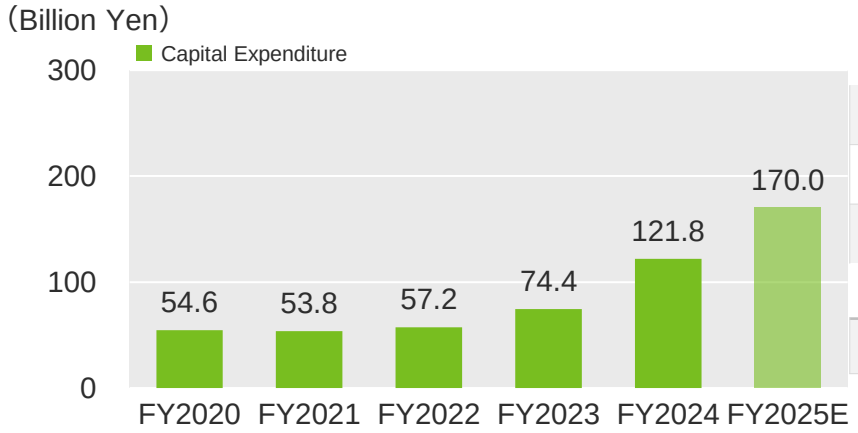


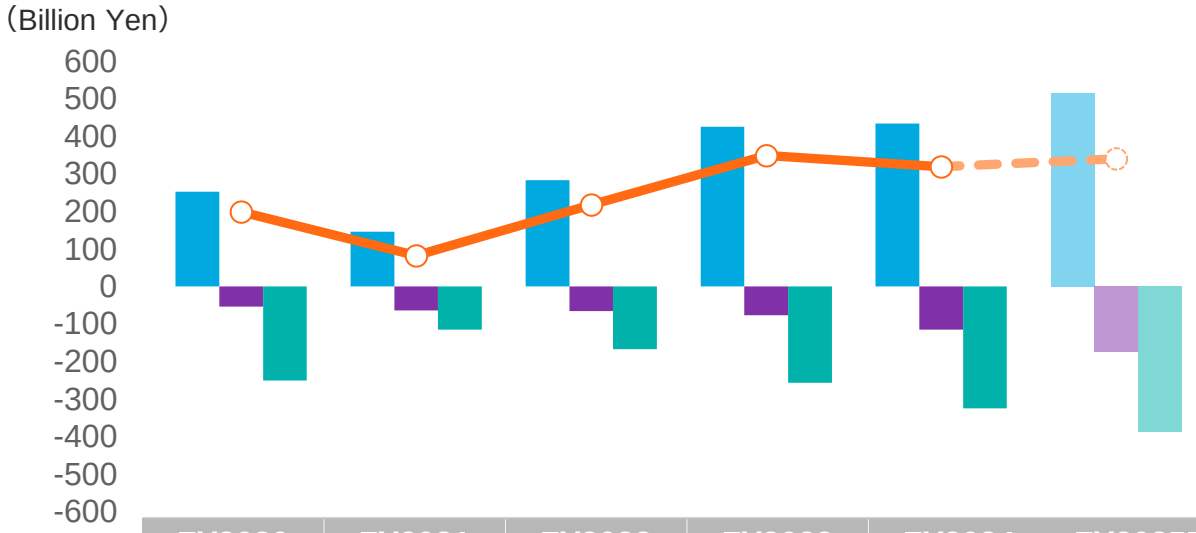
Gross profit margin rose significantly on high value-added products and improved production efficiency

Growth Investment and Cash Flow



*1 Aggregated by dividing the total net sales in the last 5 years by the total R&D expense in 6 to 10 years before



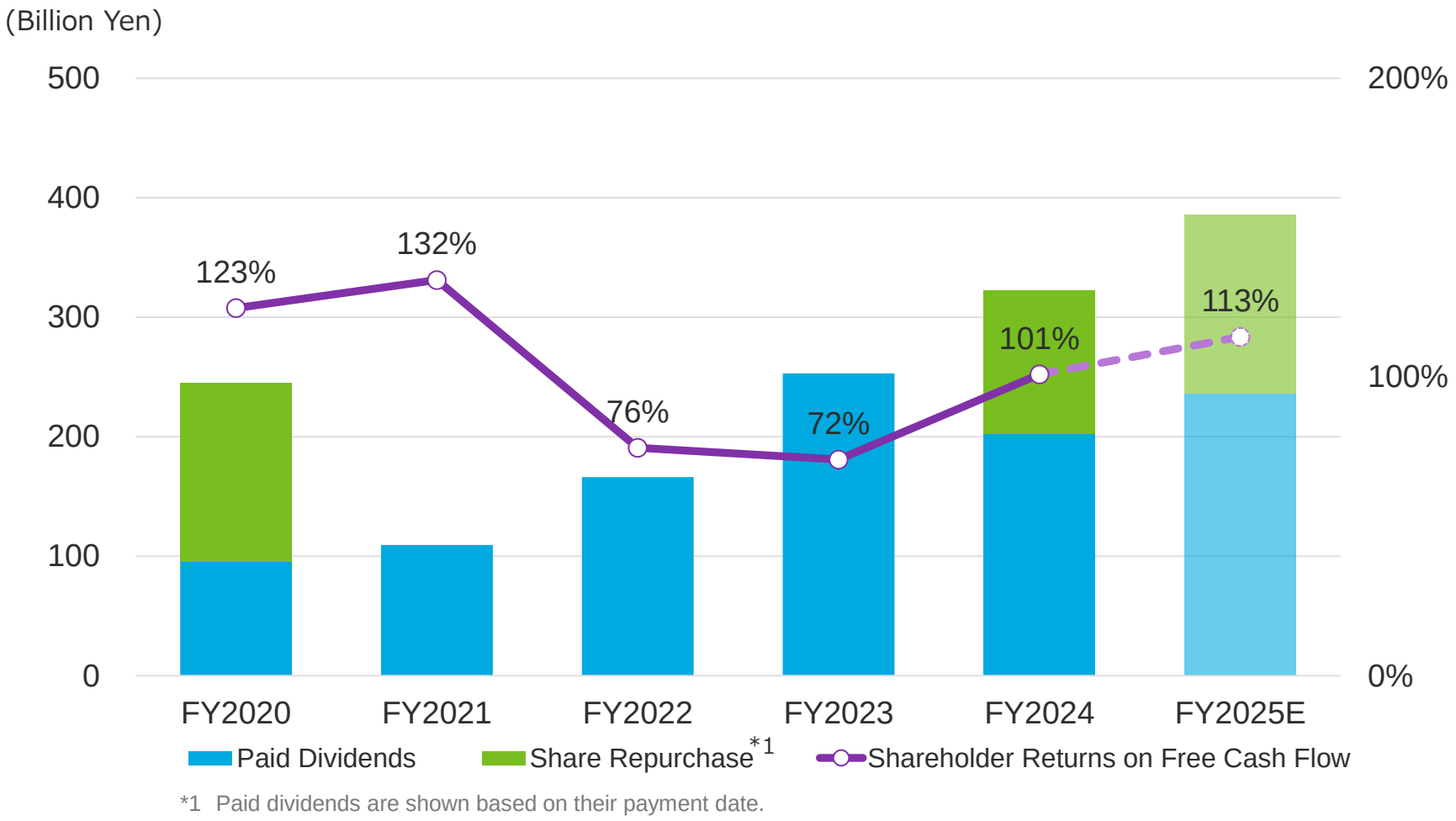


	FY2020	FY2021	FY2022	FY2023	FY2024	FY2025E
Cash flow from operating activities	253.1	145.8	283.3	426.2	434.7	
Cash flow from investing activities*2	-53.5	-63.2	-65.6	-76.7	-115.0	
Cash flow from financing activities	-250.3	-114.5	-167.2	-256.5	-325.0	
Free cash flow*3	199.5	82.6	217.7	349.4	319.6	
Cash on hand*4	338.4	311.5	371.2	473.1	472.5	

*2 Cash flow from investing activities excludes changes in time deposits and short-term investments.
*3 Free cash flow = “Cash flow from operating activities” + “Cash flow from investing activities” (excluding changes in “Time deposits” and “Short-term investments”).
*4 Cash on hand includes “Cash and cash equivalents” + “Time deposits and short-term investments” with original maturities of more than three months.

Robust cash flow supports aggressive growth investment

Shareholder Returns Trend



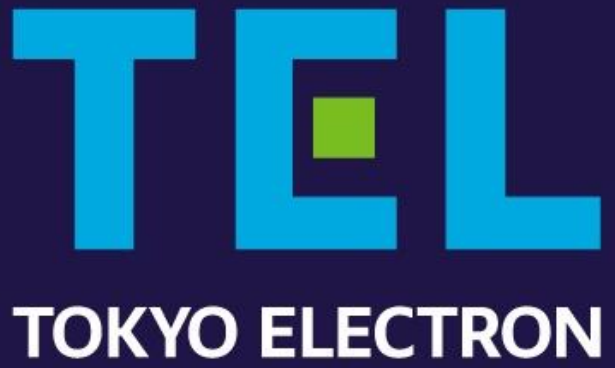
*1 Paid dividends are shown based on their payment date.

Aim for continuous high level of cash generation and shareholder returns

Summary

- Elevating gross profit margin
  - High value-added products
  - Production efficiency enhancement
- Continuous growth investment
  - Conduct R&D/capex with an eye to market growth
  - Support growth investment by robust cash flow
- Shareholder returns
  - Disburse record-high shareholder returns for FY2025
  - Continue to aim for high shareholder returns

Continue aggressive growth investment and shareholder returns through raising gross profit margin and a high level of cash generation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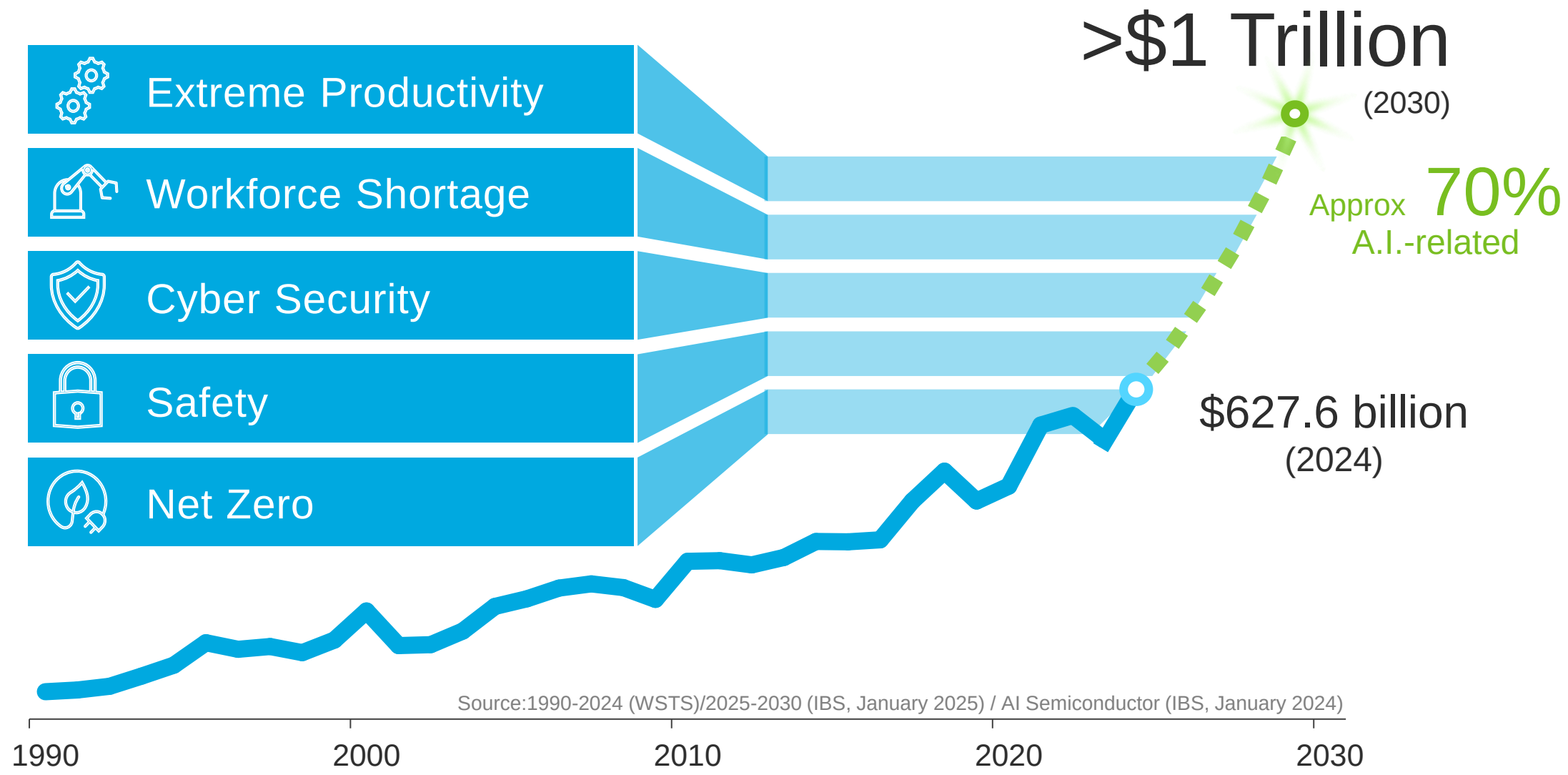
Opportunities in Frontend Process Business and Activities in Digital x Green

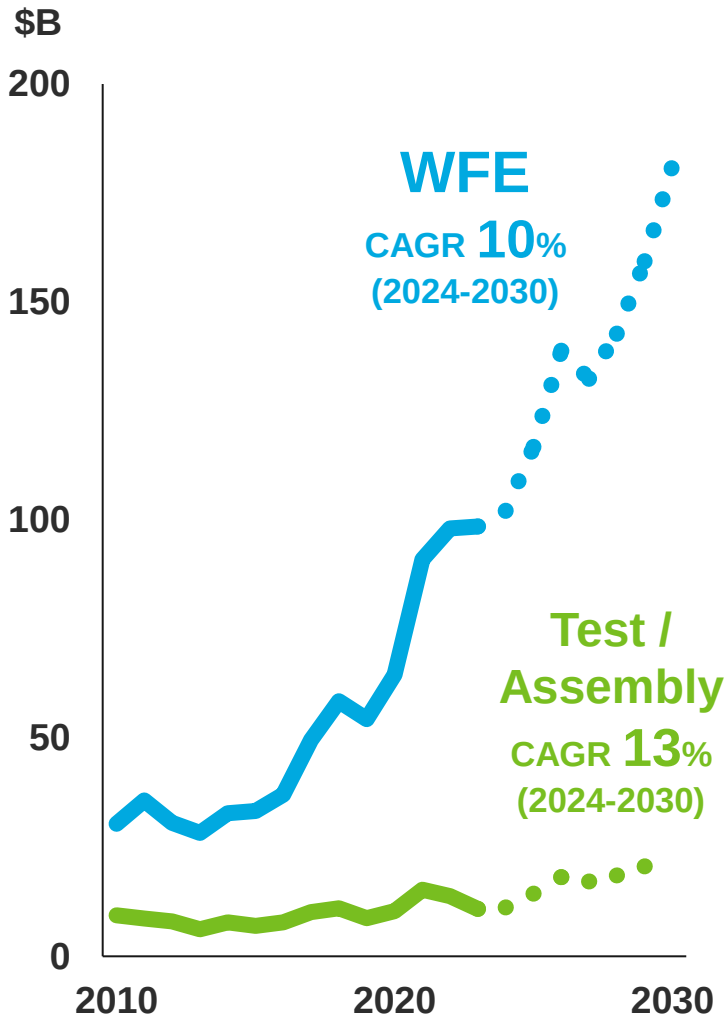
February 26, 2025

Hiroshi (Jack) Ishida
Division Officer, Frontend Process Business Division
SVP & GM

Challenges for the $1 Trillion Market



Our Growth Opportunities in the Frontend Market

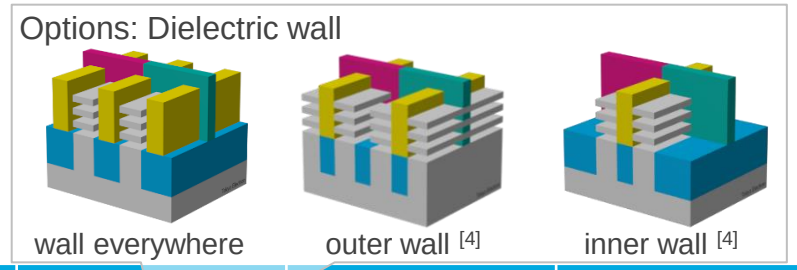


Source : TechInsights

- CAGR driven by AI-related devices to continue to drive high growth of WFE’s CAGR
- Leveraging TEL's strengths to address high-growth market areas:
  - Leading-edge logic: The etch market is expected to grow by 2.7 times, the deposition market by 2.5 times*
  - DRAM: The etch market is expected to grow by 2.3 times, exceeding the CAGR of WFE*
- By introducing new products focused on the key technological inflection points, we aim to further expand our areas of entry

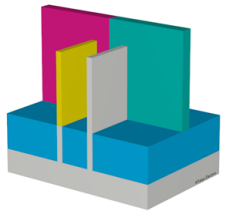
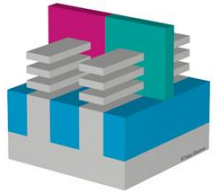
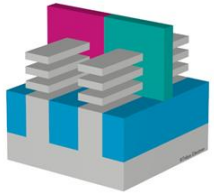
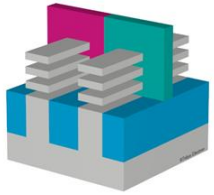
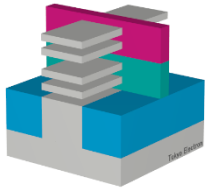
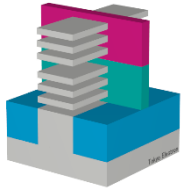
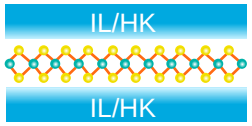
* TEL Estimates

Logic Technology Roadmap (Generic)



[1] Chih-Hao Chang (TSMC) et al., IEDM 2022
[2] Shien-Yang Wu (TSMC) et al., IEDM 2022
[3] Sandy Liao (TSMC) et al., IEDM 2024
[4] Mertens and Horiguchi (imec), EDTM 2024

Source: TEL estimates

Year of HVM (20k/month)	2022~24	2025~2026	2027~28	2029~30	2031~32	2033~34	2035~36	2037~38
Node	**3nm**	**2nm/18A/16A**	**14A**	**10A**	**7A**	**5A**	**3A**	**2A**
Transistor	2~1 Fin 	GAA NS 	GAA NS scaling 	GAA NS extension 	CFET 	2nd Gen. CFET 	3rd Gen. CFET 	2D material stack  2D material: TMDC MoS_2, WS_2, $MoSe_2$, WSe_2 etc.
Poly Pitch [nm]	48~45 [1]		45~42		48 [3] ~42	45~39		36
Min. Metal Pitch [nm]	23 [2]		20	18	17	16	14	12
Interconnect booster	Cu Barrier/Seed CIP Backside PDN (HPC)			Cu CIP or Ru subtractive	Ru subtractive AR>3, Airgap	New alloy AR>5, Airgap, BEOL Transistor		
EUV Patterning Technology	EUV MP*1, SE*2			EUV MP, SE High-NA SE		High-NA MP, SE EUV MP, SE		
Resist	CAR*3			CAR (+MOR*4)	CAR+MOR			

*1 MP: Multi-Patterning, *2 SE: Single-Exposure, *3 CAR: Chemically Amplified Resist, *4 MOR: Metal Oxide Resist

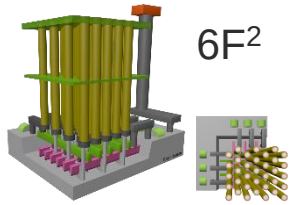
Logic scaling will continue by changing transistor structure and material evolution

DRAM Technology Roadmap (Generic)

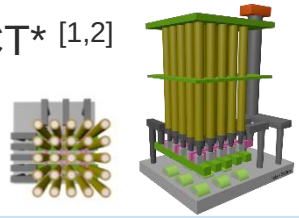
Source: TEL estimates

Year of HVM (20k/month)	2023-24	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
Node	1b	1c	1d	0a		0b		0c	0d		0e	
Cell layout / Structure	2D									3D		
F [nm] in $6F^2$	13~12.5	12~11	10	9		8		7	(3D ~1xxL)		(3D >1yyL)	
Cap. pitch [nm]	39~37.5	36~33	30	27		24		21				
Cap. A.R.	>50	>55	>65	>70		>75		>80				
Cap. Mat.	ZrAlHfO			Alternative (HfZrO Anti Ferro. etc)								
WL	TiN			Low R metal								
Peri. CMOS	HKMG									FinFET		
HBM	HBM3E (8/12Hi,24/36GB)		HBM4 (12/16Hi,36/48GB)		HBM4E (16Hi,64GB)		HBM5 (16,20Hi, 64/80GB)		HBM5E		HBM6	

$6F^2$



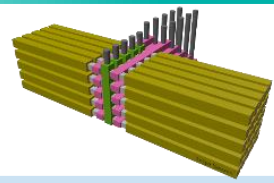
$4F^2$ VCT* [1,2]

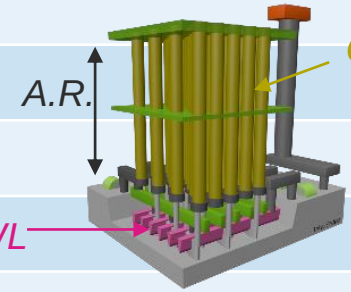


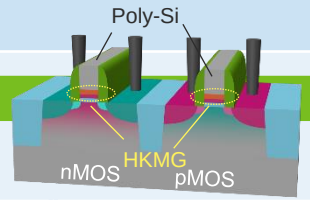
* Vertical Channel Transistor

[1] Seokhan Park (Samsung) et al., IEDM 2023

[2] Daewon Ha (Samsung) et al., IEDM 2023





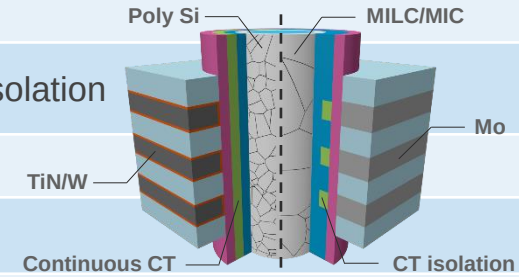


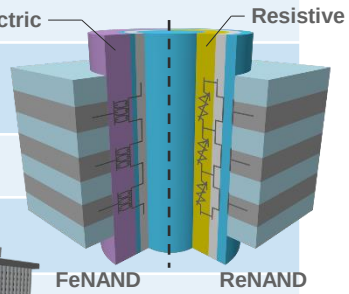
Bonding

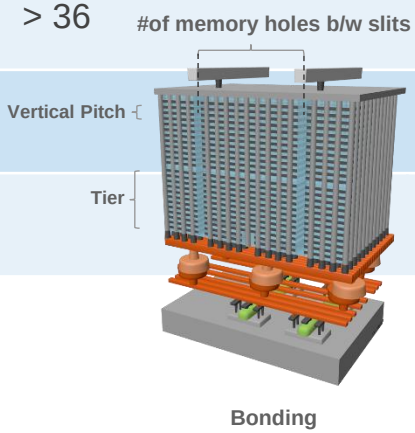
NAND Technology Roadmap (Generic)

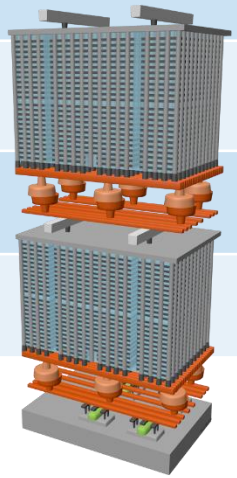
Source: TEL estimates

Year of HVM (20k/month)	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
Stack (~1.3x/1.5years)	3xxL		4xxL	5xxL		7xxL	1xxxL		*1yyyL	*1zzzL		*2xxxL
Tier	2 or 3		3 or 4	3 or 4		3 - 5	4 - 6		5 - 7	6 - 8		7 - 10
Vertical pitch [nm]	39 - 45		38 - 43	38 - 42		37 - 41	36 - 40		35 - 39	34 - 38		33 - 37
Memory height [μm]	12 - 14		15 - 19	18 - 27		24 - 36	34 - 45		45 - 62	57 - 74		70 - 84
Charge trap (CT)	Continuous CT					CT isolation				Fe/Re NAND[3]		
Channel	Poly Si grain CIP			MILC[1]/MIC[2]								
WL metal	W or Mo		Mo									
#holes btw. Slits	14 - 20		19 - 25	24 - 32		30 – 36	> 36					
Layout/Structure	Under array or Bonding		Bonding			Bonding or Multi Bonding						
Peri. CMOS	Poly Si Gate					HKMG						









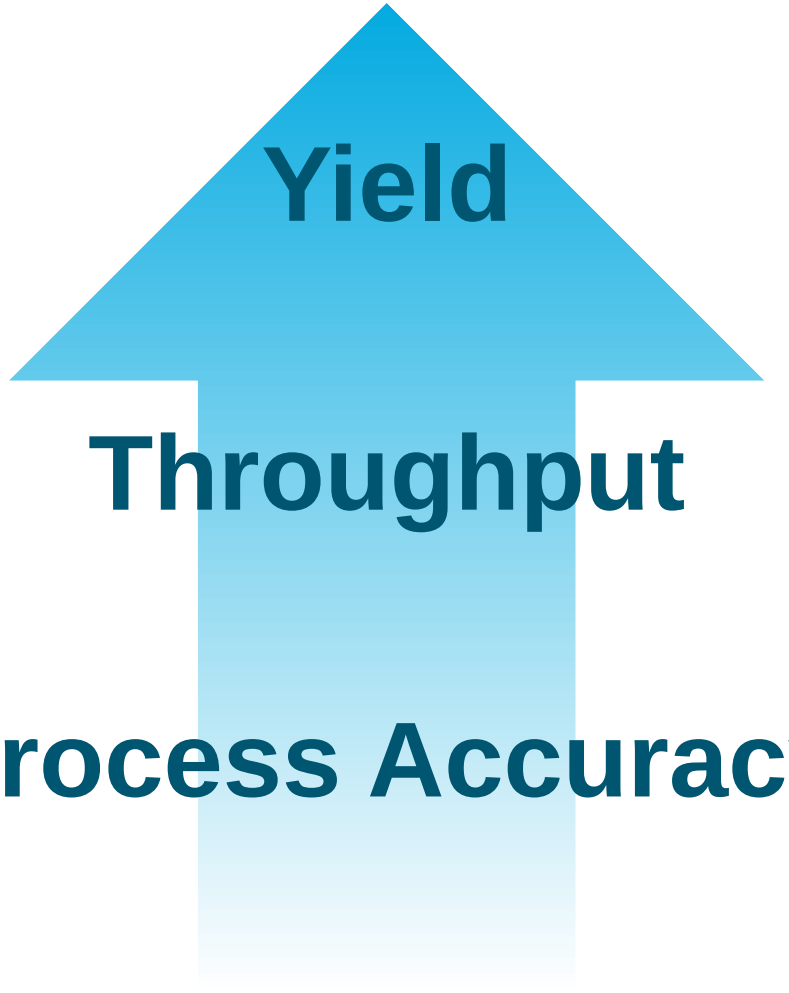
* Trend Extrapolation
[1] Metal induced lateral crystallization, N. Ishihara (Kioxia) et al., VLSI 2023
[2] Metal induced crystallization
[3] Jeehoon Han (Samsung) et al., IEDM 2023

Growth opportunities at Technological Inflection Points in Frontend Process

- Logic: GAA*1, BSPDN*2, CFET
  - Adaption of High-NA lithography, combined with multi-patterning and MOR technologies, presents opportunities for new technology Acrevia™
  - Adoption of multi-patterning to increase demand for deposition, etch, and cleaning processes.
  - GAA and CFET transistors to drive an increase in gas chemical etch processes
  - New materials like ruthenium and structural innovations such as air gaps to generate fresh opportunities
- DRAM: HBM, VCT*3, 3D DRAM
  - Adoption of multi-patterning driving increased demands in deposition and etch
  - Capacitor formation remains essential, driving ongoing demand for advanced etch and deposition
  - 3D DRAM leading to increased processes in deposition, etch and gas chemical etch
- NAND: Beyond 4xx
  - Increased layer counts leading to higher investments in deposition and etching processes
  - High aspect ratio etch to become increasingly important
  - New materials such as molybdenum, and low-resistance channel silicon to be utilized

*1 GAA: Gate All Around
*2 Backside PDN: Backside Power Delivery Network
*3 VCT: Vertical Channel Transistor

Provide High Value-Added Products for Sustainable Growth



Leveraging Digital Transformation (DX)

Best Product Dev. | Start up / Process Ramp up | Production | Best Service Delivery

MI (Materials Informatics)

Self-diagnostics (Sensors)

Robotics

PI (Process Informatics)

High Throughput Platform

AR/VR

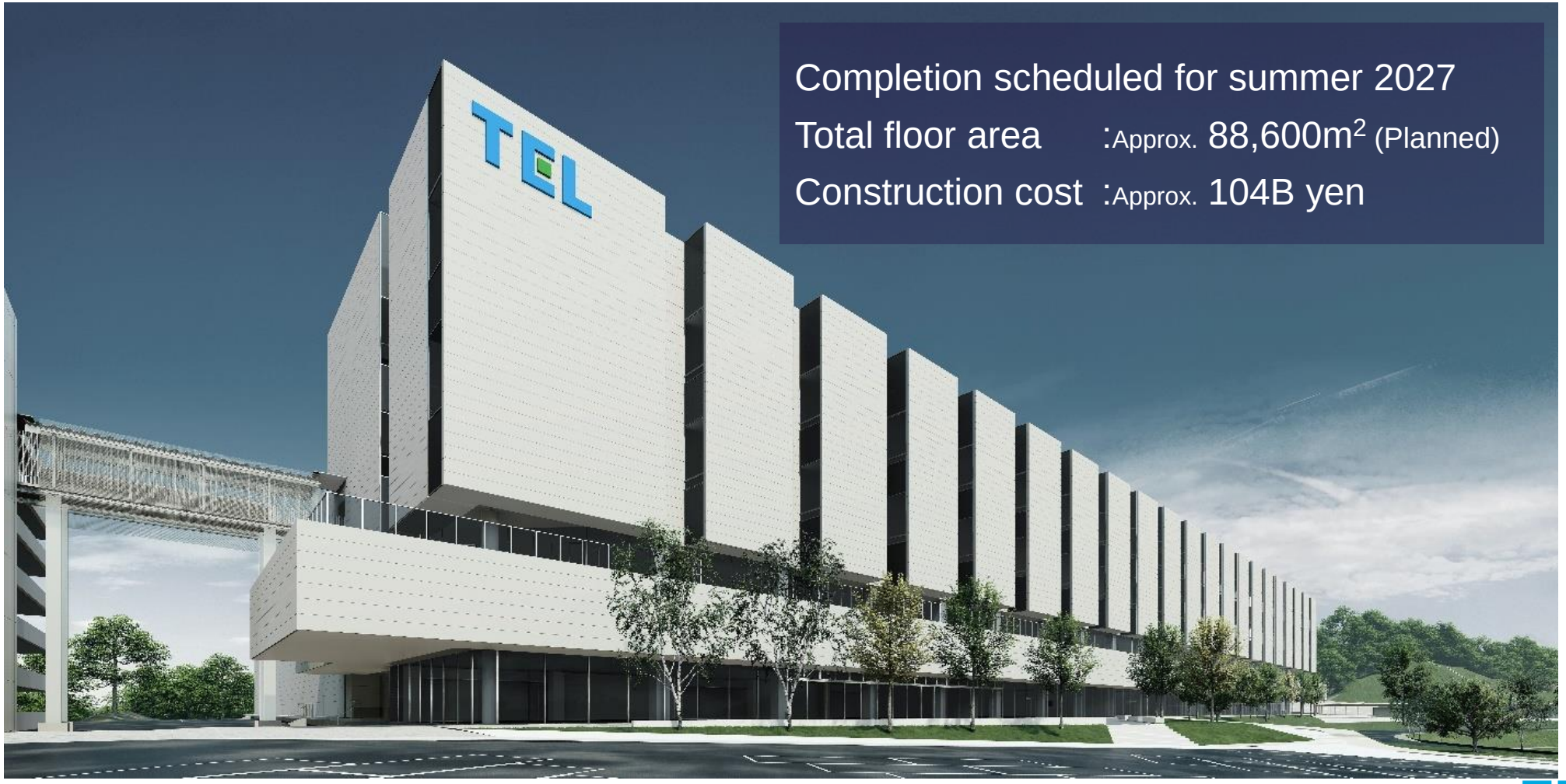
Developing digital enablers for use throughout the business
to leverage productivity and profitability

Leveraging Digital Transformation (DX) in Field Solutions

Maximize work efficiency for startup and maintenance in the Clean Room by using smart glasses and remote expert support. Use of AR/VR and DX including digital twin technology.

Use of robots for parts replacement without human assistance is expected to minimize downtime and improve the quality of engineering work.

Aiming for the Next Generation Production:
New Production Building at Tokyo Electron Miyagi



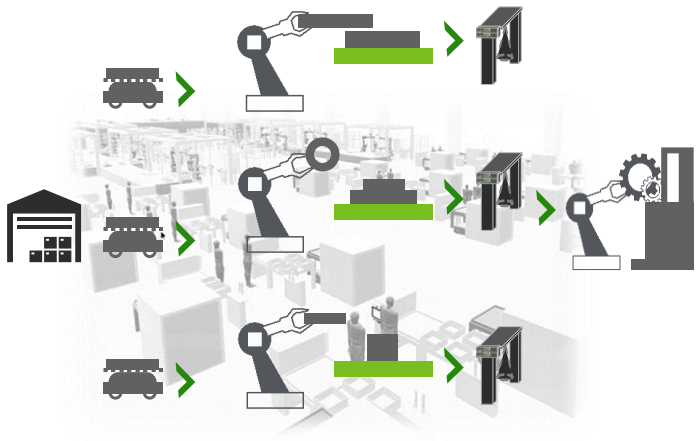
Vision for Smart Production

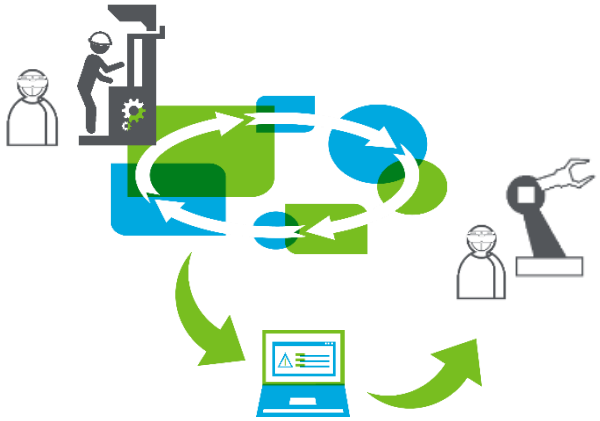
- Achieve sustainable manufacturing for the future

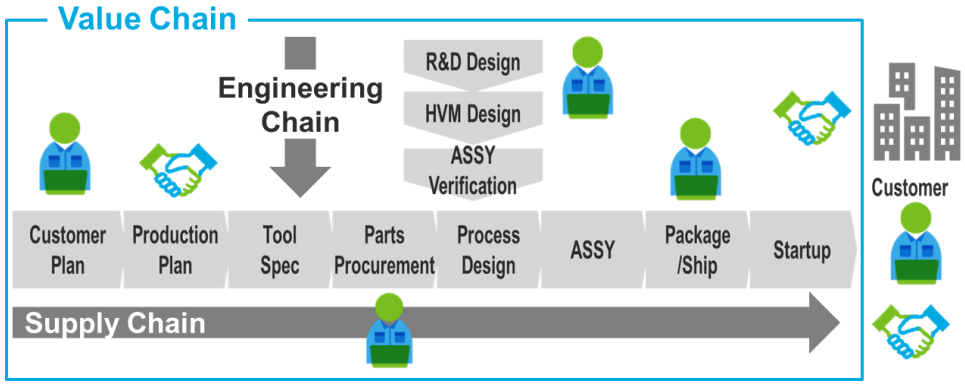
Overwhelming Efficiency
through automation and standardization

Enhancing Adaptability
to internal and external environmental changes

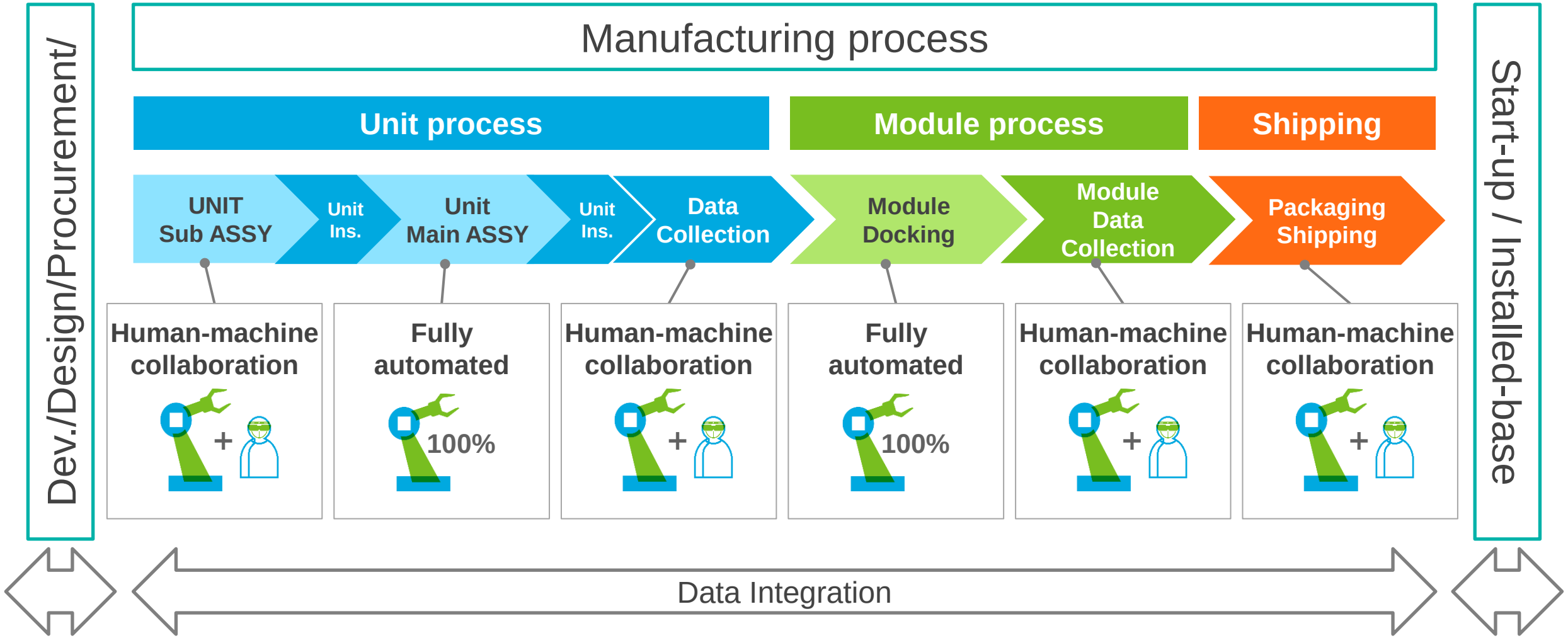
Product & Service Quality Improvement
through enhanced value chain





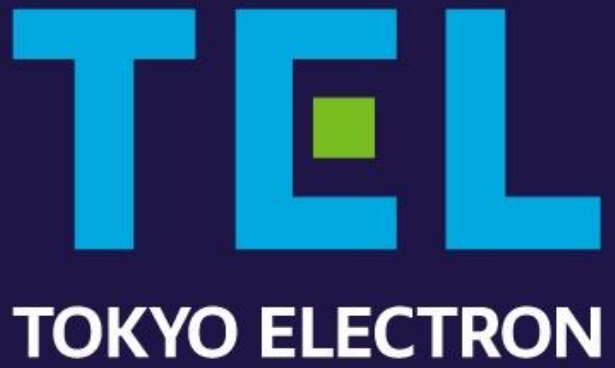


Concept of Smart Production



Summary

- Aiming for further growth in frontend equipment in the volume zone of the market
  - Advance the introduction of new products in growth areas related to AI
  - Provide high-value-added equipment that leverages our technology in technological inflection points
- Support sustainable growth in the semiconductor market through Digital x Green initiatives
  - Promote the adaption of high-productivity equipment, labor-saving techniques, process reduction, and energy-saving technologies
  - Enhance productivity and profitability in semiconductor manufacturing through the implementation of DX and robotics
  - Increase productivity and profitability of equipment through smart production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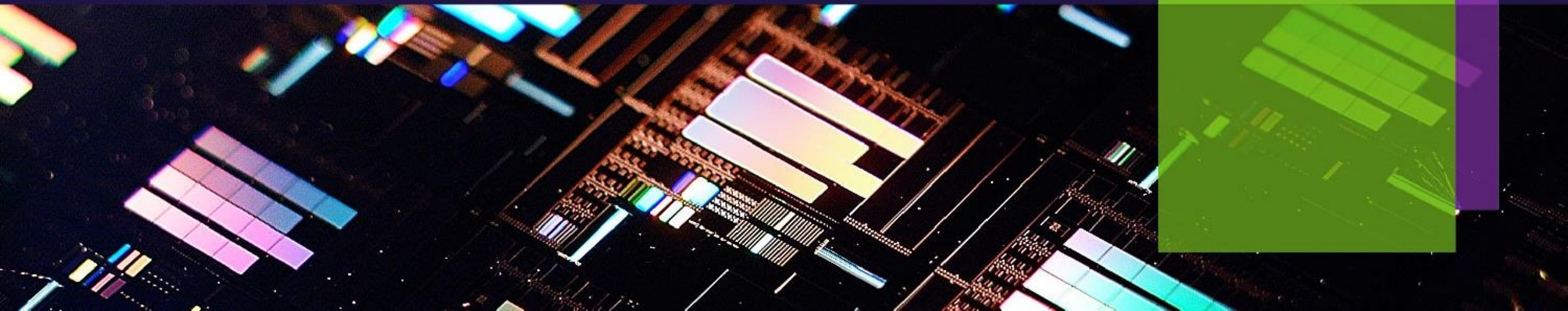
Activities in Coater/Developer and Cleaning System

February 26, 2025

Yasuhiro Washio
CTSPS BU
VP & GM



Coater/Developer

Coater/Developer: CLEAN TRACK™ LITHIUS Pro™ Z for EUV

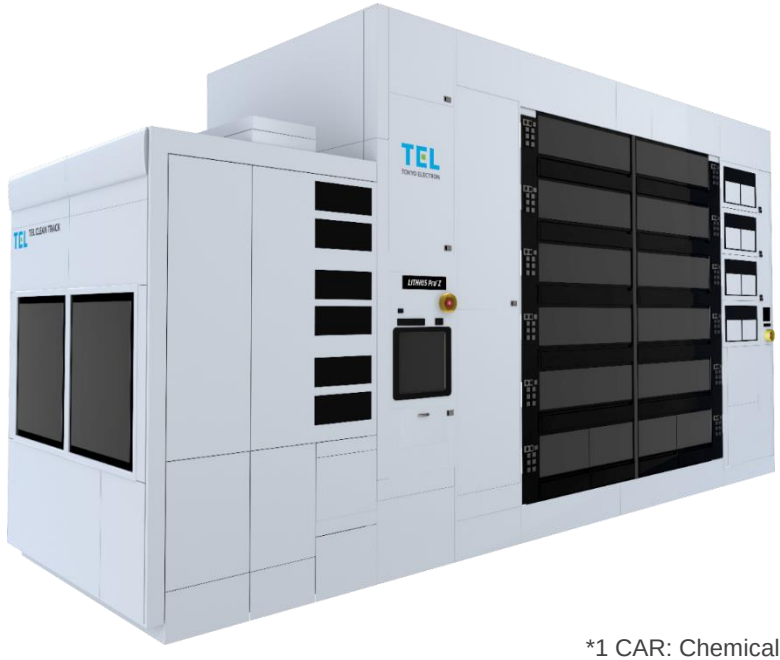
LITHIUS Pro™ Z released in 2012
(＞3000 systems shipped)

New features to support EUV CAR*1/MOR*2
to be released as on an ongoing basis

High Reliability
High share in EUV market

High Productivity
Maximizes output of EUV lithography tools, and reduces chemical consumption

High Versatility
Supports CAR, MOR and underlayers



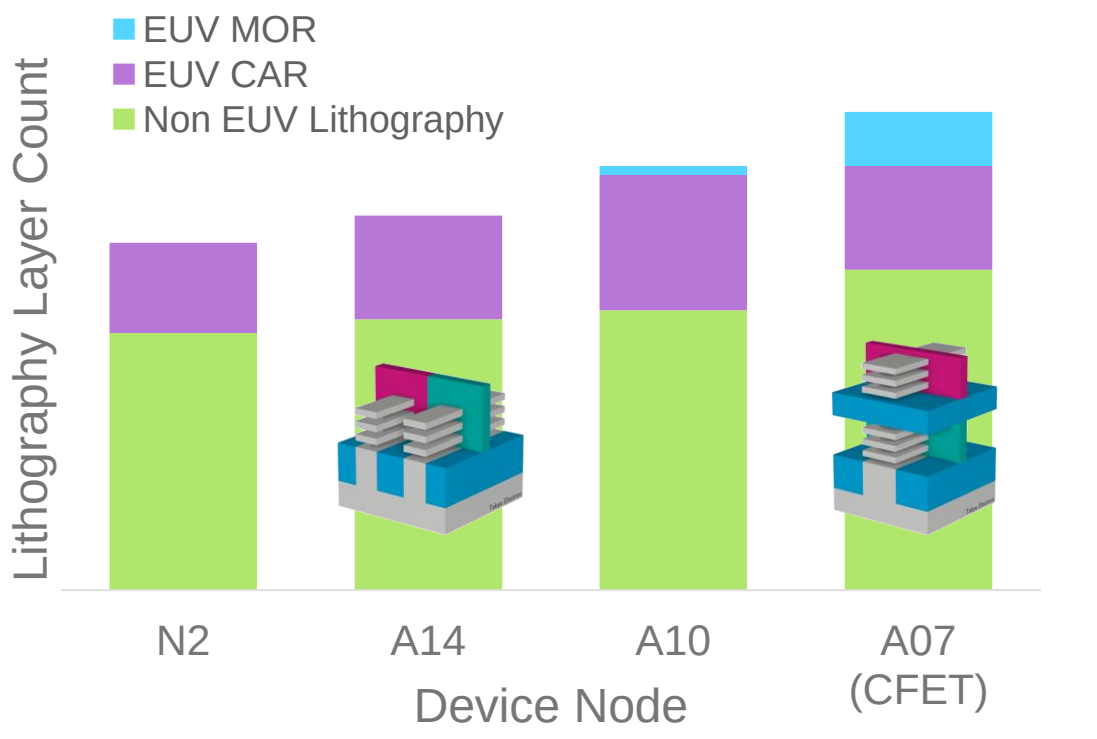
*1 CAR: Chemically Amplified Resist
*2 MOR: Metal Oxide Resist

LITHIUS Pro™ Z platform with its proven mass production for various litho tools, ensures high reliability and productivity for EUV litho, along with high versatility for next-generation EUV

Outlook on Lithography Layer Count

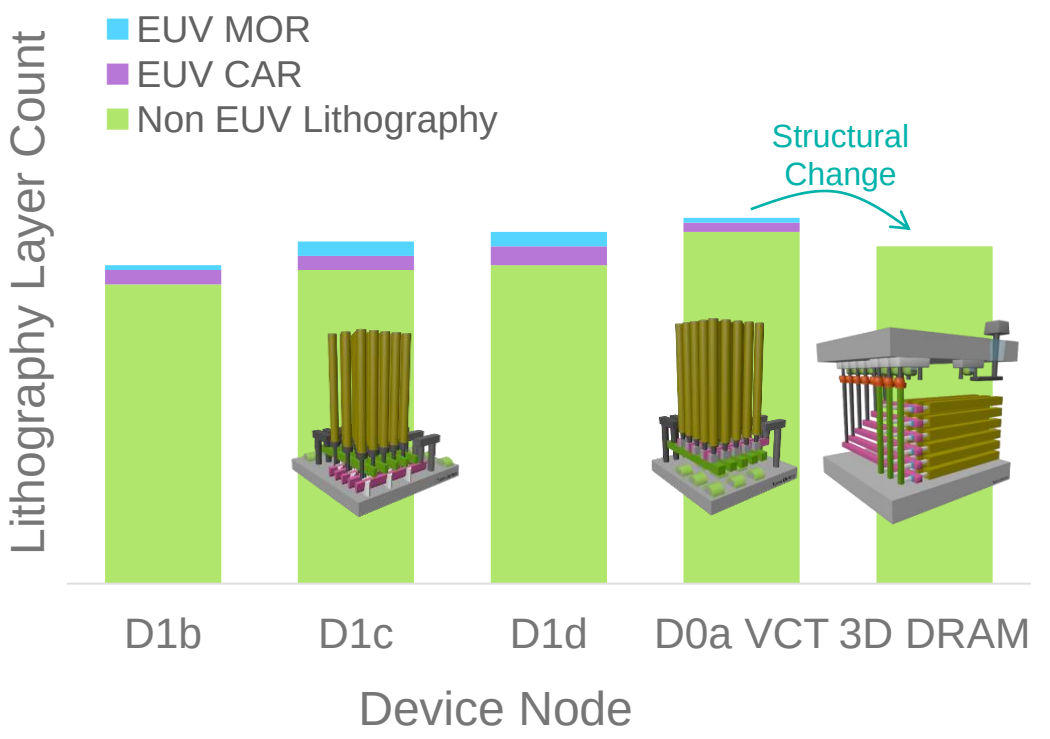
Logic

TEL Estimates



DRAM

TEL Estimates



MOR expected for Logic 10A/ DRAM D1b, development ongoing for MOR

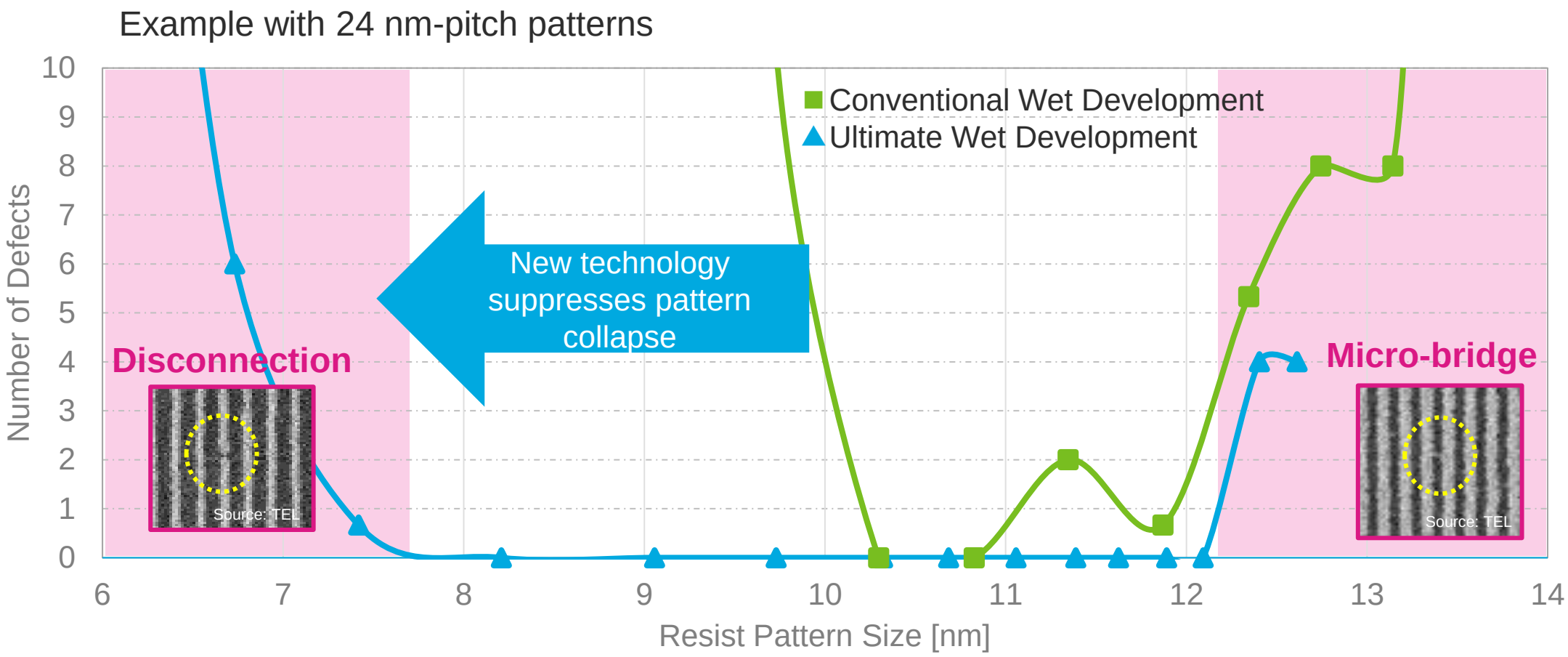
Example of MOR Solution: The Ultimate Wet Development

*1 Based on internal information and development targets
*2 Based on results of developing 24 nm-pitch lines

	Ultimate Wet Development Technology	Conventional Wet Technology	Alternative Technology
Base Technology	Coater/Developer	Coater/Developer	Etch
Process Ambient	Atmospheric	Atmospheric	Vacuum
Reaction	Chemicals	Chemicals	Corrosive Gas
Throughput*1	4x	4x	1x
Chemical Consumption*1	50% (vs. conventional)	100 %	N/A (uses gas) exhaust processed in combustion abatement post process
Anti-Pattern Collapse*1 Performance	< 8 nm*2	> 10 nm*2	< 8 nm*1
Footprint*1	In-Line	In-line	Additional Footprint

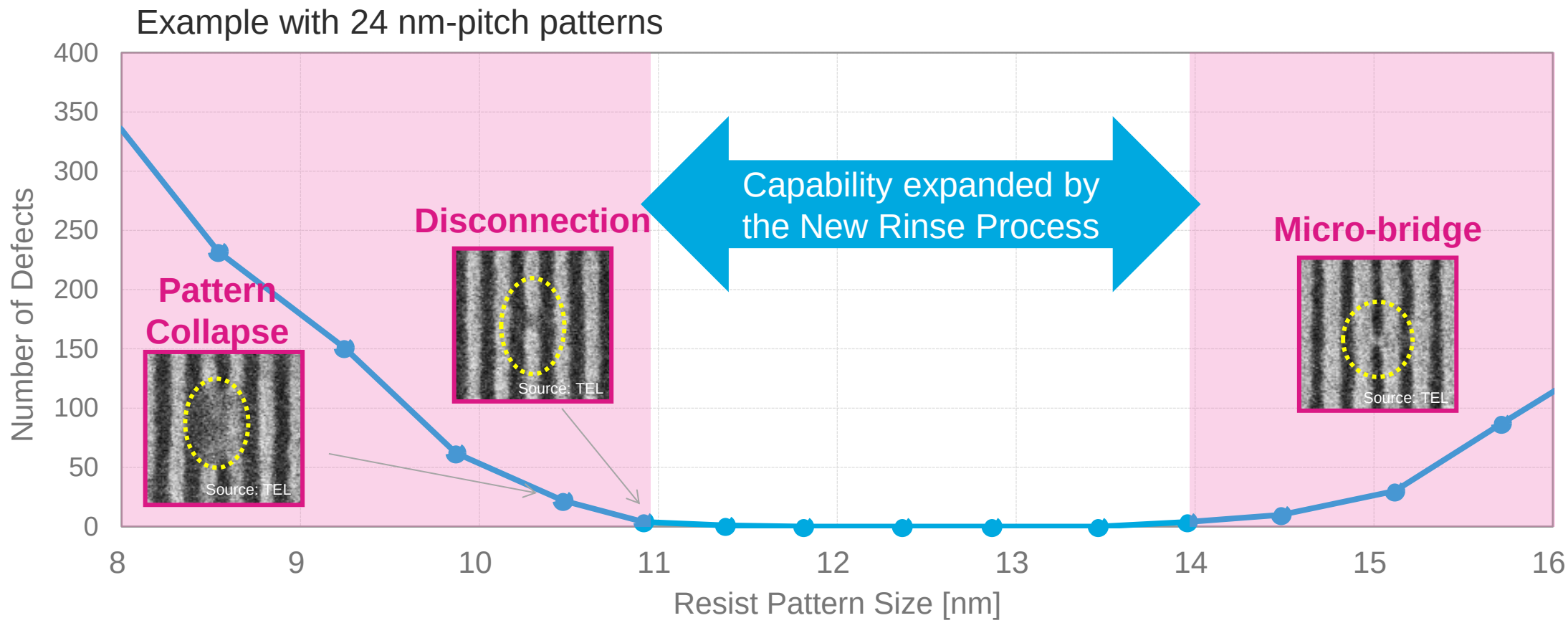
Evaluation of Ultimate Wet Development ongoing with key customers, with emphasis on productivity (throughput, footprint, maintainability, utilize existing facilities)

Example of MOR Process: The Ultimate Wet Development



The Ultimate Development technology enables the suppression of pattern collapse

Example of CAR Solution:
New Rinse Process and New Under Layer



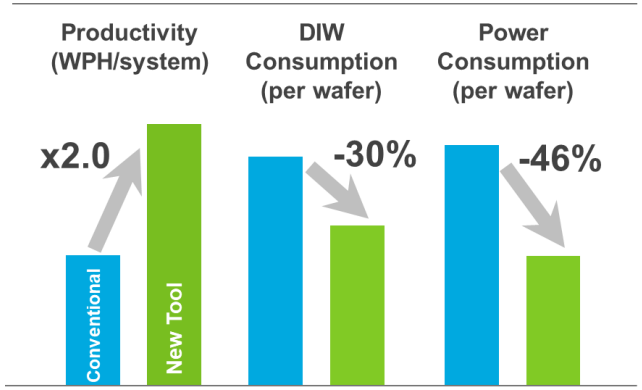
The new rinse process expands the capability of CAR to be applied to smaller patterns

Cleaning System

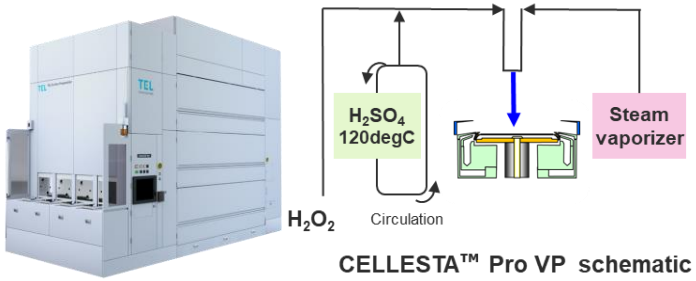
Development of Cleaning Systems

High Productivity Wet Bench (EXPEDIUS™-R)

Industry's first large-batch process (increased wafer counts)



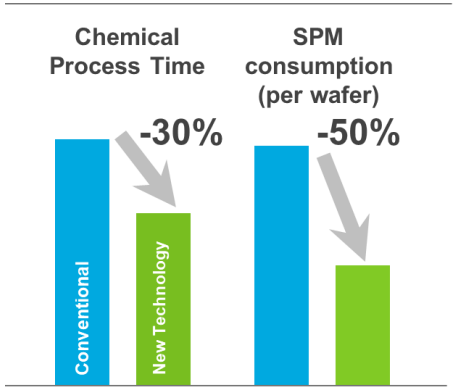
SPM*1 Vapor Technology (CELLESTA™ Pro VP)



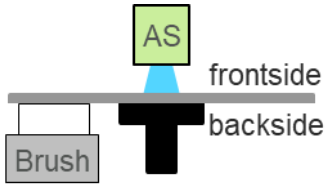
CELLESTA™ Pro VP schematic

Enabled higher temperature process due to a more effective rection by adding water vapor to chemicals

*1 SPM: Sulfuric Acid and Hydrogen Peroxide Mixture

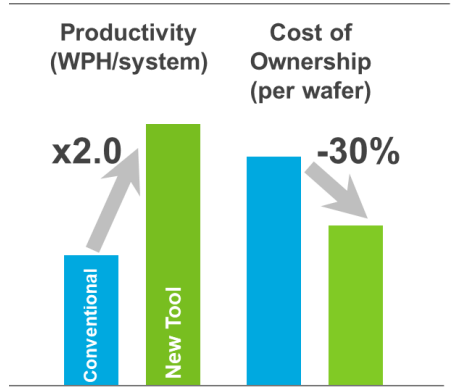


Simultaneous Scrubber (CELLESTA™ MS2)



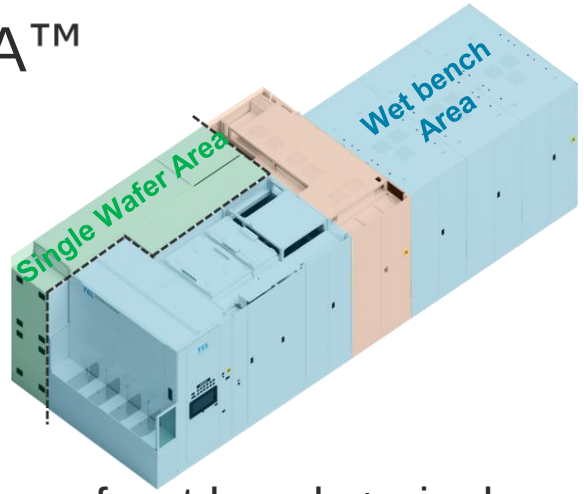
A tool enabling AS*2 process on wafer frontside and physical brushing process on wafer backside simultaneously in a single chamber

*2 AS: Atomized Spray



New Cleaning Tool: ZEXSTA™

- ZEXSTA™



A combination of wet bench + single-wafer process

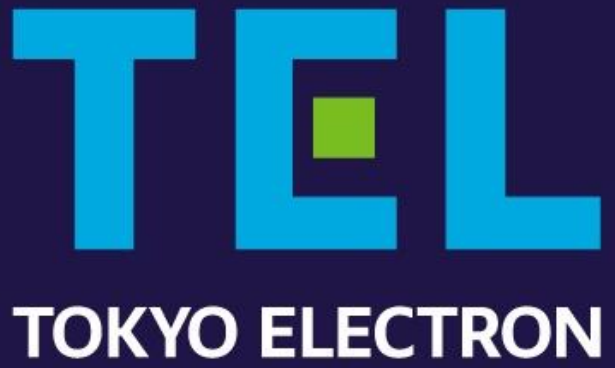
Method	Features
Wet Bench	High-temp/ long-duration process, wet etch
Single Wafer	Advanced drying technology, particle control

- Target Application
  - Advanced wet etch + advanced dry tech

    - Highly selective wet etch process will be required for also 3D DRAM in addition to 3D NAND
  - High throughput + surface cleanliness

    - High surface cleanliness is required for logic and DRAM

TEL will contribute to customer technology development by continuing to create new value, overcoming the constraints of traditional equipment classifications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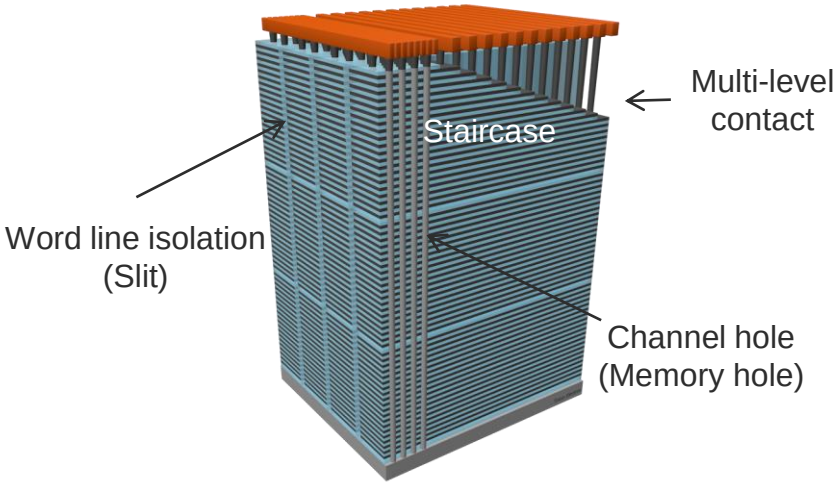
Latest Technological Challenges and Activities in Etch

February 26, 2025

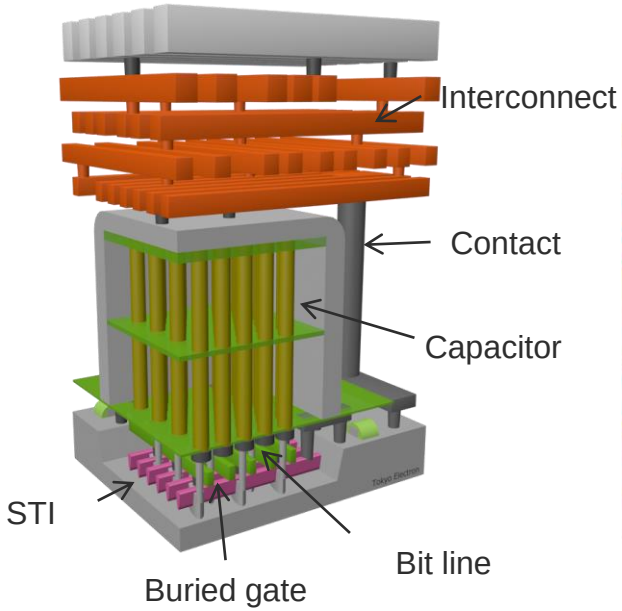
Tetsuya Nishiara
ES BU
VP & GM

Requirements and Various Etch Technologies

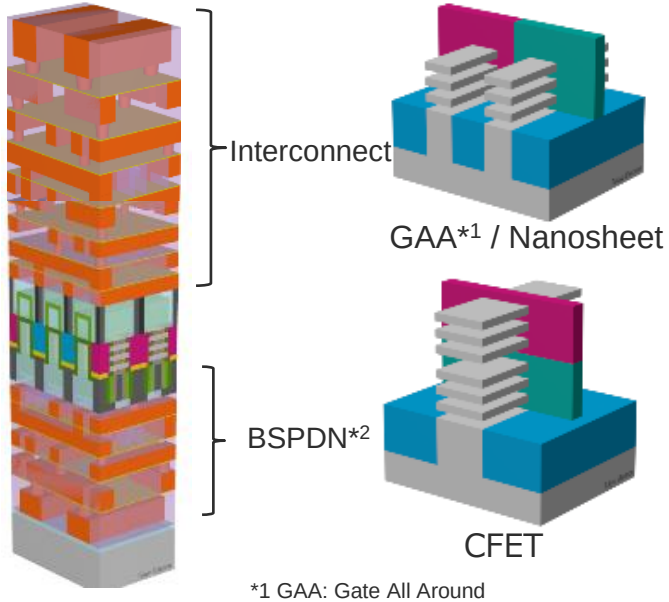
3D NAND



DRAM



Logic

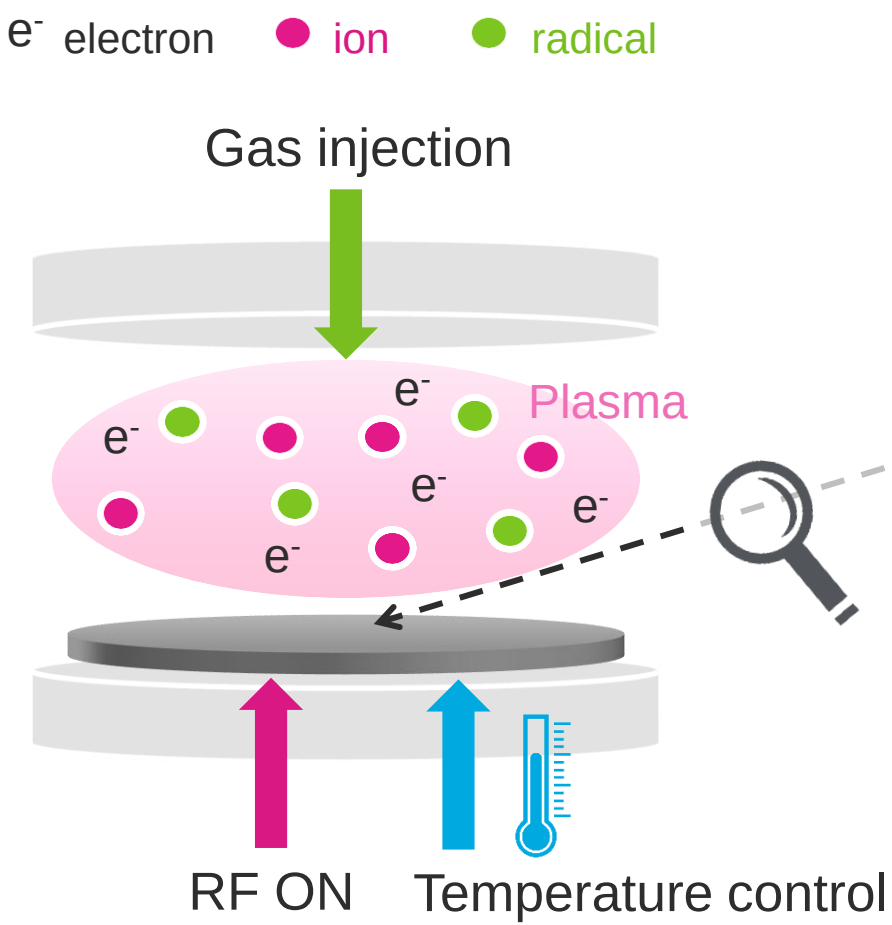


*1 GAA: Gate All Around
*2 BSPDN: Backside Power Delivery Network
*3 CD: Critical Dimension

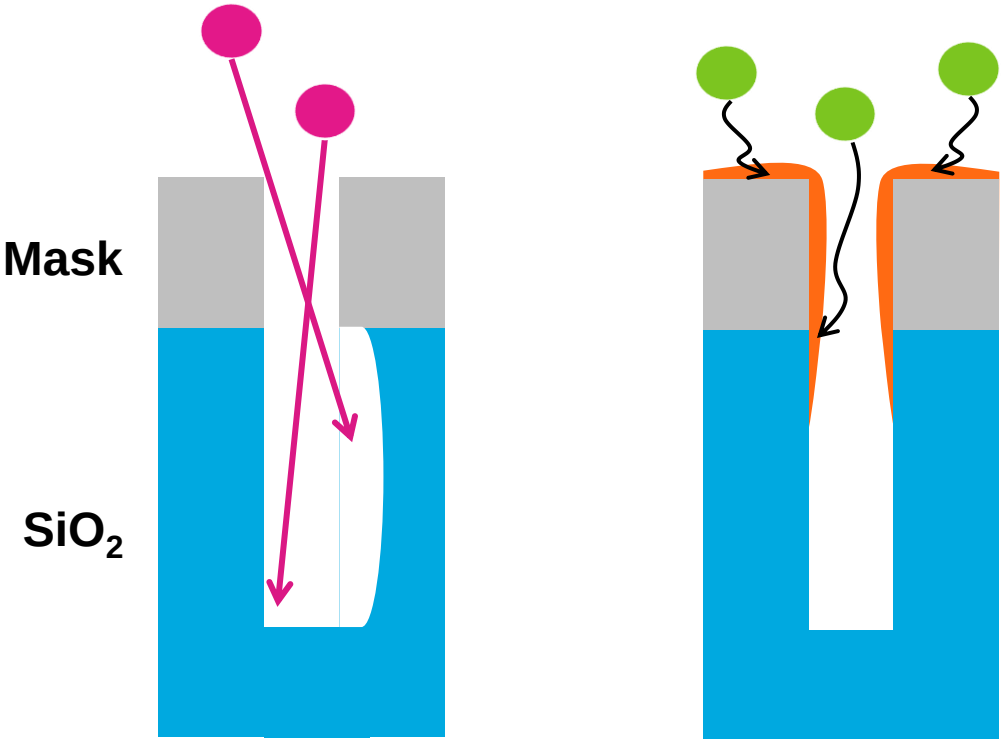
Device trend	Stacking	Scaling/new structure	Scaling/new structure
Technology Required	Fast and vertical high aspect ratio etch Depth monitoring and process control Within wafer uniformity control	Small CD*3, high aspect ratio capacitor etch Scaled mask etch (EUV, multi patterning) HBM (increase in interconnect, etc.)	High selectivity through precise ion control Low-damage process Profile control (vertical, etc.)

Etch technology with precise controllability is required for further evolution of devices

Overview of Etching and Key Parameters



Key Parameters for Etch Controllability



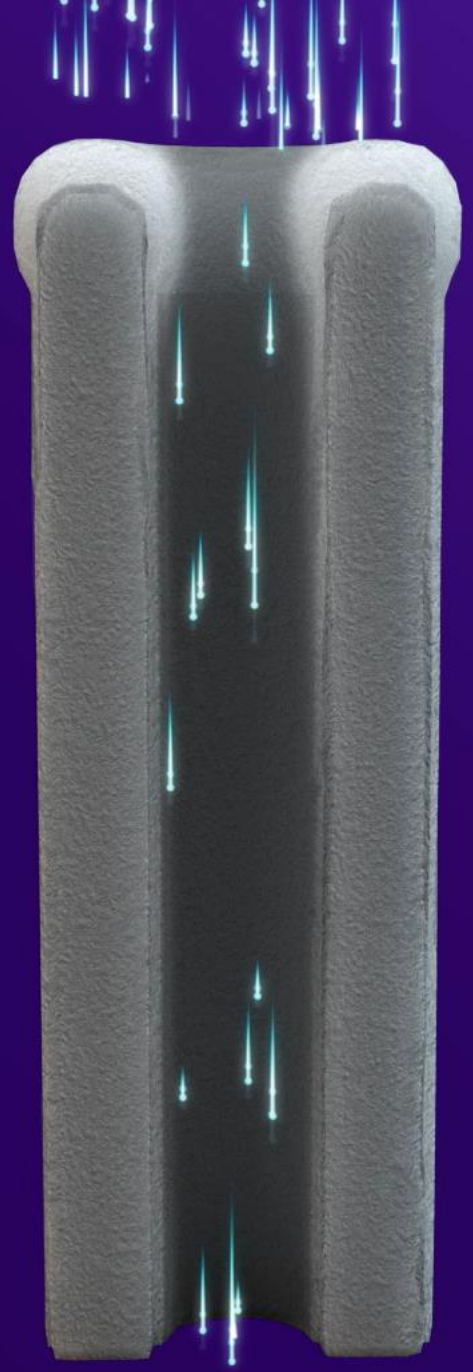
- Ion energy
- Ion incident angle

- Gas species
- Wafer temperature

Video

Clog — Bow

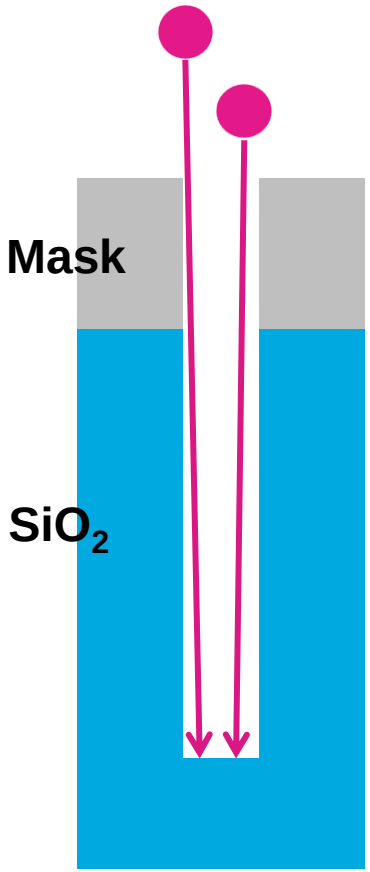
Risk Trade Off



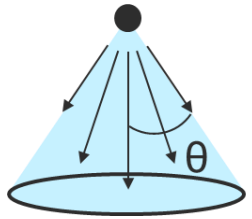
Our Unique Technology 1: HERB™

(HERB™: High Efficiency Rectangular Bias™)

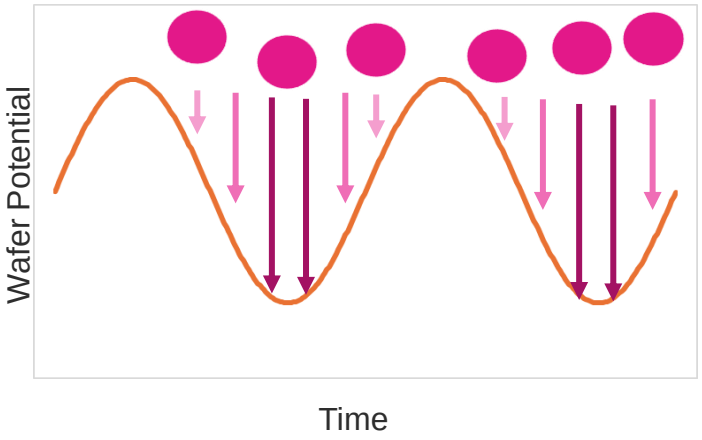
Ion transportation



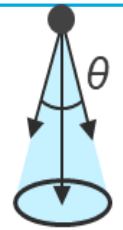
Conventional Technology (Sine wave)



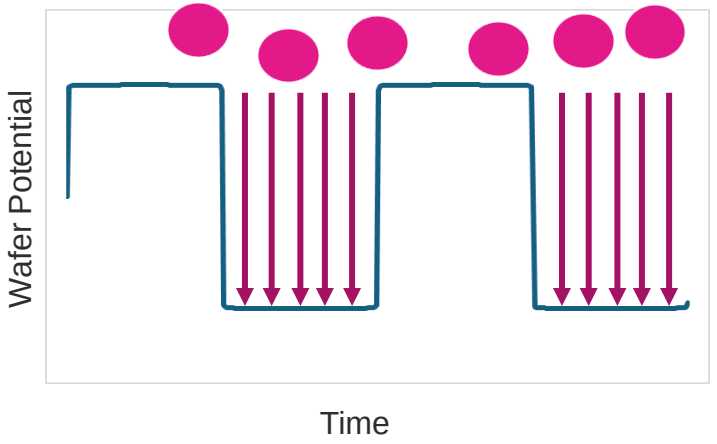
The force attracting ions varies
→incident angle varies



Novel Technology (HERB™)



Force attracting ions are strong and consistent
→incidence angle becomes perpendicular



Video

HERB™

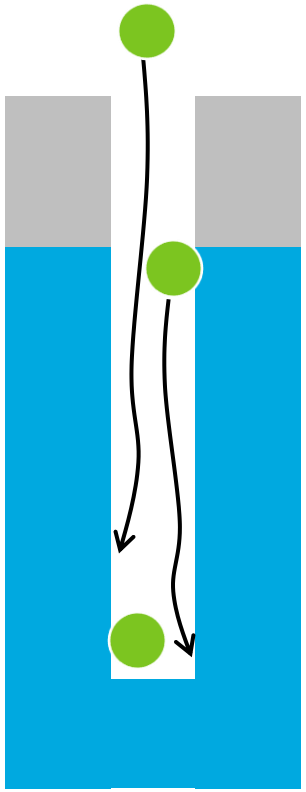
Vertical

Deeper

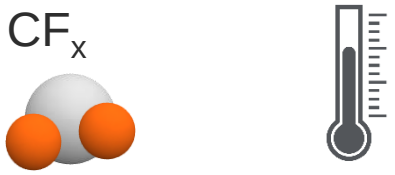
Ion Angle

Our Unique Technology 2: PHastIE™

Radical transportation

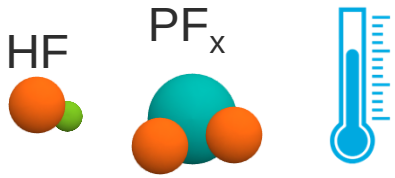


Conventional Technology (CF$_x$ + room temp.)



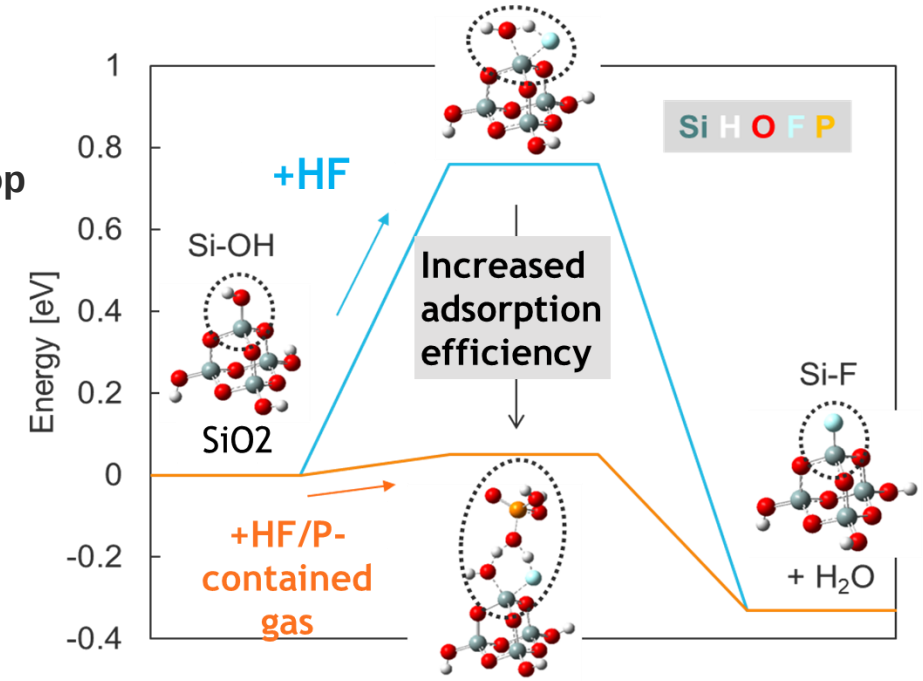
CFx tends to polymerize/adsorb easily
Hinders transportation when accumulated at top

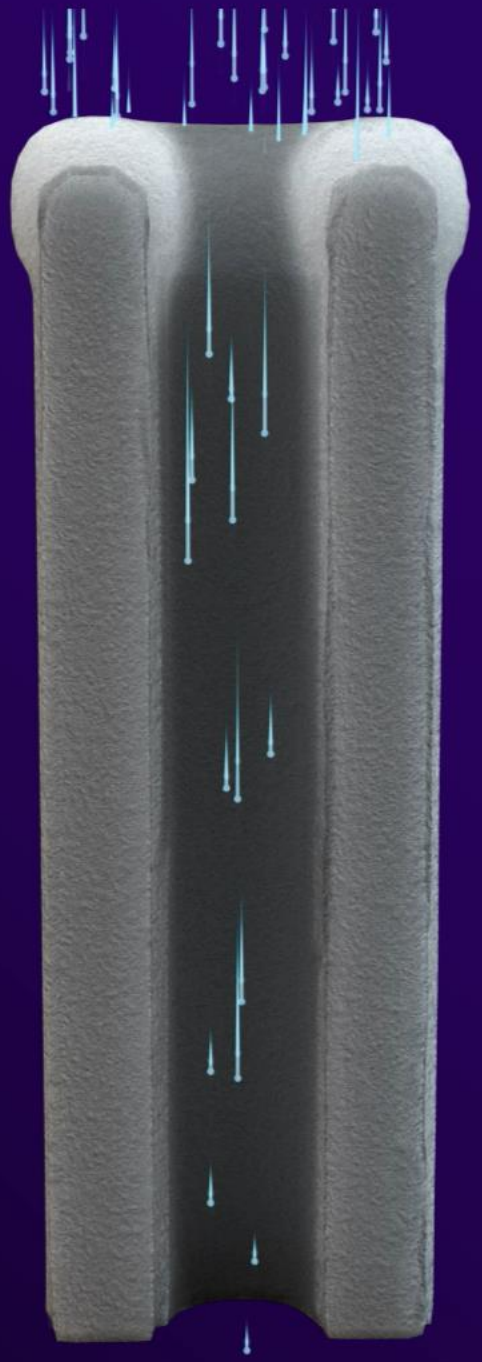
Novel Technology (PHastIE™)



Resolved the issue with novel gas
Achieved high etch rate in combination with low temp.

(PHastIE™: Phosphorus + Hydrogen based “Fast” Ion Etch™)





PHastIE™

Video

Less Deposition
by **New Chemistry**

Sidewall Protection
by **Cryogenic Temp Control**

Higher Etch Rate
by **New Chemical Reaction**

TELAVES™ for Novel Cryogenic HARC Etch

Beyond

10μm

2.5x

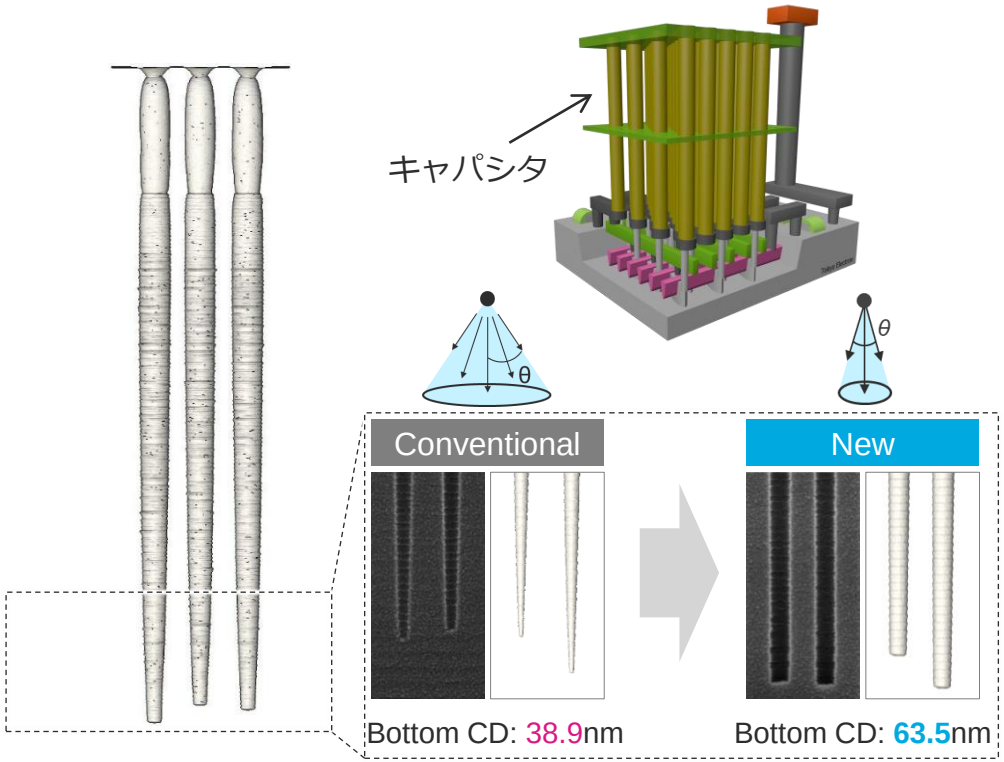
Faster

Process	Environment
Cryogenic temp.	**Power Consumption**
More Linear, Deeper & Faster	Less Power **-43%**
Plasma Control	**CO_2e** **-83%**
Deep-learning Optimization	Less Carbon Footprint

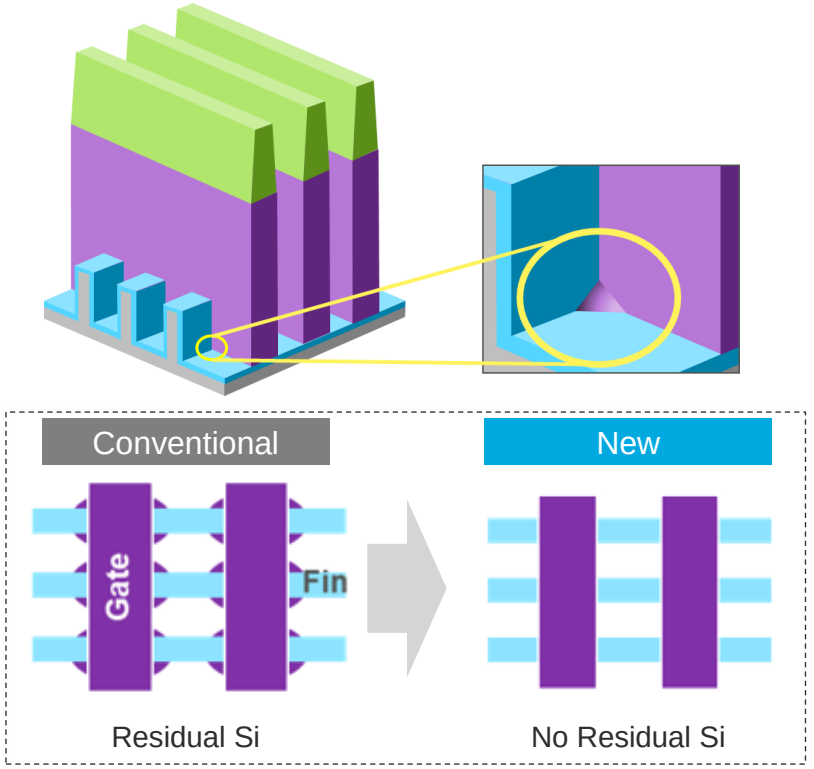
Presented world's first new cryogenic process in 2023 (@VLSI 2023), achieving both high process and environmental performance

Future of New Etch Technologies

DRAM: Capacitor SiO_2 Etch



Logic: Gate Silicon Etch

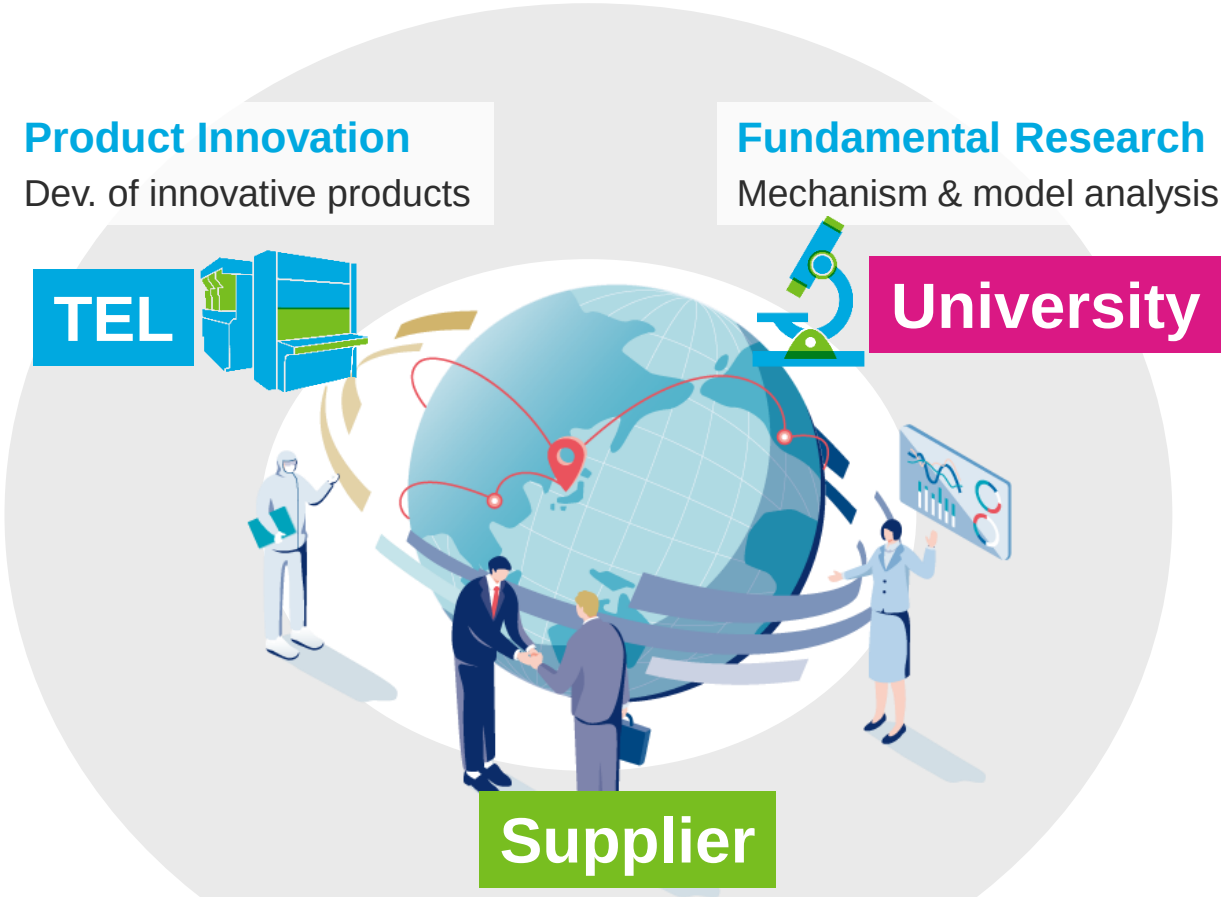


New technologies created through the development of ideal etching process development, will be applied to a variety of critical processes

Development Eco System for Further Growth

Product Innovation
Dev. of innovative products

Fundamental Research
Mechanism & model analysis



Supplier Collaboration
“Collaboration & Co-creation” with suppliers

- Continuously creating industry-first technologies through a **development ecosystem involving suppliers, universities and TEL**
- The development of sustainable solutions through this ecosystem is the source of our competitive advantage
- The **Miyagi Technology Innovation Center** in TEL Miyagi plays a key role

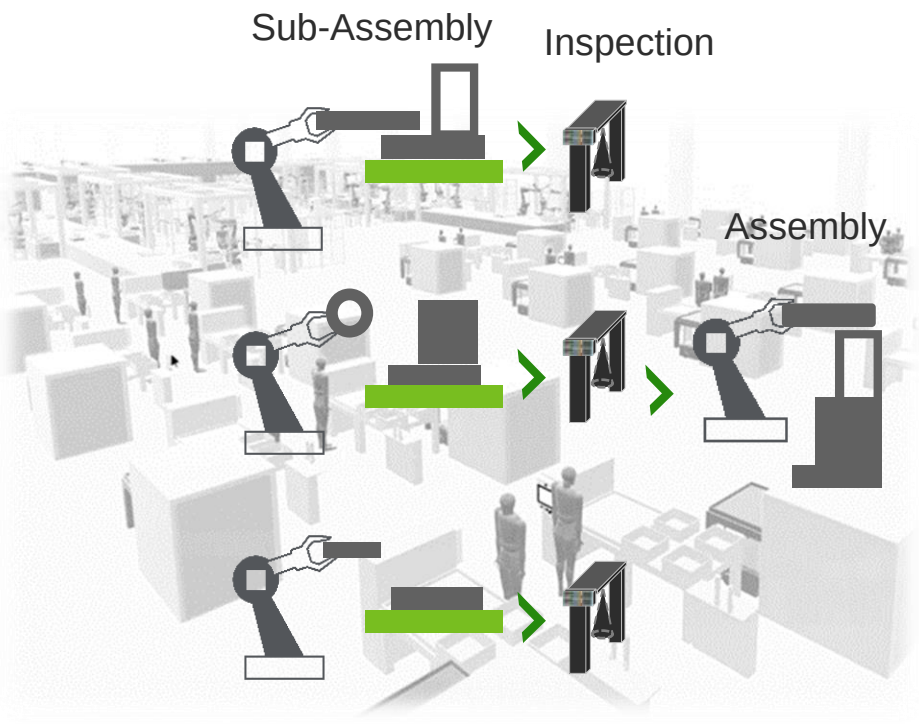
Smart Manufacturing to Achieve High Quality and Productivity

Development & Design

Feed Forward

Feedback

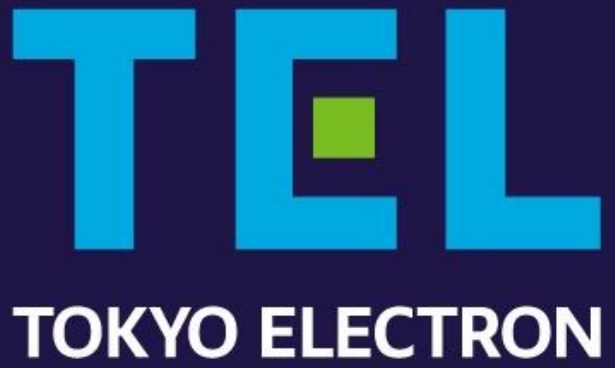
Smart Manufacturing



By centralizing development and production in TEL Miyagi,
we ensure continuous concurrent engineering and advanced manufacturing capabilities

Our mission:

To continue developing supreme etching technology
that exceeds our customers' imaginations,
and to continue to deliver it in a timely manner.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Business Strategy in Thin Film Deposition

February 26, 2025

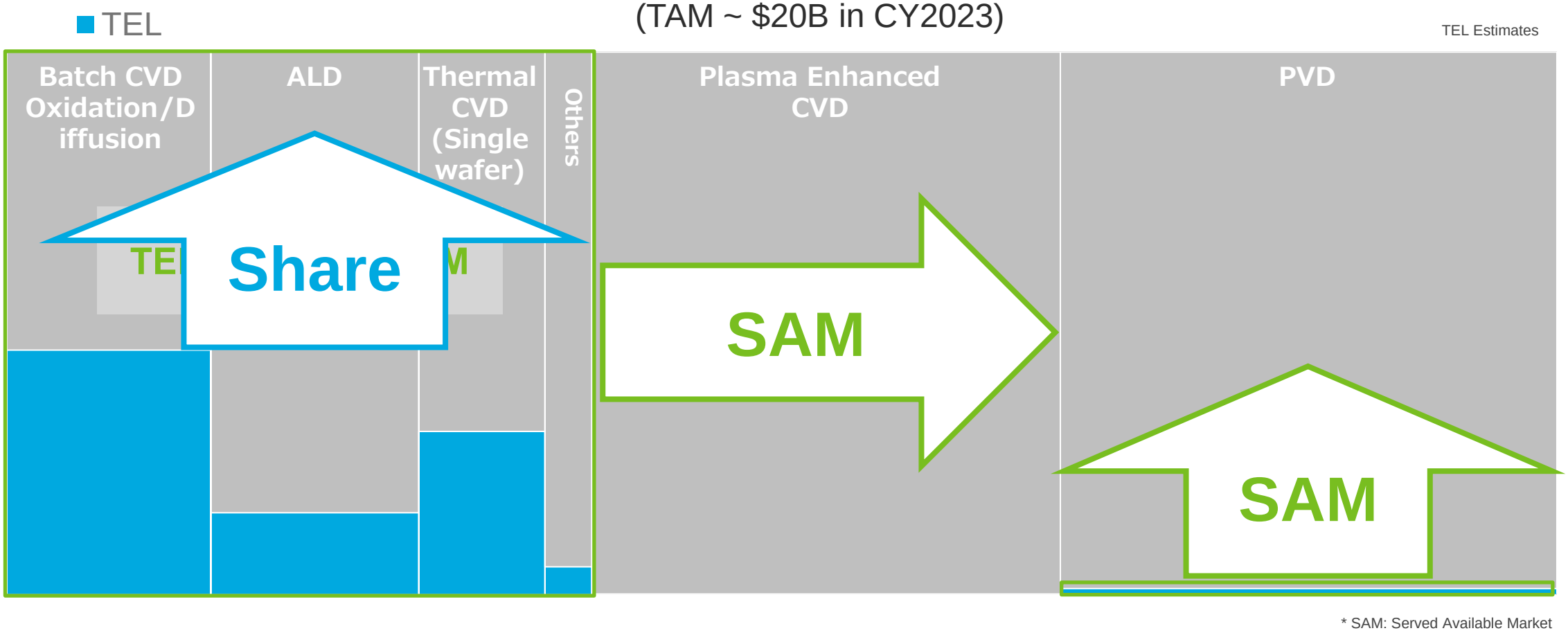
Shigeki Nakatani
TFF BU
VP&GM

Business Strategy in the Thin Film Deposition Market

Expanding Market Share and SAM*

TEL's Market Share and SAM in Thin Film Deposition

(TAM ~ $20B in CY2023)



* SAM: Served Available Market

Strategies in the Film Formation Business 1:
Expand SAM Using Single Wafer Deposition Equipment

Triase+™

Single Reactor
Existing Platform

Episode™ 1

Single Reactor
Equipped with up to eight process modules

Episode™ 2 DMR*

***Duo Matched Reactor**
Achieved high productivity
by processing 2 wfs/PM

Released in July 2024

Episode™ 2 QMR**

****Quad Matched Reactor**
Equipped with a newly developed
high-density plasma source

Scheduled for release in 2026

Video

Strategies in the Film Formation Business 1:

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Episode™ 2 QMR**

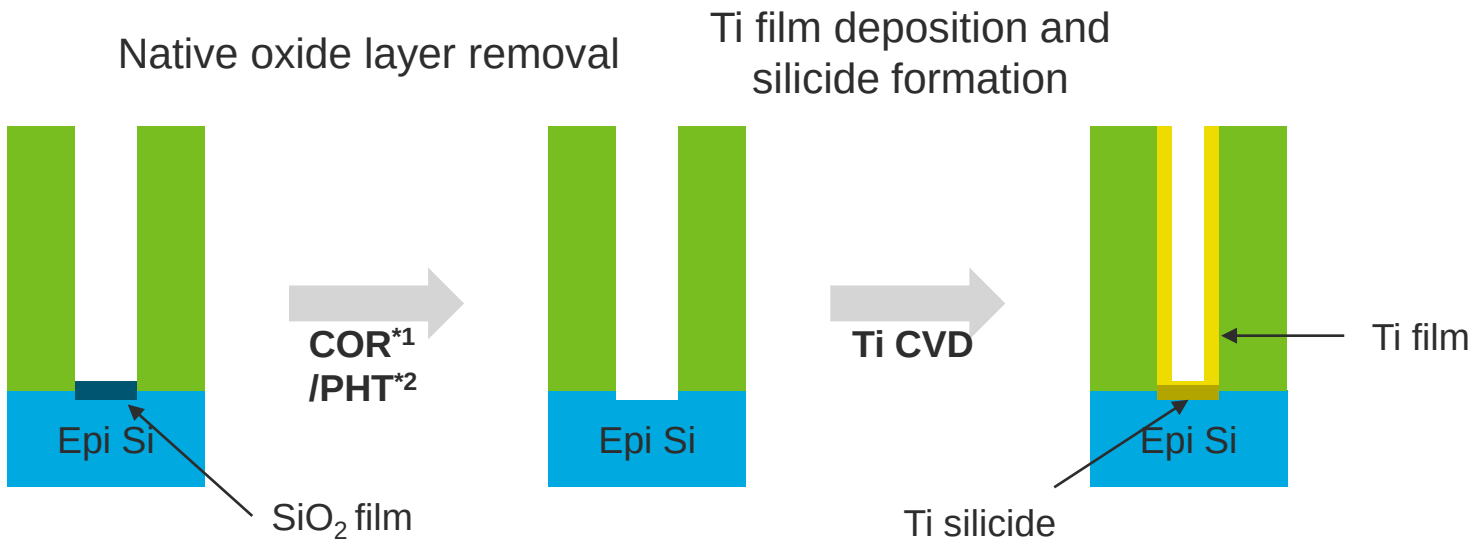
****Quad Matched Reactor**

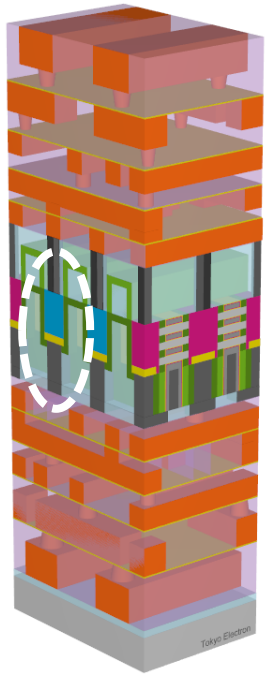
Equipped with a newly developed
high-density plasma source

Scheduled for release in 2026

Episode™ 1: Contact Formation Process

- Example of process flow



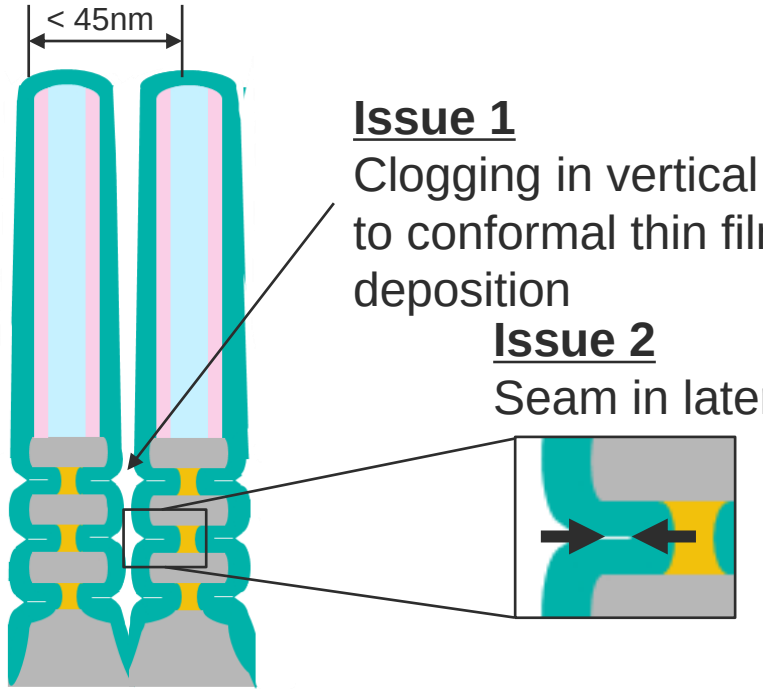


*1 COR: Chemical Oxide Removal
*2 PHT: Post Heat Treatment

Multiple types of process modules are equipped on a high-vacuum transfer module, and low-resistance contacts are achieved by sequentially processing native oxide layer removal and metal film formation

Episode™ 1: Inner Spacer Formation - Lateral Gapfill

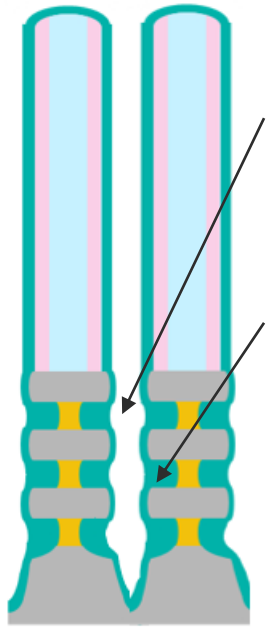
- Issues :
  Leak due to dielectric breakdown due to etching



Issue 1
Clogging in vertical gap due to conformal thin film deposition

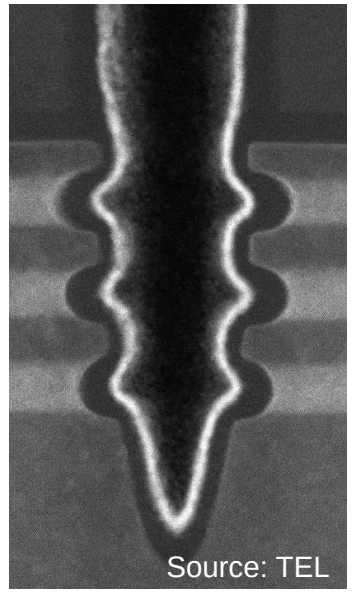
Issue 2
Seam in lateral gap

- Solutions :
  Improve lateral gapfill performance



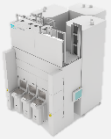
Solution 1
Thinner film deposition on the side walls

Solution 2
Seamless gapfill in lateral gap



Realized seamless lateral gapfill using a unique thin film deposition technique and laterally uniform film modification using a newly developed high-density plasma

Episode™ 2: Performance Comparison

		Triase+™ 	Episode™ 2 DMR 
Productivity and Footprint	Productivity per system	1 4PM/4-reactor	1.5 3PM/6-reactor
	Footprint	1	0.65
	Productivity per unit area	1	2.31
	Throughput	1	~ 1.8
Operation	Process knobs	✓	✓
	Construction cost for facilities	1	0.64*
Application	Legacy to leading-edge nodes	✓	✓
	New features for cutting-edge devices	N/A	✓
Smart Function	Data logger	N/A	✓
	Intelligent controller	N/A	
Environmental Performance	Power consumption per wafer	1	0.75

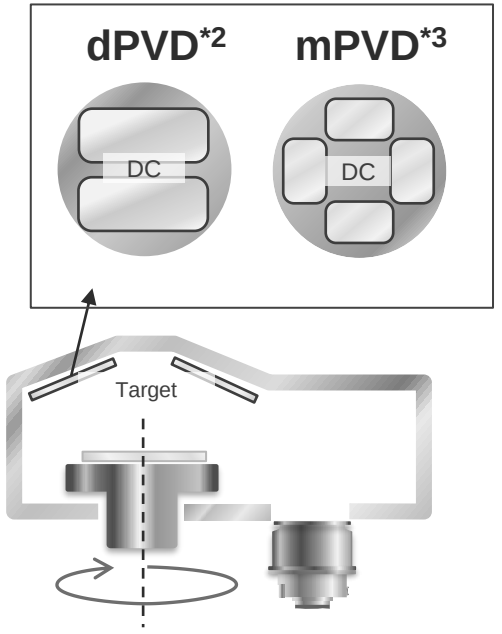
*TEL Estimates

Strategies in the Film Formation Business 2:

SAM Expansion with PVD

LEXIA™ -EX **Released in December 2024**

- Oblique angle sputter with wafer rotation system
  - Excellent thickness uniformity (1σ 0.5%)
- Unique multi-cathode*1 configuration
  - High deposition rate
  - Capability of tuning film composition ratio with multiple materials
- High throughput (~100WPH)
- Significant footprint reduction vs conventional model



*1 Cathode: An electrode for material deposition
*2 dPVD: Dual cathode PVD
*3 mPVD: Multiple cathode PVD

Strategies in the Film Formation:

Growth in Batch Thermal Process/Deposition

- Major applications
  - Silicon process in general (dummy gate, channel Si, etc.)
  - Batch ALD high-k (capacitor dielectric)
  - Plasma/Thermal ALD-SiN/SiO_2
  - Batch molybdenum (word line)

- Development plans
  - Increase load port size (8 lots, 200 wafers/batch)
  - Improve exhaust conductance to mitigate pattern loading effect
  - Enhance energy efficiency (elevate heater performance)
  - Enhance labor reduction (one-touch start-up, self-maintenance, DX)

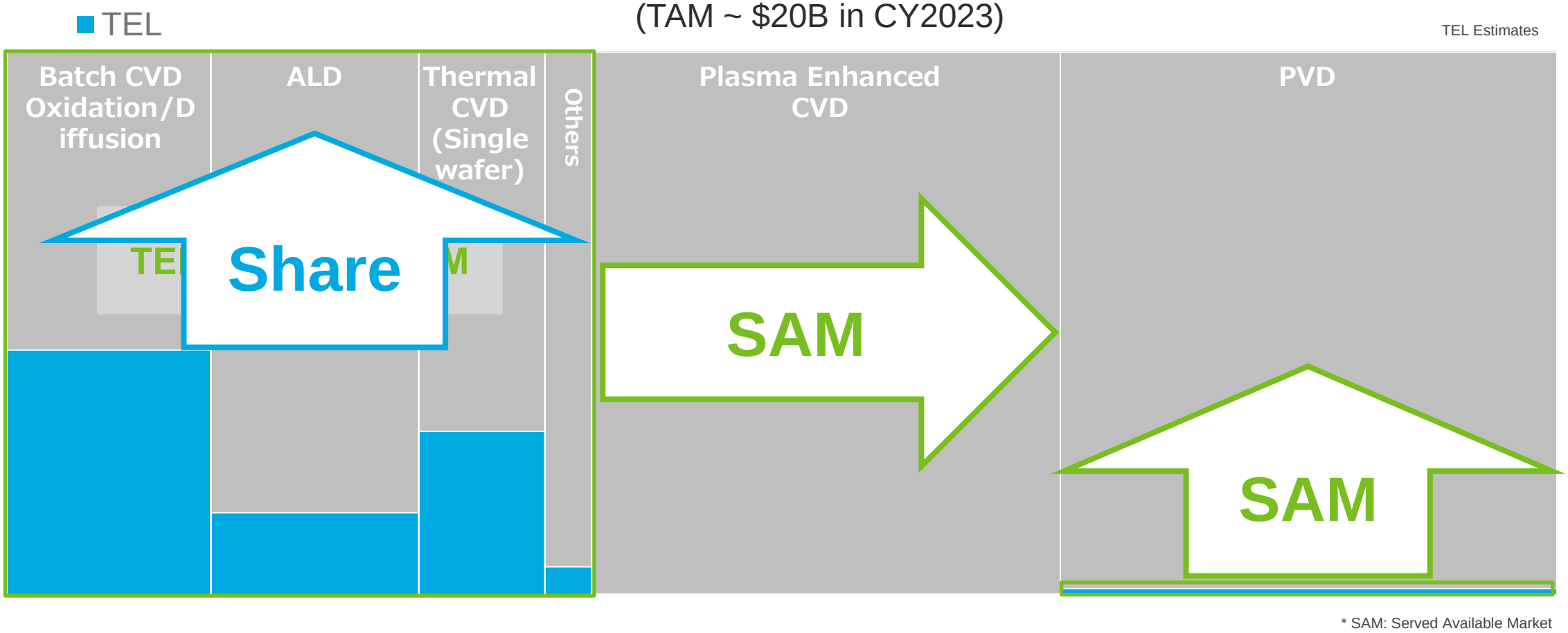
TELINDY™ PE-II

Business Strategy in the Thin Film Deposition Market

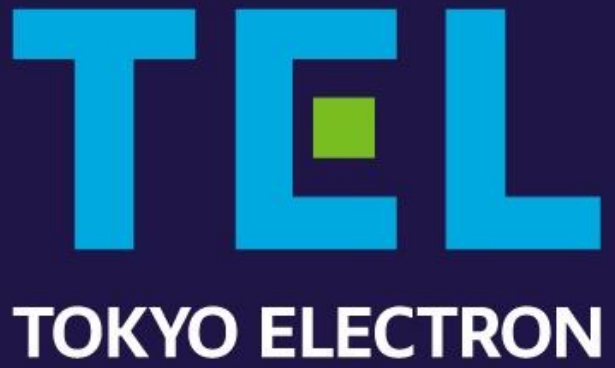
Expanding Market Share and SAM*

TEL's Market Share and SAM in Thin Film Deposition

(TAM ~ $20B in CY2023)



* SAM: Served Available Market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Diverse Systems and Solutions

February 26, 2025

Hiroshi (Kan) Ishida
DSS BU
VP & GM

Video

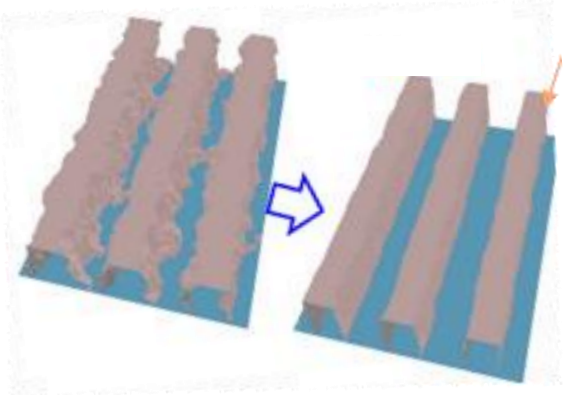
Acrevia™

TEL Original Gas Cluster Beam (GCB) System

- Beam Angle is freely Adjustable
- LSP（Location Specific Processing）Wafer Scan
  → Enable 3Dimetional Etching

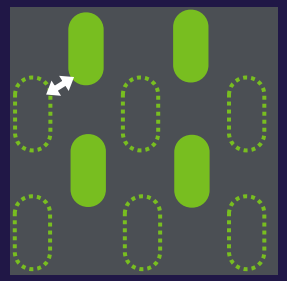
✓ Drastically Improve EUV productivity
by EUV step reduction with fine patterning

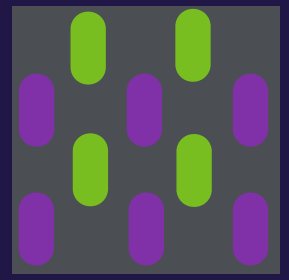
✓ Realize yield by removing defect between pattern and improving LER/LWR*

Before  After

* LER/LWR: Line Edge Roughness / Line Width Roughness

Too Narrow





1st EUV

Etch

2nd EUV

TEL Manufacturing and Engineering of America, Inc.

- Gas Cluster Beam (leading-edge patterning)
- Low-damage physical cleaning (HBM, advanced packaging, etc.)
- Development of unique products for leading-edge processes

Manufacturing: Chaska, MN

R&D: Chelmsford, MA

Metaverse

Autonomous Mobility

Green Energy

IoT & Information

Communications

Power Device (Si / SiC / GaN)

Waveguide

µLED

Si Photonics

CIS

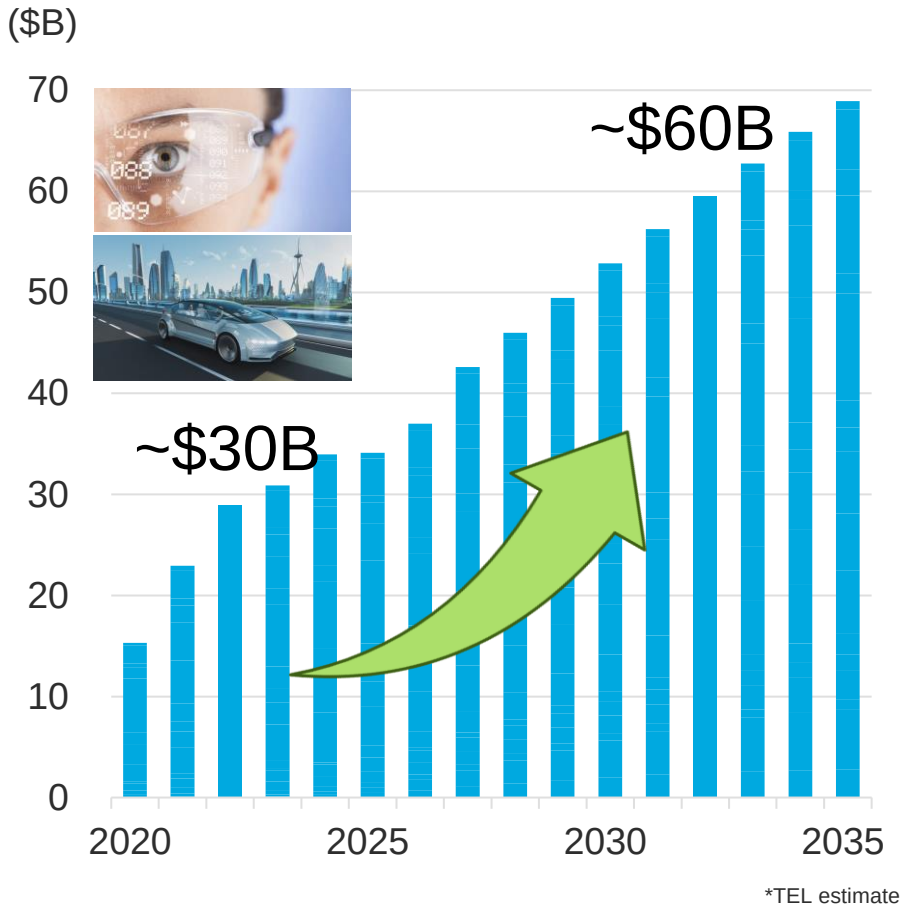
Displays

RF

MAGIC Market

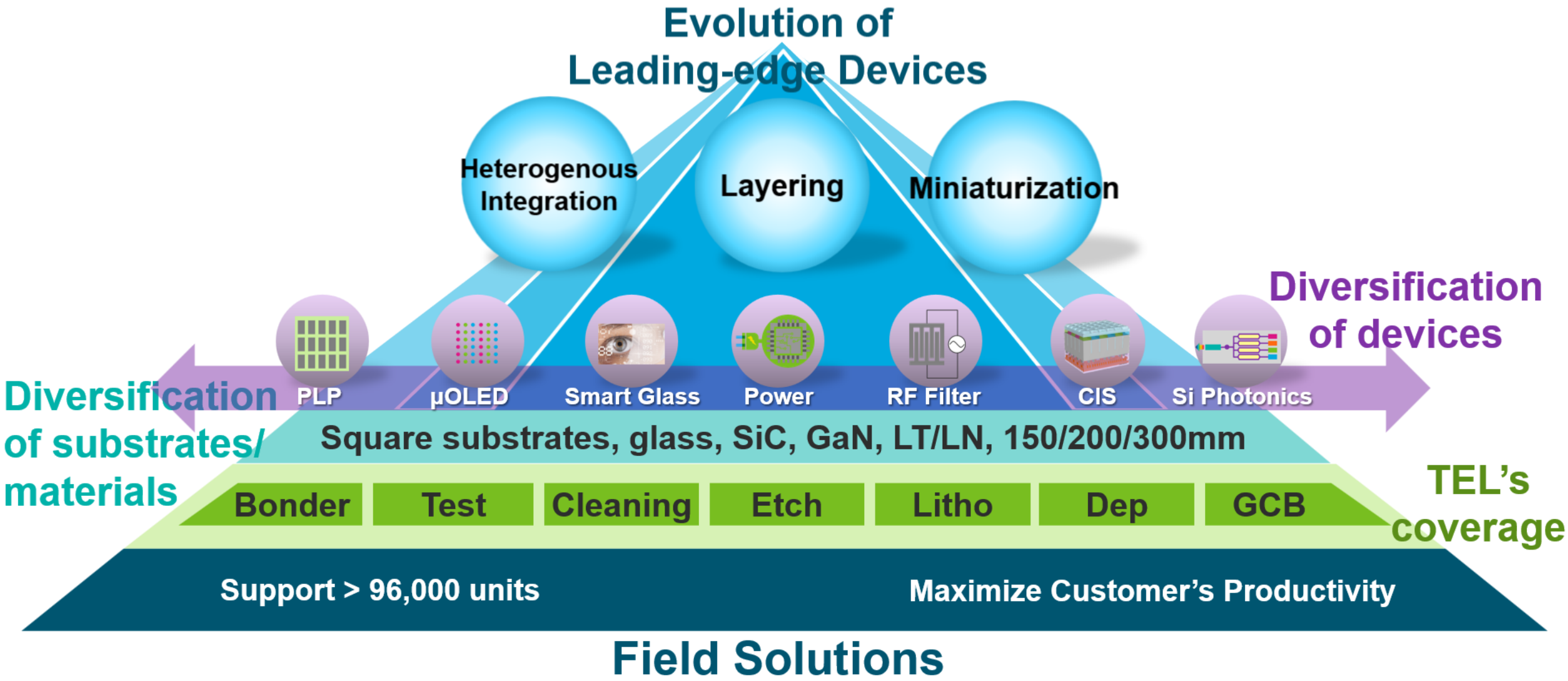
- MAGIC Market to double
- Development & sales for MAGIC specialty applications
- Demo line ready for 200mm MAGIC
  - ✓ Yamanashi, Kumamoto, Miyagi
  - ✓ Massachusetts, Minnesota, Florida

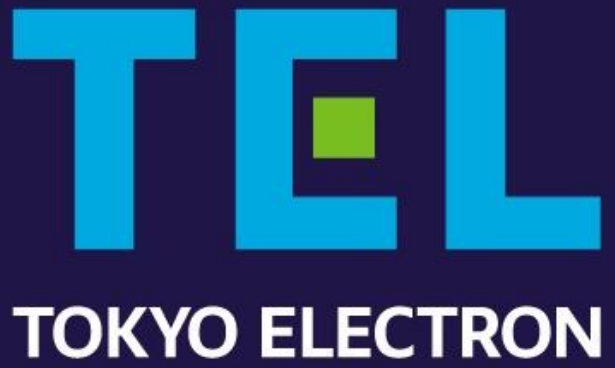
- Market Estimates



*TEL estimate

Providing Diverse Systems and Solutions for Diverse Needs

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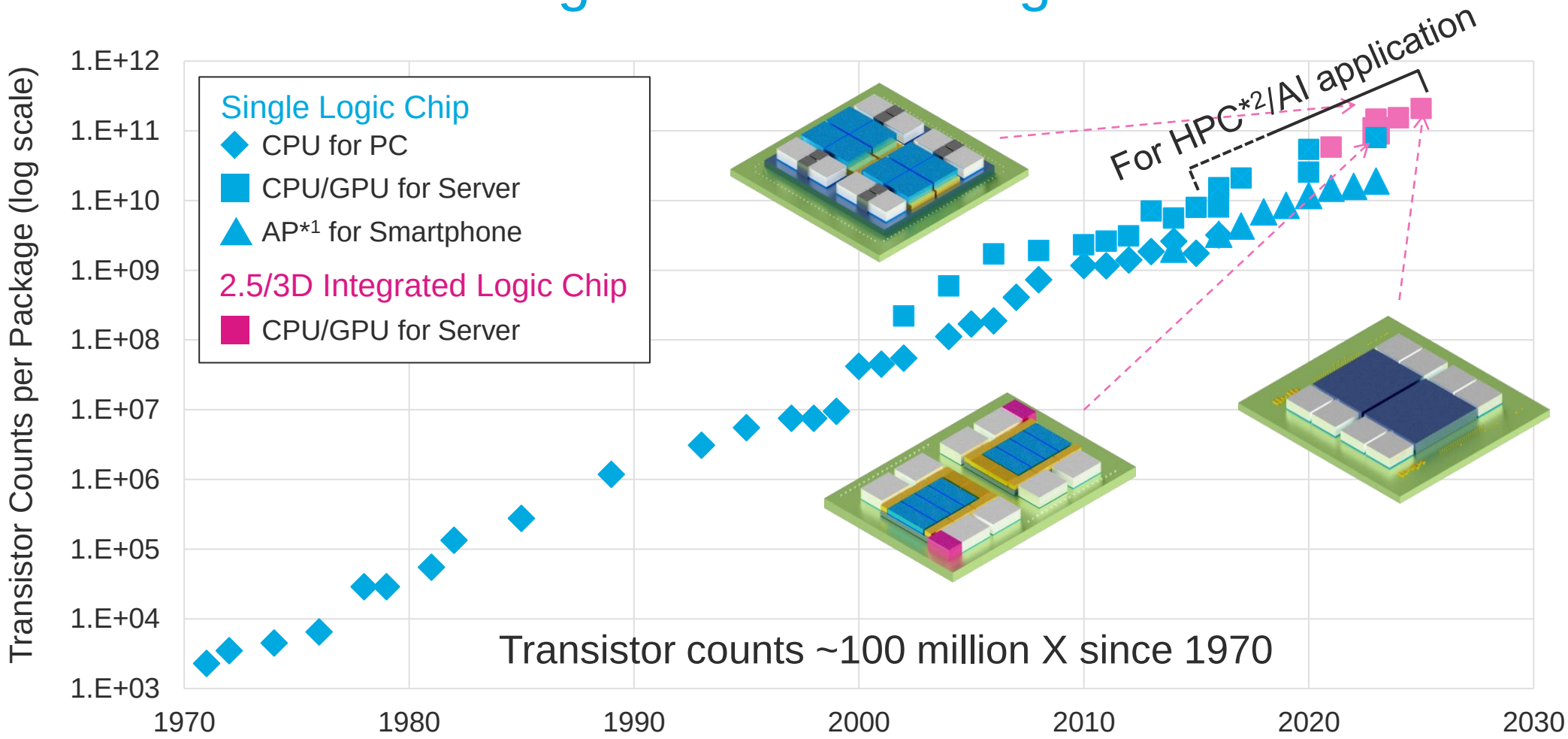
Technology Trends and Business Opportunities in Assembly Processes

February 26, 2025

Keiichi Akiyama
Division Officer, Backend Process Business Division
SVP&GM

Transistor Counts in Logic Device Packages



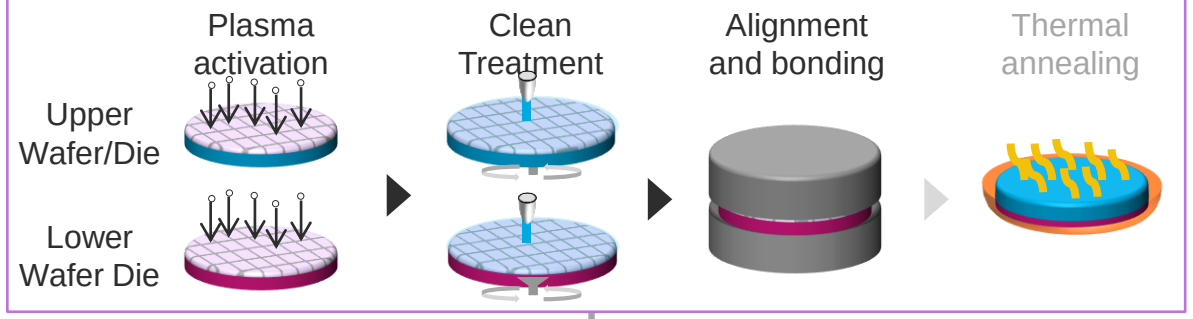
Source : Wikipedia
*1 AP : Application Processor
*2 HPC : High Performance Computing

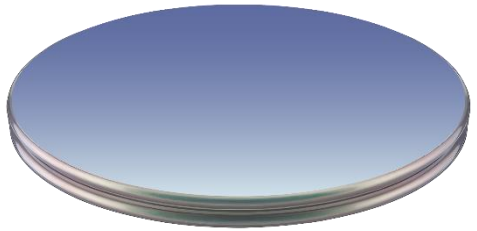
Transistor counts in HPC/AI, alongside node scaling and advanced packaging, are leading the way

*1 AP : Application Processor
*2 HPC : High Performance Computing

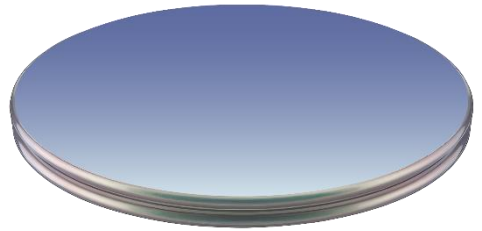
TEL's Opportunities for Bonding Technology

Bonding Technology

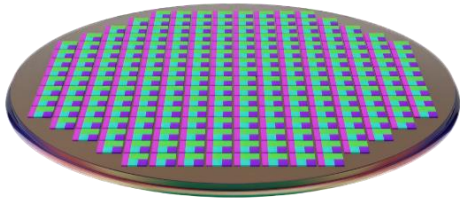




Wafer-to-Wafer Bonding



Wafer-to-Wafer Bonding



Die-to-Wafer Bonding

Benefits for Pitch scaling & Higher speed / Lower power consumption

Frontend Process

Advanced Packaging

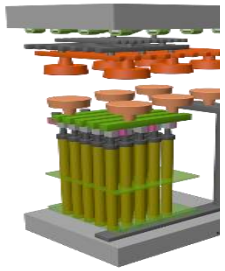
3DI / Test Business Expands Opportunities for HPC/AI Device

Frontend Process

Device Manufacturing

BSPDN*1

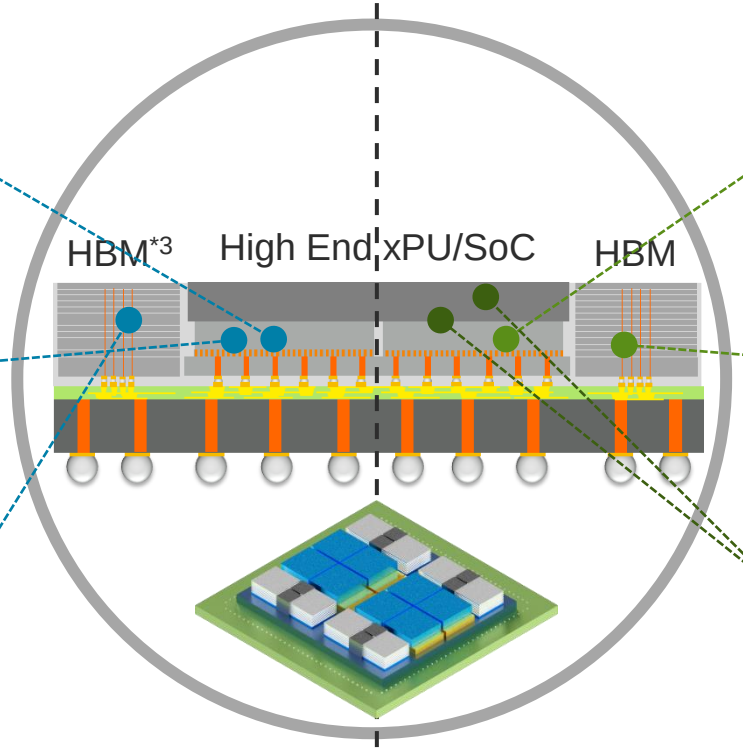
CFET*2



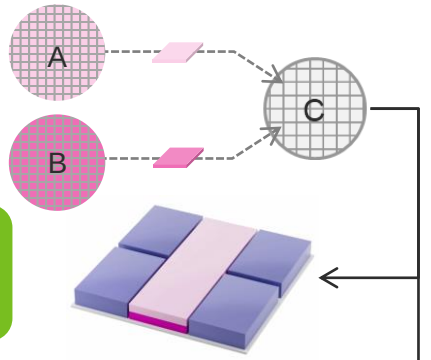
DRAM

Advanced Packaging

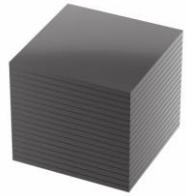
Assembly after Dicing/Singulation



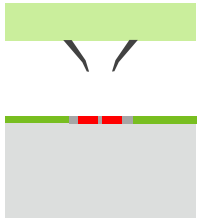
3DIC



Stack Memory



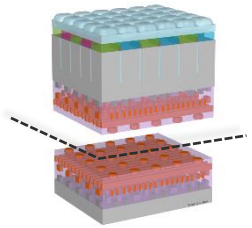
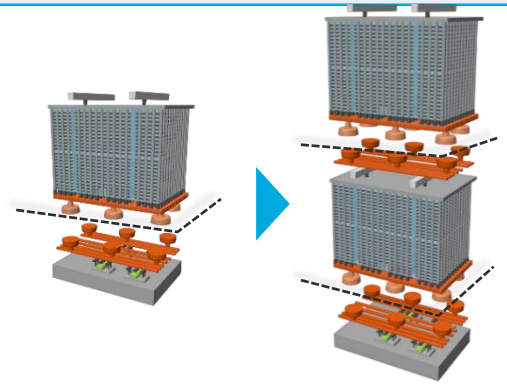
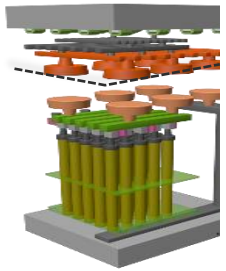
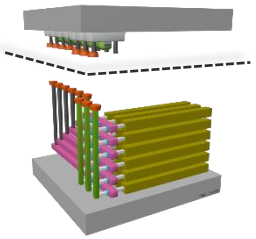
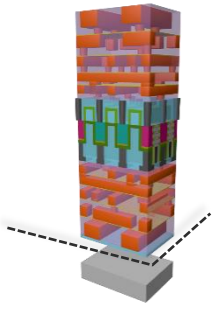
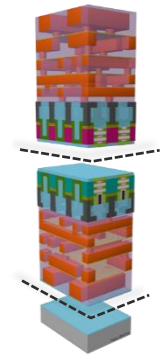
Die Test for KGD*4



*1 BSPDN: Back Side Power Delivery Network
*2 CFET: Complementary Field Effect Transistor
*3 HBM: High Bandwidth Memory
*4 KGD: Known Good Die

Frontend Process : Wafer-to-Wafer Bonding

Broad Applications and Expansion of Bonding Technology

Application	Frontend Process					
	CIS[*1]	NAND		DRAM		Logic
Stacking Device	BSI[*2] Pixel + (Peripheral) + Logic	3D NAND Cell + Peripheral	: + Cell + Cell + Peripheral	VCT[*5] DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	3D DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	BSPDN Logic + Si Substrate	BSPDN & CFET Logic + Logic + Si Substrate
Bonding	Wafer to Wafer (CHB[*3]/Fusion)	Wafer to Wafer (CHB)		Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)	
Structure							
Status	HVM[*4]	R&D~HVM	R&D	R&D	R&D	R&D~HVM	R&D

The design of future devices is transitioning from single bonding to multi-bonding structures

*1 CIS: CMOS Image Sensor
*2 BSI: Backside Illumination
*3 CHB: Cu Hybrid Bonding
*4 HVM: High Volume Manufacturing
*5 VCT: Vertical Channel Transistor

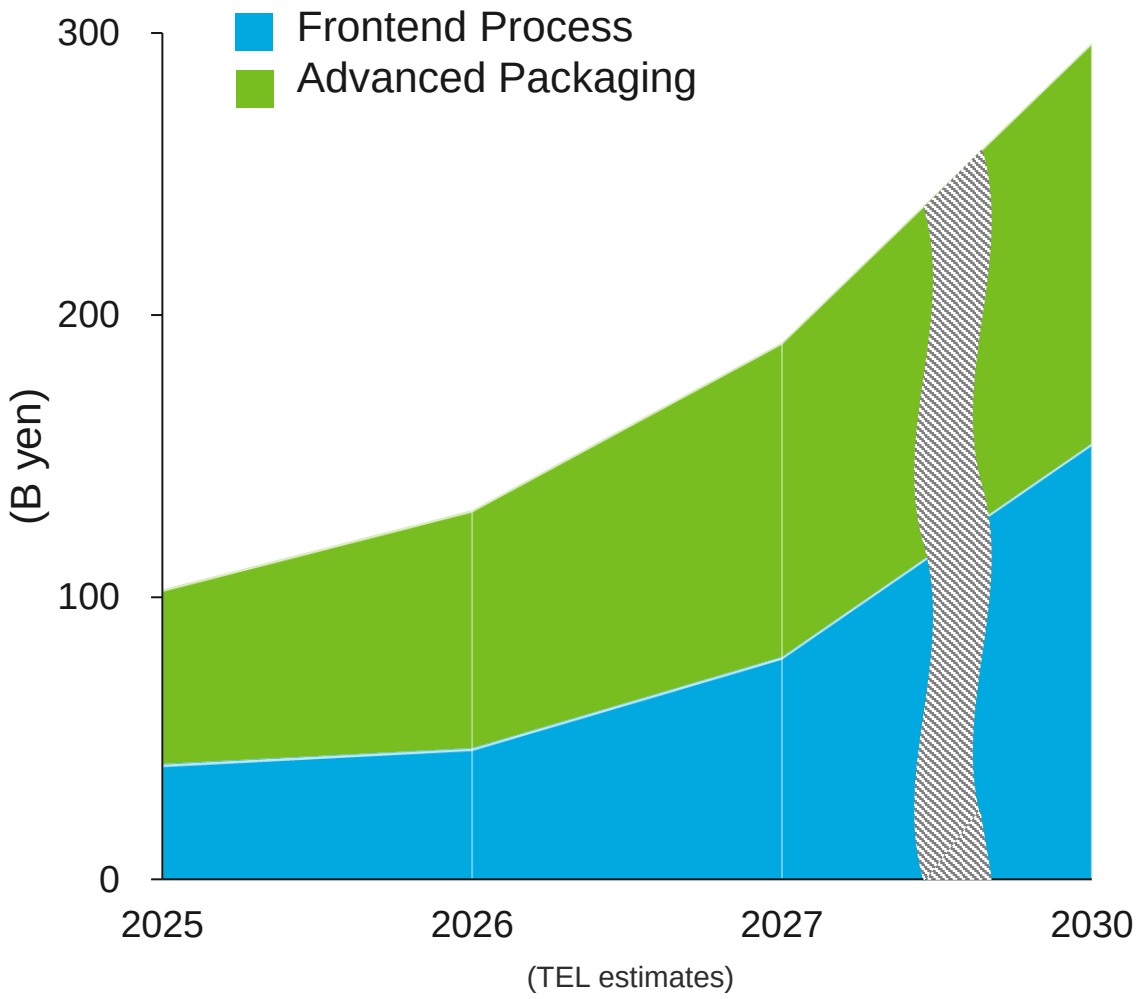
Advanced Packaging : Wafer-to-Wafer / Die-to-Wafer Bonding

Broad Applications and Expansion of Bonding Technology

Application	Advanced Package		
	Stack Memory / HBM	3DIC	
Stacking Device	DRAM Wafer ⋮ DRAM Wafer + DRAM Wafer + Logic Wafer OR DRAM (Die) ⋮ DRAM (Die) + DRAM (Die) + Logic Wafer	SoC Disaggregation Device A Wafer + Device AorB Wafer OR A, B, C, Die, Wafer	Heat Spreader Heat Spreader + Device
Bonding	Wafer to Wafer / Die to Wafer (CHB/Fusion)	Wafer to Wafer / Die to Wafer (CHB)	Wafer to Wafer (Fusion)
Structure	**Micro Bump** → ***Cu hybrid*** (More stacks) Change • Thinner die / more stacks • High density connection • Better thermal conductance Cu	**Monolithic SoC** → ***3D Stack IC*** SRAM, CPU/GPU, I/O&Peripheral Change • Small formfactor (3D stack vs. 2D) • Higher speed (shorter wiring, no bump) • Lower power (shorter wiring, no bump) • Lower cost (higher yields, easy to mix processes) • Shorter time to market (matured IP block reuse)	Heat Spreader • Better thermal conductance
Status	R&D	R&D ~ HVM	HVM

The opportunity for CHB/fusion bonding is growing to encompass advanced packaging

Bonding Process Equipment TAM*



Anticipating a TAM CAGR of 24% from CY2025 to CY2030

- Projected to achieve 300 billion yen by CY2030
- Encompassing both frontend processes and advanced packaging equipment
- Addressing bonding/debonding, slicing, and thinning process equipment utilizing various technologies

* TAM : Total Available Market

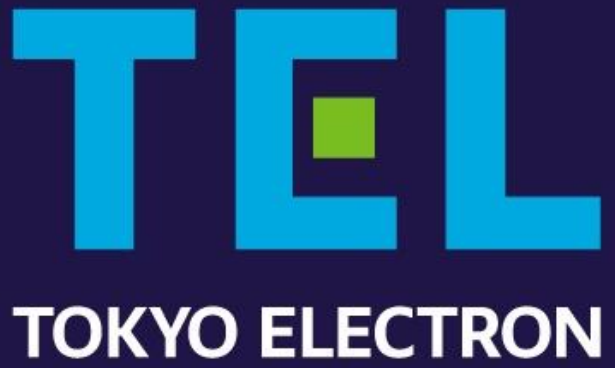
Today’s Message

- Bonding processes are at a critical inflection point for next-generation device manufacturing and advanced packaging, and further technological innovation is required to achieve this
- TEL has the advantage of covering all the technologies necessary to realize bonding technology under one roof, and has established a system to quickly respond to customer expectations
- Engagement with customers is progressing smoothly through our strategy, which places our R&D centers near the R&D bases of major customers
- We accelerate evaluation with customers’ devices towards mass production

TEL Technology Center, Korea

TEL Technology Center, America

Tokyo Electron Kyusyu Limited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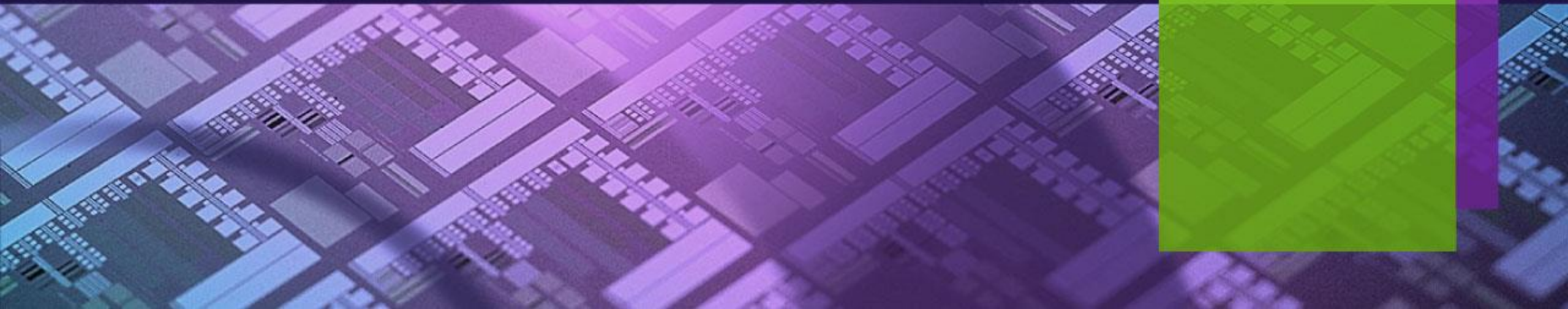
Product Strategy in Assembly Processes

February 26, 2025

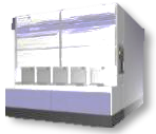
Yohei Sato
ATS BU
VP & GM



History of Product Launches in Assembly and Test* Systems

New Category Product　Next Generation/Improvement Product

Synapse™ S
Fusion bonder



Synapse™ V
Temporary bonder

Synapse™ Si
Cu hybrid / Fusion wafer bonder

Prexa™
Wafer Prober

Ulucus™ L
Laser Edge Trimmer

Synapse™ Si (high accuracy)
Cu hybrid / Fusion wafer bonder

Ulucus™ LX
Extreme Laser Lift Off

Die Test Prober
Upcoming system for release

Year | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026

Synapse™ Z plus
De-bonder

Synapse™ ZF
Post bond re-worker

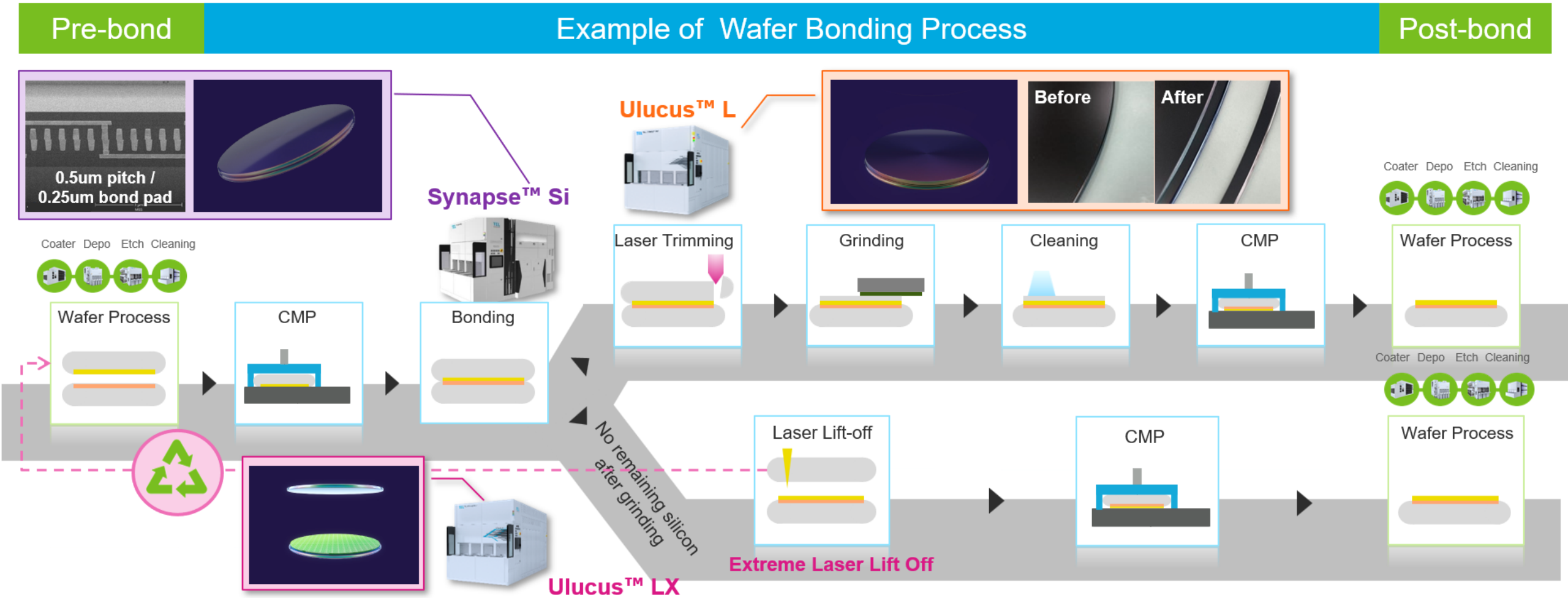
Ulucus™ G
Wafer Thinning

3DI
Upcoming system for release

Accelerating product development to prepare for the era of 3D integration

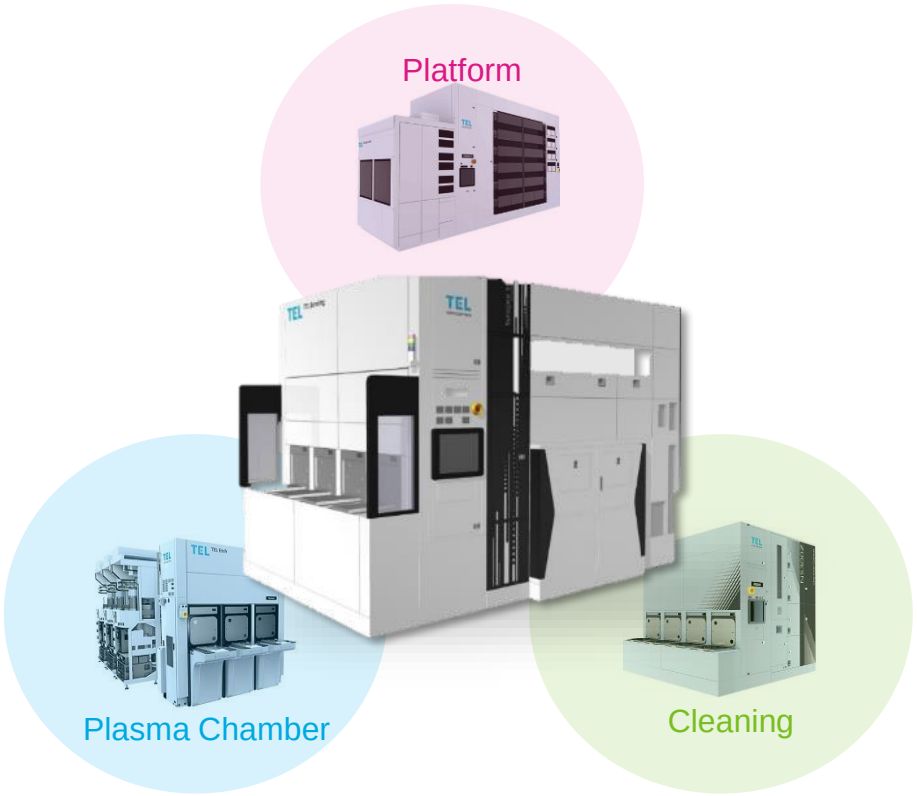
*Test : Prober for Advanced Packaging Test

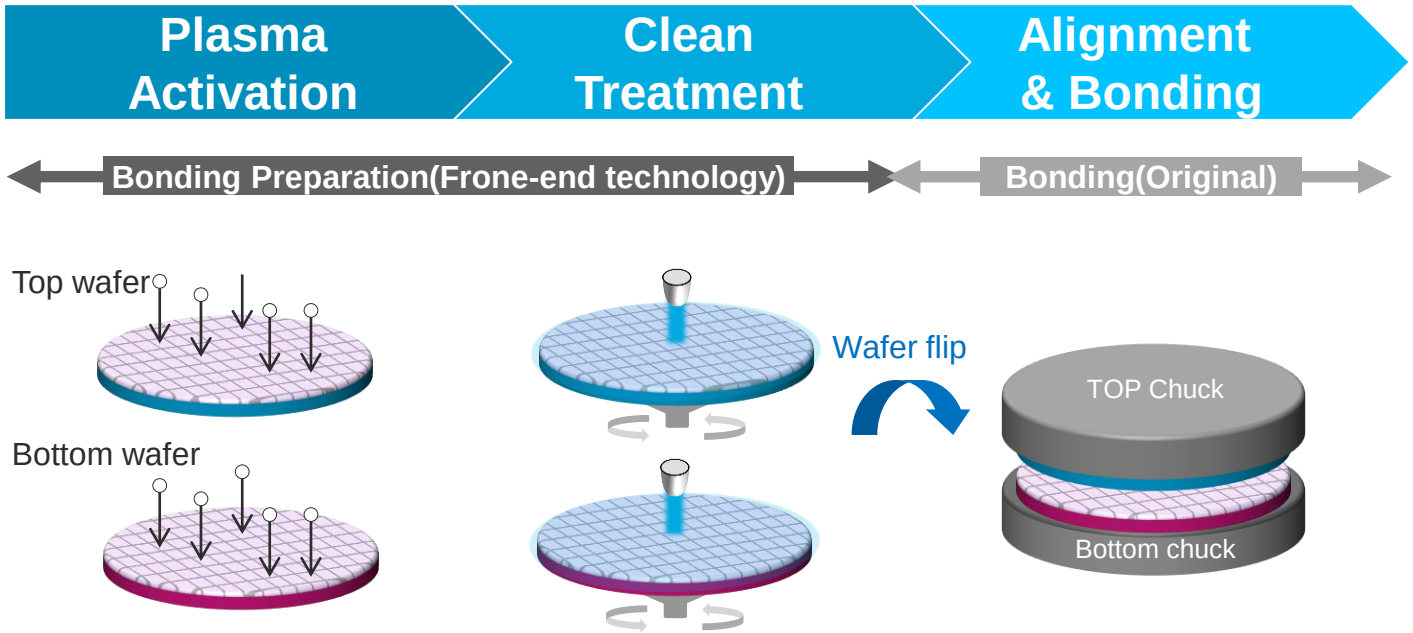
Frontend Wafer Bonding Process and TEL Products



Integrating various TEL equipment enables next generation wafer bonding processes that deliver high performance and process efficiency

Wafer-to-Wafer Permanent Bonder Synapse™ Si



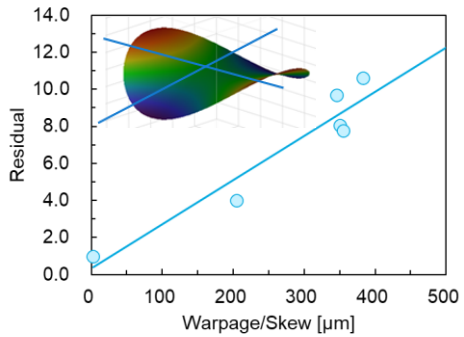


- TEL's existing broad technology and business contributing effective product development/CIPs
- Making good progress with major memory, logic customers towards high volume manufacturing
- Leading W2W Fusion/Cu hybrid bonding technology for next generation device manufacturing

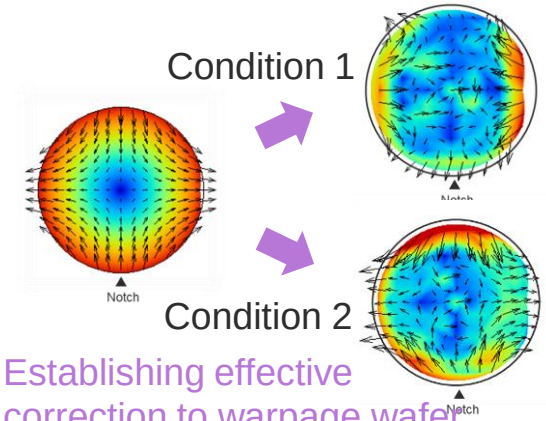
Wafer Bonder Technology Roadmap and Challenges

CY	2024	2025	2026	2027	2028	2029	2030	Beyond
Logic Node	2nm	2nm	2nm+	14A	14A	10A	7A	5A
Logic	Distortion ≤ 4nm （BSPDN）			Distortion ≤ 3nm （BSPDN）		Distortion ≤ 2nm （CFET）		
NAND	2-wafer-bonding				3-wafer-bonding		≥ 4-wafer-bonging	
NAND	Wafer warpage < 500μm				Wafer warpage > 500μm			
DRAM	2D DRAM			2D/3D DRAM				
DRAM	Distortion ≤ 5nm / DxDy ≤ 70nm			Distortion ≤ 3nm / DxDy < 50nm				

Wafer Warpage Challenges and Actions

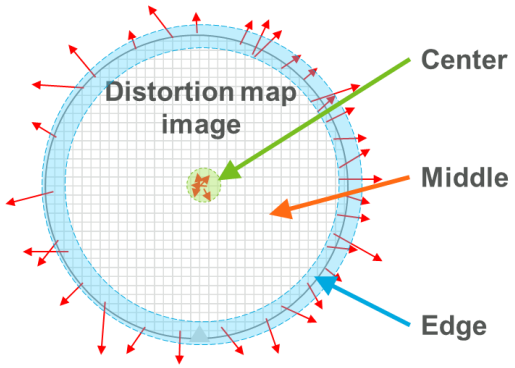


Relation between wafer warpage and residual (distortion)

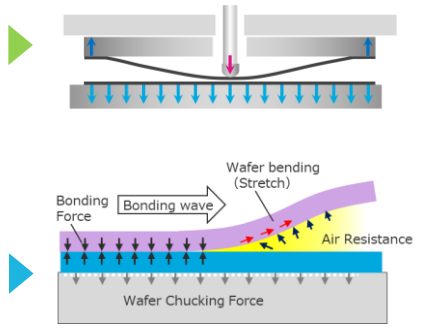


Establishing effective correction to warpage wafer

Distortion Challenges and Actions



Distortion vector



Optimizing hardware and process

TEL is developing various technologies in advance to prepare for next-generation devices

Introducing Ulucus™ LX for Post-Wafer Bonding Process

TEL

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News Room / Tokyo Electron Launches Ulucus™ LX, an Extreme Laser Lift Off System for 300mm Wafer-Bonded Devices

2024.12.09

Products / Services IR #Others

Tokyo Electron Launches Ulucus™ LX, an Extreme Laser Lift Off System for 300mm Wafer-Bonded Devices

Tokyo Electron (TEL; Head Office: Minato-ku, Tokyo; President: Toshiki Kawai) today announced the launch of Ulucus™ LX, an Extreme Laser Lift Off system for 300mm wafer-bonded devices.

With the advent of the AI era, the need to improve the performance and energy efficiency of semiconductor devices is more pressing than ever. As a result, 3D integration using permanent wafer bonding technology has become essential to the continued evolution of semiconductor devices. As a critical technology for high degrees of integration along with device scaling, permanent wafer bonding is increasingly in demand for the production of diverse semiconductor devices. These devices often require multiple bonding processes, making the technology hurdle even more challenging. Under these circumstances, the polishing and grinding steps to remove the unnecessary portion of silicon wafers requires a large amount of DI water during processing, and leads to reduced yield and a limitation on the number of available chips. Instead, an innovative technology is needed that contributes both to sustainability and productivity improvement.

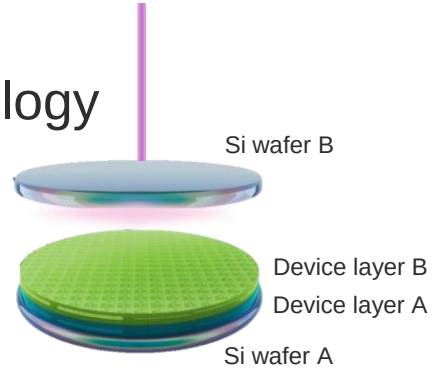
Ulucus™ LX is an innovative system designed to meet this need, featuring TEL's Extreme Laser Lift Off technology and capable of performing laser beam irradiation, wafer removal, and wafer cleaning in a single unit. The system integrates TEL's advanced laser control and wafer separation expertise, with the cleaning technologies cultivated in its single-wafer cleaning systems (NS and CELLESTA™ series) and the LITHIUS Pro™ Z Coater/Developer platform that has a large installed base.

Customers using this system will be able to replace multiple processes in permanent wafer bonding, including wafer backgrinding, polishing, and chemical etching, while reducing deionized water consumption by more than 90%.* By eliminating the need for conventional edge trimming, the system also increases the number of viable chips per wafer. In addition, TEL is developing the technology to reuse the excess silicon wafers removed by this system.

"In addition to scaling, the accelerating adoption of 3D high-density packaging is further evolution of semiconductor performance," said Yohei Sato, General Manager of ATS BU at TEL. "Wafer bonding is one of the most critical steps in 3D packaging. Of particular interest is the post-bonding wafer thinning process, where there are high expectations for a technological breakthrough. The newly released Ulucus™ LX system with Extreme Laser Lift Off technology is an innovative solution that helps improve productivity and reduce environmental impact. TEL will continue to develop and introduce advanced technologies and products that meet the needs of our customers."

https://www.tel.com/news/product/2024/20241209_001.html

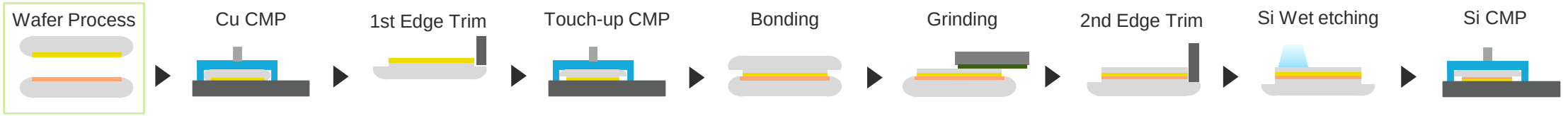
- **Equipment released in December 2024**
- **Incorporating extreme laser lift-off (XLO) technology**
  - Advanced thinning and critical technology for post-wafer bonding process
  - Unique laser technology enables separation of the Si-substrate from the device layer



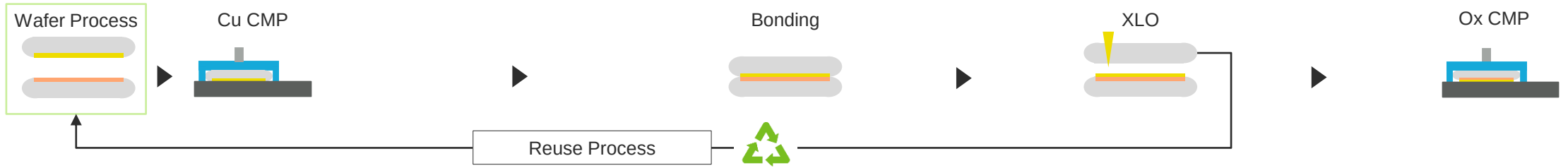
- **Advantages for process and environment**
  - Enhanced efficiency in silicon active areas
  - Fewer process steps required
  - Reduced need for DI water usage and CO_2 emission
  - Opportunity for wafer reuse

Ulucus™ LX Advantages

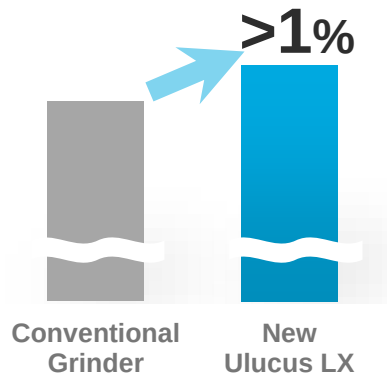
Permanent Bonding Process with Grinding & Blade Edge Trimming (Conventional)



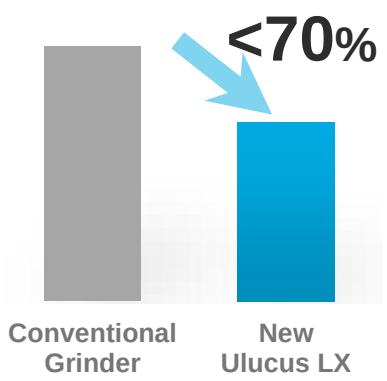
Permanent Bonding Process with XLO (Extreme Laser Lift Off)



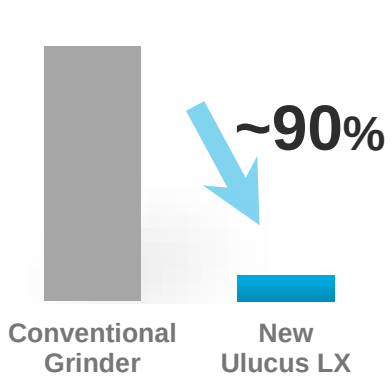
Active Silicon Area



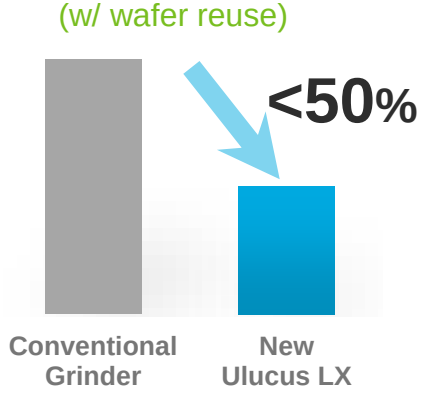
of Process Steps



DIW* Usage



CO_2 Emission
(w/ wafer reuse)



No Silicon Sludge
→ Advantage Over Grinder

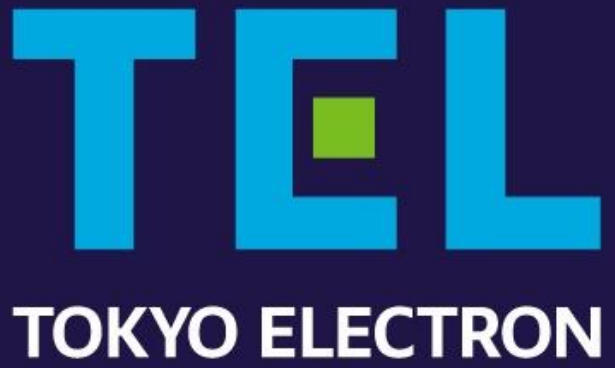
Source: TEL

* DIW : De-ionized Water

Video

Today’s Message

- TEL is accelerating the development of equipment for the bonding process, with the arrival of the 3D integration era.
- TEL is proactively developing fusion and Cu hybrid bonding technologies necessary for next-generation device manufacturing, leading the industry.
- TEL will further strengthen our engagement with key customers in memory and logic device manufacturing to expand the application of bonding technologies and achieve mass production implementation.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