Medium-term Management Plan Progress and New Financial Model

May 29, 2018

Toshiki Kawai
Representative Director, President & CEO
Forward Looking Statements

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  Forecast of TEL's performance and future prospects and other sort of information published are made based on information available at the time of publication. Actual performance and results may differ significantly from the forecast described here due to changes in various external and internal factors, including the economic situation, semiconductor/FPD market conditions, intensification of sales competition, safety and product quality management, and intellectual property-related risks.

- Processing of numbers
  For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.

- Exchange risk
  In principle, export sales of Tokyo Electron’s mainstay semiconductor and FPD production equipment are denominated in yen. While some settlements are denominated in dollars, exchange risk is hedged as forward exchange contracts are made individually at the time of booking. Accordingly, the effect of exchange rates on profits is negligible.

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FPD: Flat panel display
Today’s Key Messages

- Semiconductor production equipment market will continue to grow
  Approaching $60B+ phase

- Making good progress in business development in focus areas
  Outperform market growth

- Establish new financial model towards further growth
  Aim for world class ROE and 30%+ operating margin in the medium- to long-term
FY2018 (April 2017-March 2018) Highlights

- Net sales +41% YoY driven by the growth of the SPE* and FPD** market and expansion of market share in focus areas
- Operating income and net income attributable to owners of parent reached new record highs

Net Sales and Gross Profit Margin

Operating Income and Operating Margin

Net Income Attributable to Owners of Parent and ROE

* SPE: Semiconductor production equipment
** FPD: Flat panel display
FY2019 Financial Estimates

(Billion yen)

<table>
<thead>
<tr>
<th></th>
<th>FY2018 (Actual)</th>
<th>FY2019 (Estimates)</th>
<th>H1</th>
<th>H2</th>
<th>Full year</th>
<th>Full year YoY change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Net sales</td>
<td>1,130.7</td>
<td>690.0</td>
<td>710.0</td>
<td>1,400.0</td>
<td>+23.8%</td>
<td></td>
</tr>
<tr>
<td>SPE</td>
<td>1,055.2</td>
<td>634.0</td>
<td>654.0</td>
<td>1,288.0</td>
<td>+22.1%</td>
<td></td>
</tr>
<tr>
<td>FPD</td>
<td>75.0</td>
<td>56.0</td>
<td>56.0</td>
<td>112.0</td>
<td>+49.2%</td>
<td></td>
</tr>
<tr>
<td>Gross profit</td>
<td>475.0</td>
<td>288.0</td>
<td>310.0</td>
<td>598.0</td>
<td>+122.9</td>
<td></td>
</tr>
<tr>
<td>Gross profit margin</td>
<td>42.0%</td>
<td>41.7%</td>
<td>43.7%</td>
<td>42.7%</td>
<td>+0.7pts</td>
<td></td>
</tr>
<tr>
<td>SG&amp;A expenses</td>
<td>193.8</td>
<td>115.0</td>
<td>117.0</td>
<td>232.0</td>
<td>+38.1</td>
<td></td>
</tr>
<tr>
<td>Operating income</td>
<td>281.1</td>
<td>173.0</td>
<td>193.0</td>
<td>366.0</td>
<td>+84.8</td>
<td></td>
</tr>
<tr>
<td>Operating margin</td>
<td>24.9%</td>
<td>25.1%</td>
<td>27.2%</td>
<td>26.1%</td>
<td>+1.2pts</td>
<td></td>
</tr>
<tr>
<td>Income before income taxes</td>
<td>275.2</td>
<td>173.0</td>
<td>193.0</td>
<td>366.0</td>
<td>+90.7</td>
<td></td>
</tr>
<tr>
<td>Net income attributable to</td>
<td>204.3</td>
<td>128.0</td>
<td>142.0</td>
<td>270.0</td>
<td>+65.6</td>
<td></td>
</tr>
<tr>
<td>owners of parent</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Net income per share (Yen)</td>
<td>1,245.48</td>
<td>779.95</td>
<td>-</td>
<td>1,645.20</td>
<td>+399.72</td>
<td></td>
</tr>
</tbody>
</table>

Expect to generate record high profits* for third consecutive year

* Net income attributable to owners of parent
Substantially Outperform Market Growth

- FY’18 results (compared to FY’17)
  ⇒ TEL sales growth +41.4%  (WFE* market growth** +37%)
  Operating income growth +80.6%

- FY’19 estimate (compared to FY’18)
  ⇒ TEL sales growth +23.8%  (WFE market growth +15%)
  Operating income growth +30.2%

Grow share in focus areas (etch, cleaning, ALD systems)

* WFE (Wafer fab equipment): The semiconductor production process is divided into front-end production, in which circuits are formed on wafers and inspected, and back-end production, in which wafers are cut into chips, assembled and inspected again. Wafer fab equipment refers to the production equipment used in front-end production and in wafer-level packaging production.
** WFE market growth rates are for the calendar year.
**Medium-term Management Plan Progress**

<table>
<thead>
<tr>
<th>WFE*</th>
<th>FY’16 (Actual)</th>
<th>FY’17 (Actual)</th>
<th>FY’18 (Actual)</th>
<th>FY’19 (Estimate)</th>
<th>FY’20 financial model</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Market size</strong></td>
<td>$31B</td>
<td>$37B</td>
<td>$51B</td>
<td>$58B</td>
<td>$42B $45B</td>
</tr>
<tr>
<td><strong>Net sales</strong></td>
<td>¥663.9B</td>
<td>¥799.7B</td>
<td>¥1,130.7B</td>
<td>¥1,400.0B</td>
<td>¥1,050.0B ¥1,200.0B</td>
</tr>
<tr>
<td><strong>Operating margin</strong></td>
<td>17.6%</td>
<td>19.5%</td>
<td>24.9%</td>
<td>26.1%</td>
<td>24% 26%</td>
</tr>
<tr>
<td><strong>ROE</strong></td>
<td>13.0%</td>
<td>19.1%</td>
<td>29.0%</td>
<td>-</td>
<td>20-25%</td>
</tr>
</tbody>
</table>

* WFE (Wafer fab equipment): The semiconductor production process is divided into front-end production, in which circuits are formed on wafers and inspected, and back-end production, in which wafers are cut into chips, assembled and inspected again. Wafer fab equipment refers to the production equipment used in front-end production and in wafer-level packaging production.

FY2016 (CY2015) market size does not include equipment for wafer-level packaging.

Proceed according to plan in both strengthening competitiveness of products and raising profitability
We Are Now at a Turning Point

With the spread of IoT technology the age of big data is beginning.
Applications/services That Big Data Will Realize

- Telemedicine
- Smart mobility
- Smart cities
- Smart grids
- Autonomous driving
- Smart fabs
- Industrial robots

Demand for further technological evolution of semiconductors
Big Investment in the Cloud

Hyperscale data center construction boom

- Continuing data growth (CAGR 27%*)
- Necessary to replace servers every 5 years

338 ➡ 628 locations
CY2016 CY2021

Source: CISCO

* CISCO’s definition: Operator with annual revenue of over $1B from IaaS/PaaS, over $2B from SaaS, over $4B from internet, search and social networking, and over $8B in e-commerce/payment processing

** Source: CISCO GCI2017.2 CAGR of data center traffic 2016-2021

Continued strong demand for memory
New Trend: Edge Computing

Cloud computing

Edge computing

Health platforms
Autonomous driving
Smart fabs

Market growth for services where delay is unacceptable
Leading-edge chips with high speed and low power consumption are essential

- Too much data to process quickly
- Delay: Several hundred milliseconds

- Processes data in real-time from nearby
- Delay: Several milliseconds
Rising Added-value in SPE

WFE investment (100k WSPM*, greenfield/TEL estimate)

Expanded business opportunities for SPE manufacturers on arrival of new applications and rising level of technological difficulty

* WSPM: Wafer starts per month
Higher Sophistication of Display Technologies

Increasing screen size

Increasing resolution

Design flexibility

TV:
- FHD
- 4K
- 8K

Mobile, VR:
- 300 ppi
- 1000 ppi

Flexible, edge bent, free format

Expanded business opportunities due to technological change
WFE Market Outlook

WFE market by application*

CY’16  CY’17  CY’18*  CY’19*  CY’20*  CY’21*  
$37B    $51B    $58B    $61B    $62B    $63B    

* TEL estimate

- WLP
- DRAM
- Non-volatile memory
- Logic foundry
- Logic & others (MPU, AP, others)

WFE market approaching $60B+ phase
## New Financial Model (FY2021)

<table>
<thead>
<tr>
<th>WFE</th>
<th>Market size</th>
<th>$55B</th>
<th>$62B</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Net sales</strong></td>
<td>¥1,500.0B</td>
<td>¥1,700.0B</td>
<td></td>
</tr>
<tr>
<td><strong>Operating margin</strong></td>
<td>26.5%</td>
<td>28%</td>
<td></td>
</tr>
<tr>
<td><strong>ROE</strong></td>
<td>30-35%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Aim for a world class operating margin of 30%+ in the medium- to long-term
Rationale for Revisions to Financial Model

- Business development in focus areas is making good progress, and achievement of the financial model announced in May 2017 is in sight.

- Over the past year it has become widely recognized that the semiconductor industry has entered a new growth stage on the expansion of new applications that support social infrastructure such as AI and IoT.

- On outlook for further growth in the semiconductor industry we have upwardly revised our expected WFE market size to $62B in FY2021.

- Even if WFE should shrink to $55B due to temporary market shifts, we will aspire to a management structure that is able to flexibly respond to market shifts and to secure net sales of ¥1,500.0B and an operating margin of 26.5%.

Establish new financial model based on further market growth and opportunities for significant growth for TEL.
Three Focus Areas for New Growth Opportunities

Product competitiveness

- Create strong next-generation products
- Constantly pursue higher management efficiency
- Higher productivity

Responsiveness to customers

- Become the best and sole strategic partner

Make steady progress in Best Fit in New Market = “responding to diversity” and achieve Best in Class, as stated in our 2015 medium-term
Highlights from the Past 3 Years (Initiatives to Date)

1. Reorganization of Development & Production Group
   - Established Process Integration Center (PIC)
   - Merged Yamanashi and Tohoku plants, established TEL Technology Solutions
   - Built new development building for etch systems
     (Scheduled for completion Sep. 2018)
   - Made systems intelligent through utilization of AI and IT

2. Established new account structure (Global Field Div.)

3. Reorganized business units (CTSPSBU, TFFBU)

4. Responded to increased production
   (etch, deposition and test systems)

5. Introduced new global HR systems
Further Promotion of Our 3 Focus Areas (Future Initiatives)

1. Promote development of technologies that leverage TEL’s comprehensive strengths
   - Process integration technology that unites diverse technologies
   - Develop next generation platforms

2. Promote early stage joint development and evaluation with customers
   - Share roadmap for multi-generational technologies: shift collaboration “from dots to lines”
   - Expand onsite evaluation activity

3. Increase productivity and added-value using data and AI
4. Respond to growing China business
5. Increase earnings in field solutions business
6. Promote efficiency though launch of business reform project
7. Implement medium-term incentive plan
Field Solutions (FS)

Leverage our strengths as an equipment manufacturer to increase earnings in both the used equipment/modification and part/service segments.

Business strategy

- Respond to new customer needs driven by IoT
  - Provide upgrades and remanufactured equipment that handle new applications
- Contribute to improving customer productivity
  - Provide added-value services using remote connections
  (Installed base of 66,000 units)
Response to Growth in China Business

- Expect China to comprise 30% of WFE (CY’20)
  - Customers planning 10-15 new plants (CY’18-CY’20)
- Capture high share and service business through high value added products and comprehensive support
- Build solid business base
  - Hiring of engineers going well (3x vs CY’16)
  - Enhance training centers

Steadily build business base in growing market
Increasing Development and Production Capabilities

- Miyagi plant (etch systems)
  - Began operations at new logistics building, plan to raise productivity through automation
  - New development building (plan to complete by September)
  - Double production capability (plan to begin operations from October)

- Yamanashi and Tohoku plants (deposition, gas chemical etch, test systems)
  - Decided to build new production buildings
  - Strengthen BCP* with high earthquake resistance

* BCP: Business continuity plan

Secure development and production capabilities in line with further growth stage
## TEL’s Sustainability (economic value × social value = corporate value creation)

- Going forward, continue to work to resolve social issues and contribute to the achievement of sustainable development goals (SDGs) through our business activities in accordance with the Ten Principles of the UN Global Compact and RBA* code of conduct.

### Environment
- Climate change, water, biodiversity, environmental management

### Social
- Human rights, employment and labor, health and safety, supply chain, local communities

### Governance
- Corporate governance, compliance, risk management

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Continue to be a company trusted by all stakeholders

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* RBA: Responsible business alliance
Contributing to the Environment is a Key Strategy

- Lower energy consumption of TEL products
- Manufactured devices realize low power consumption

Result: Raises TEL’s value

Technological proposals that reduce environmental impact create significant value
## New Financial Model (FY2021)

<table>
<thead>
<tr>
<th>WFE market Market share</th>
<th>FY2018 (Actual)</th>
<th>FY2019 (Estimates)</th>
<th>FY2021 (Plan)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$51B 14%</td>
<td>$58B 15%</td>
<td>$55B 18%</td>
</tr>
<tr>
<td>Net sales</td>
<td>1,130.7</td>
<td>1,400.0</td>
<td>1,500.0</td>
</tr>
<tr>
<td>SPE</td>
<td>1,055.2</td>
<td>1,288.0</td>
<td>1,400.0</td>
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<td>FPD</td>
<td>75.0</td>
<td>112.0</td>
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<td>Gross profit</td>
<td>475.0</td>
<td>598.0</td>
<td>650.0</td>
</tr>
<tr>
<td>Gross profit margin</td>
<td>42.0%</td>
<td>42.7%</td>
<td>43.3%</td>
</tr>
<tr>
<td>SG&amp;A expenses</td>
<td>193.8</td>
<td>232.0</td>
<td>252.0</td>
</tr>
<tr>
<td>SG&amp;A expenses to sales ratio</td>
<td>17.1%</td>
<td>16.6%</td>
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<tr>
<td>Operating income</td>
<td>281.1</td>
<td>366.0</td>
<td>398.0</td>
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<td>26.5%</td>
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<tr>
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<td>204.3</td>
<td>270.0</td>
<td>292.0</td>
</tr>
<tr>
<td>Net profit margin</td>
<td>18.1%</td>
<td>19.3%</td>
<td>19.5%</td>
</tr>
</tbody>
</table>

Increase corporate value through innovative technologies and groundbreaking proactive solutions, raise efficiency and secure even higher profitability and resistance to market shifts.
### Gross Profit, SG&A Expenses (Sales ¥1,700.0B Model)

#### (Billion yen)

<table>
<thead>
<tr>
<th></th>
<th>FY2018 (Actual)</th>
<th>FY2019 (Estimates)</th>
<th>FY2021 (Plan)</th>
<th>Growth rate (FY’18-FY’21)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gross profit</td>
<td>475.0</td>
<td>598.0</td>
<td>745.0</td>
<td>+57%</td>
</tr>
<tr>
<td>Gross profit margin</td>
<td>42.0%</td>
<td>42.7%</td>
<td>43.8%</td>
<td>+1.8pts</td>
</tr>
</tbody>
</table>

- Raise gross profit margin of core SPE, FPD products
  - Timely introduction of new products to an expanding market
  - Lower cost ratio through product quality improvements

#### (Billion yen)

<table>
<thead>
<tr>
<th></th>
<th>FY2018 (Actual)</th>
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<th>FY2021 (Plan)</th>
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<td>17.1%</td>
<td>16.6%</td>
<td>15.8%</td>
<td>-1.3pts</td>
</tr>
</tbody>
</table>

- Proactively invest in growth areas while planning appropriate SG&A and R&D expenses
R&D Expenses, Capex Plan

Conduct proactive investment towards further growth
Accounts receivable turnover
- Current: 52 days ⇒ Achieved target

Inventory turnover
- Current: 111 days ⇒ Target: 95 days

ROE
- Current: 29% ⇒ Target: 30-35%

Maintain focus on assets and capital efficiency
Capital Policy, Shareholder Returns

- **Approach to capital policy**
  - While closely monitoring the business environment and our necessary cash balance, we will strive to raise ROE through earnings maximization and by raising capital efficiency

- **Approach to shareholder return policy (basically linked to performance)**

  **Dividend payout ratio:** 50%

  **Annual DPS of not less than ¥150**

  We will review our policy if the company does not generate net income for 2 consecutive fiscal years

  **We will flexibly consider share buybacks**

  No change in shareholder return policy
Summary

- Establish new financial model backgrounded by expected growth in semiconductor and production equipment markets. Aim for short, medium and long term growth.

- Aim to increase sales beyond market growth rate through stronger competitiveness of products and deeper cooperation with customers.

- Raise development efficiency and business productivity and secure even higher profitability and resistance to market shifts.

Aim for sustained growth in corporate value through a management base with global-standard strength.
Evolving Semiconductor Device Application and the Future of Process Technology

May 29, 2018

Akihisa Sekiguchi, Ph.D.
VP & GM, Deputy General Manager, Technology Strategy Division, Advanced Semiconductor Technology Division, Global R&D
Outline

- Trends and issues in semiconductor process technology: Mainstream devices (CMOS Logic, NAND, DRAM)
- Technology challenges deep dive: Logic devices
- Devices that may drive further growth of the WFE market in the future autonomous driving enablers and AI
- Summary
Trends and Issues in Semiconductor Process Technology
Process Technology Issues for Major Semiconductor Devices

3D NAND
- Multi-layering & productivity
- High selectivity process
- Realizing highly uniform process suitable for 3D structures

DRAM
- Enhancements from 1Y-1Z
- High aspect ratio process, enhanced precision and material specific adaptation to achieve higher bit density

Logic
- 5 & 3 nm development
- Precision patterning process co-optimized for device design and new materials

Drive collaboration in & out of the company to accelerate creation of innovative process technologies
Increasing number of layers requires a variety of new technical solutions.
DRAM Technical Issues

Higher capacitance $\rightarrow$ Higher dielectric constant

RC delay due to miniaturization $\rightarrow$ Introduction of logic Cu interconnects

Source: TECHINSIGHTS

Cylinder (Present)
Scaling limit
Pillar (Future)

Needs higher-k and lower leak current

From Al to Cu wiring
Technology Challenges Deep Dive: Logic Devices
Device Scaling Trends

Complex 3D processes to realize N3 EUV slowly gets manufacturing adoption
Scaling Issue: Overlay

Step 1: Line/Space
Cross section of a logic structure

Step 2: Cut
Self aligned multi patterning (SAMP) with high etch and dep usage

EUV intro

LELELE = (Litho-Etch)_3 (etch and dep usage reduced)

Multi-expo: (Litho + Etch) x n
Overlay error for every exposure
Lower yield
3 masks
Too close
Closer
Too far

EUV

Single expo: (Litho + Etch) x 1
Overlay error reduced
1 mask
Higher yield

iArF

1 mask

EUV reduces overlay error but SAMP is still in use
### Logic FEOL/MOL Technology Roadmap

<table>
<thead>
<tr>
<th>Node</th>
<th>16-14 nm</th>
<th>10 nm</th>
<th>7 nm</th>
<th>5 nm</th>
<th>&lt; 3.5 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Transistor</strong></td>
<td>FinFET</td>
<td></td>
<td></td>
<td></td>
<td>Nanowire/Nanosheet FET</td>
</tr>
<tr>
<td><strong>Contact</strong></td>
<td>Diamond shaped Epi</td>
<td>Contact</td>
<td>Wrap around contact</td>
<td>Contact</td>
<td>Co and other materials</td>
</tr>
</tbody>
</table>

Scaling and performance enhancement concurrently requires structure, design and material changes, which makes integration challenging.
Complexity of the Fabrication Processes for Logic Devices

Nanowire FET

Wrap around contact (WAC)

Self-aligned contact (SAC)

R. Coquand et al., VLSI tech. 2013

Precise control in an atomic level

Conventional patterning

Multi-color patterning

Applications

<table>
<thead>
<tr>
<th></th>
<th>N+1</th>
<th>N+2</th>
<th>N+3</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEOL</td>
<td>Patternning and hard mask</td>
<td>Nanowire FET</td>
<td></td>
</tr>
<tr>
<td>MOL</td>
<td>Patternning and hard mask</td>
<td>Contact structure (WAC)</td>
<td></td>
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<tr>
<td></td>
<td>New plug material (Ru)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BEOL</td>
<td>Patternning and hard mask</td>
<td>EUV productivity</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Selective deposition</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common</td>
<td>Pitch imbalance control</td>
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</tbody>
</table>

Design and process technology co-optimization is a challenging integration issue
Major Semiconductor Devices: FinFET

FinFET formation alone is a complicated process
Challenges in Nanowire/Nanosheet Fabrication

Nanowire/Nanosheet formation is even more complicated than FinFET
Structural formation modelling and electrical simulation are now a must
## Logic BEOL Technology Roadmap

<table>
<thead>
<tr>
<th>Node</th>
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<th>5 nm</th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Patterning</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Dual damascene</td>
<td>SAV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Self-aligned via (SAV)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Non SAV</td>
<td>SAV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Metallization</strong></td>
<td>Cu: ECD Ta/TaN PVD</td>
<td>Cu</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Replacement of Cu: Ru, Co, CoAl</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Self-aligned block (SAB)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fully self-aligned via (FSAV)</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Scaling and overlay issues require new integration schemes

TEL's estimates using IEDM, VLSI symposium, IITC papers
R&D for Future Growth: Beyond Cu

- Line width reduction is pushing copper to its limits
- New material required

Source: An Steegen, imec technology forum 2017
New Opportunities through Integration

Buried power rail (new material)

Source: imec presentation at ISPD 2016

Close integration between process equipment is a must in order to propose solutions to realize further scaling through new materials and structural solutions.
Devices That May Drive Further Growth of the WFE Market in the Future Autonomous Driving Enablers and AI
Autonomous Driving

Semiconductor usage will increase with the arrival of autonomous driving

Higher Automotive Functionality

- Hybrid vehicles use 2.5-3 times more semiconductor devices compared to conventional gasoline vehicles
- Electric vehicles use even more than 2x
- With ADAS*, additional value add is $50-$100
- Autonomous driving vehicles transit 6TB of data daily to Data Centers

* ADAS: Advanced driver assistance system

Increase in semiconductor usage from conventional gasoline, hybrid, electrical, to autonomous vehicles (not to mentions the infotainment data related adders)

- ADAS today uses 6 cameras per vehicle
- In the near future, ~10 per vehicle
  - Interior, driver, passenger monitoring
  - AR/VR
  - Airbag control
ADAS • Device Challenges for Autonomous Driving

- **Viewing, Sensing camera**
  - Front 1-2, back1-3, CIS
  - In the future 10-12
  - Higher pixel density
  - Faster image readout
  - Processing circuit

- **LiDAR* cost**
  (Infrared laser scan in 3D)
  - High end LiDAR: ~few million yen
  - Motorless MEMS version will drive cost below 50,000 yen

- **mm radar**
  - Higher resolution, wider angle
  - From SiGe to Si CMOS (~2019)
  - Integrated communication IC and micro controller (~2022)

- **Processor/Memory/ECU**
  - CPU under autonomous driving use a few KW
  - DRAM degradation under high temp (refresh cycle)
  - Using auto temperature grade LPDDR4
    - High temp tolerant DRAM cell
    - Error reduction circuit
    - Data/ECC*** transmission function
  - Flexible ECU development

---

* LiDAR: Laser imaging detection and ranging  
** ECU: Engine control unit  
*** ECC: Error correction code
Autonomous driving vehicles may use 10x (cost) in terms of semiconductors versus conventional gasoline vehicles.
Semiconductor Sales Amount

Worldwide Semiconductor Sales Estimate

<table>
<thead>
<tr>
<th>Year</th>
<th>Military/Civil Aerospace</th>
<th>Industrial</th>
<th>Data Processing</th>
<th>Consumer</th>
<th>Communication</th>
<th>Automotive</th>
<th>Automotive rate</th>
<th>Industrial rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY’16</td>
<td>346</td>
<td>9.9%</td>
<td>9.3%</td>
<td>9.9%</td>
<td>10.0%</td>
<td>12.8%</td>
<td>10.8%</td>
<td>15.4%</td>
</tr>
<tr>
<td>CY’17</td>
<td>420</td>
<td>9.8%</td>
<td>9.3%</td>
<td>9.2%</td>
<td>10.1%</td>
<td>12.1%</td>
<td>10.8%</td>
<td>15.1%</td>
</tr>
<tr>
<td>CY’18</td>
<td>470</td>
<td>9.9%</td>
<td>9.2%</td>
<td>9.6%</td>
<td>10.1%</td>
<td>12.1%</td>
<td>10.8%</td>
<td>15.0%</td>
</tr>
<tr>
<td>CY’19</td>
<td>502</td>
<td>10.1%</td>
<td>9.9%</td>
<td>10.1%</td>
<td>11.2%</td>
<td>12.1%</td>
<td>11.9%</td>
<td>16.9%</td>
</tr>
<tr>
<td>CY’20</td>
<td>493</td>
<td>12.1%</td>
<td>11.9%</td>
<td>12.4%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY’21</td>
<td>497</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY’22</td>
<td>520</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>


Semiconductor market will continue to grow nicely in the future.
Artificial Intelligence

Phenomenal growth rate of AI Semiconductors

AI chip development intensifying

AI devices expected to grow at an annualized rate of almost 70%

Source: Gartner Forecast: AI Neural Network Processing Semiconductor Revenue, Worldwide, 2018 , 11 January 2018
Charts/graphics created by Tokyo Electron based on Gartner research
Motivation for AI Chip Development

- **GPU (Graphics Processing Unit)**
  - De facto standard for deep learning today
  - But energy consumption is high and requires additional cooling mechanism
  - For loosely linked neural networks, there is inefficiencies in computation
    - Some data centers use FPGAs listed below
    - New ASICs are being developed and further evolution is needed as an accelerator

- **FPGA (field-programmable gate array)**
  - Adapts to the various deep learning calculation models and circuits can be modified flexibly
  - But computation is relatively slow (clock frequency: tens of MHz - hundreds of MHz)
  - Design hurdle is high and requires hardware knowledge

- **Neuromorphic**
  - New brain like architecture and device development is being accelerated to optimize AI application
  - Existing semiconductor processes and materials are thought to be compatible
  - Tokyo Electron Limited works with multiple partners to address AI development needs
New semiconductor devices will grow WFE market over the medium- to long-term.
Summary
Summary – Diversity of Semiconductor Technology

More Moore

CMOS scaling

2017~

Now

Patterning

Logic with new material, new structure

- Strained Si
- High-k metal gate

- FinFET
- Cu/ULK
- ArF-immersion
- DP/MP
- EUV
- NIL, EBDW

- CFET
- Nanowire FET
- ReRAM

- NAND
- 3D NAND
- STT-MRAM

- Wire-bonding
- InFO
- 2.5D

- DRAM
- DRAM

More than Moore

Heterogeneous

Si photonics

Advanced packaging (3DI/WLP)

Emerging memory

- Neuromorphic
- Neuromorphic
- Neuromorphic
Devices That Have Made Today’s Technology Possible

With new devices like AI and Neuromorphic chips joining the mix, the market will continue to grow synergistically with the communication system network growth.
Technology Evolution at a Glance
Coater/developer, Cleaning System Business Strategy

May 29, 2018

Seisu (Yoh) Ikeda
SVP & GM, Deputy General Manager, Business Division, General Manager, CTSPS BU
Coater/developer and Cleaning Systems Market Outlook

TEL’s coater/developer and cleaning SAM* in WFE market

- **Coater/developer**
  - Introduction of EUV lithography for mass production
  - Established regional offices in China and expanded support for customers

- **Cleaning system**
  - Growth in wet etch market for 3D NAND
  - Increased demand for bevel cleaning
  - Further demand for drying technology that prevents pattern collapse accompanying miniaturization

Growth in coater/developer and cleaning systems markets on demand for increasing density of semiconductor components
EUV: Approach and Results

- Linking valuable data, customer needs, issues and information received through many collaborative businesses with development
- Maintain 100% share in EUV in-line equipment market

Continue acceleration of further EUV development
## Changing Issues in Introduction of EUV Mass Production (announced at EUVL Symposium)

<table>
<thead>
<tr>
<th>Priority</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Reliable source operation with &gt; 75% availability</td>
<td>Reliable source operation with &gt; 85% availability</td>
<td>Reliable source operation with &gt; 85% availability</td>
<td>Resist resolution, stochastics, and sensitivity met simultaneously</td>
</tr>
<tr>
<td>2</td>
<td>Resist resolution, sensitivity &amp; LER* met simultaneously</td>
<td>Resist resolution, sensitivity &amp; LER met simultaneously</td>
<td>Resist resolution, sensitivity &amp; LER met simultaneously</td>
<td>Reliable source &gt; 250W operation with &gt; 90% availability</td>
</tr>
<tr>
<td>3</td>
<td>Mask yield &amp; defect inspection/review infrastructure</td>
<td>Mask yield &amp; defect inspection/review infrastructure</td>
<td>Keeping mask defect free</td>
<td>Keeping mask defect free</td>
</tr>
<tr>
<td>4</td>
<td>Keeping mask defect free</td>
<td>Keeping mask defect free</td>
<td>Mask yield &amp; defect inspection/review infrastructure</td>
<td>Mask yield &amp; defect inspection/review infrastructure</td>
</tr>
</tbody>
</table>

* LER: Line edge roughness

**Source:** 2017 EUVL Symposium Closing Remarks

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**Importance of resist performance and coater/developer technology increasing within EUV process**
Product Strategy for Coater/developers

- Promote unification of system platforms
  - Improve value for customers and unify development with latest platform of LITHIUS Pro™ Z series

- Develop value-added products for miniaturization and 3D structures
  - Address 3D NAND wafer warpage

- Improve quality of service and efficiency through use of data and automation
  - Realize high-quality global support not reliant on technical skill of personnel
Growth of TEL’s Cleaning Business

- **CY’17 market share: 25% (YoY+5pts, achieved medium-term plan early)**

<table>
<thead>
<tr>
<th>Market share</th>
<th>CY’15 (Actual)</th>
<th>CY’16 (Actual)</th>
<th>CY’17 (Actual)</th>
<th>. . .</th>
<th>CY’20 (Target)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cleaning system</td>
<td>18%</td>
<td>20%</td>
<td>25%</td>
<td>. . .</td>
<td>27%+</td>
</tr>
</tbody>
</table>

- **Expand sales of CELLESTA™ single wafer cleaning system**
  - Bevel cleaning*: Improved yield around extreme edge of wafer
  - Post-etch cleaning for memory: improved productivity
  - Apply best known coater/developer methods to cleaning system business
    - Share leading-edge technology and expertise by unifying development

- **Expand sales of EXPEDIUS™ batch cleaning system**
  - Contribute to improved productivity of 3D NAND
  - Improve wet etch performance and contribute to enhanced yield

---

* Bevel cleaning: process for removing unnecessary film from the outer part of the wafer

Due to increasing number of films stacked on wafer, films on a wafer’s extreme edge become defects, affecting yield

Established leading position in developing equipment for accurate removal of film from a wafer's extreme edge, improving yield for customers

CORP IR / May 29, 2018
Evolving Devices: Issues and Factors Lowering Yield

- Increased impact on wafer edge due to multi-layering
  - Concern over film delaminating from edge and wafer warpage

- Impact of microscopic particle on device yield in miniaturization
  - Increase of patterning processes
  - Increase of 3D structures

- Increased risk of pattern collapse in miniaturization
  - Increased difficulty in drying due to higher aspect ratio of device structure

Further increase of factors reducing yield for customers on progression of multi-layering and miniaturization
TEL’s Initiatives on Factors Affecting Lower Yield

- Increased impact on outer part of wafer due to multi-layering
  - Contribute to improving factors that reduce yield due to impact on wafer edge

- Impact of microscopic particle in miniaturization
  - Develop TEL original technologies enabling removal of microscopic particles and particles between patterns

- Increased risk of pattern collapse in miniaturization
  - Develop drying technology which takes advantage of TEL’s original surface modification technology, etc.

Aim to further increase share by contributing to the improvement of yield for customers
Summary

- Coater/developer: Maintain high share and raise value by continuing to differentiate via technological development through collaborative activities in leading-edge technology sectors, especially EUV.

- Coater/developer: Maintain high share and enhance our ability to support customers in China, where the market is growing rapidly.

- Cleaning system: Continue to differentiate via technological development, focusing on processes where customers need a high level of technological support, such as improving yield.

- Synergies: Raise efficiency of development and production by sharing BKM* and promoting unification of development, production and management of coater/developer and cleaning systems.

* BKM: Best known method
Etch System Business Strategy

May 29, 2018

Yoshinobu Mitano
SVP & GM, General Manager, ES BU
Etch System Market Outlook

Trends in etch technology

- **Miniaturization of DRAM**
  - Increases in patterning and copper interconnect processes

- **Multi-layering of 3D NAND**
  - Higher ratio of HARC* process

- **Miniaturization and greater structural complexity of logic**
  - Increases in patterning processes, isotropic etch

* HARC (High aspect ratio contact) process: a process for forming deep holes that requires advanced processing technology

Growth in etch system market due to increase in patterning processes and greater structural complexity
Business Opportunities and Strategy

- Win share and raise profitability by leveraging technological advantage
  - DRAM: Win share in patterning process, etc. through productivity differentiation
  - NAND: Win share in new HARC process through technological differentiation
  - Logic:
    - Leverage RLSA™ plasma silicon etch to drive sales growth in transistor periphery processes
    - In contact processes, aim to increase share with atomic layer etch (ALE)
    - In 3D transistors, capture share with isotropic etch

- Grow sales through proactive development and investment in production

<table>
<thead>
<tr>
<th>Market share</th>
<th>CY’15 (Actual)</th>
<th>CY’16 (Actual)</th>
<th>CY’17 (Actual)</th>
<th>...</th>
<th>CY’20 (Target)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etch system</td>
<td>21%</td>
<td>23%</td>
<td>26%</td>
<td></td>
<td>30%+</td>
</tr>
</tbody>
</table>

Focus on HARC, patterning, 3D structure processes, aim for 30%+ share by CY2020
Memory: Results and Initiatives

DRAM

- Capacitor process (HARC)
- Copper interconnects process: Leveraged knowledge of logic to win share
- Patterning: Realized reduced costs for customers by combining etch steps

3D NAND HARC process

- Differentiate with technology related to process accuracy, grew share in 6X/9X generations, and aim to capture additional processes in 12X

DRAM: Won share in target areas, doubling share from 3 years ago
NAND: Won application from second customer in slit process.
Aim to leverage new technology to increase POR wins
Logic: Focus Processes and Key Points

- Transistor periphery 3D structures
  - FinFET
  - Nanowire
  - Nanosheet

- Miniature contact process
  - SAC (Self-aligned contact)

Key requirement
1. High SiN selectivity (less SiN loss)
2. Narrow slit etch capability

- Contact/interconnect process; more complex patterning

Leverage technological advantage in increasingly complex etch processes, respond to new needs
Leading-edge Logic Initiative 1: Silicon Etch

Superior aspects of RLSA™ plasma etcher in silicon etch

<table>
<thead>
<tr>
<th>Typical ICP etcher</th>
<th>RLSA™ plasma etcher</th>
</tr>
</thead>
<tbody>
<tr>
<td>Faceting</td>
<td>Rectangle</td>
</tr>
<tr>
<td>Depth variation</td>
<td>Equal depth</td>
</tr>
<tr>
<td>Non-vertical form</td>
<td>Vertical shape</td>
</tr>
</tbody>
</table>

In silicon etch, differentiate through processing performance and productivity.
Leading-edge Logic Initiative 2: Highly Selective Etch

<table>
<thead>
<tr>
<th>Conventional etch</th>
<th>Quasi-ALE*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Self-aligned contact</td>
<td></td>
</tr>
<tr>
<td>Si-ARC etch</td>
<td></td>
</tr>
</tbody>
</table>

*ALE (Atomic layer etch): Highly selective etch technology at the atomic level

Aim to win share through rising demand for highly selective etch
Leading-edge Logic Initiative 3: Gas Chemical Etch

Broadening of applications for gas chemical etch

- Min. Fin pitch
- Si
- SiGe

N+1

- Min. Fin pitch
- Si
- SiGe

N+2

- Min. Fin pitch
- Si
- SiGe

N+3

- Nanowire
- Nanosheet

Differentiate through isotropic selective etch technology needed for 3D transistors
Miyagi Plant: New Logistics Building and Module Assembly and Shipping, New Development Building

Module: EFEM*
Production start: Jan. 2018

Module: VTM**
Production start: Sep. 2018

New development building
Scheduled completion: Sep. 2018
Total floor space: 11,700m²

* VTM (Vacuum transfer module): Module that sends wafers to etch chamber
** EFEM (Equipment front end module): Module that moves wafers from FOUP/load ports to VTM
Summary

- Expect continued growth in the etch system market driven by multi-layering of 3D NAND and increasing complexity in logic patterning

- Aim to raise profitability by focusing on TEL’s strengths in HARC, patterning, interconnects, achieving share of 30%+ in CY’20 through technological differentiation

- We will proactively invest towards further market growth
Deposition System Business Strategy

May 29, 2018

Shingo Tada
VP & GM, General Manager, Thin Film Formation BU
Miniaturization and evolving device structure are driving growth of the high value-added deposition market.
Business Opportunities and Strategy

- In areas where we already participate in the deposition market (ALD, CVD and diffusion furnaces), introduce technology with high added value and outperform market growth
  - Introduce next generation thermal processing systems with higher productivity and controllability
  - Introduce new single wafer platform for cluster process

- Accelerate development of new materials, new applications
  - Evaluate new materials for metal deposition systems
  - Develop anisotropic deposition and selective growth process

<table>
<thead>
<tr>
<th>Market share</th>
<th>CY’15 (Actual)</th>
<th>CY’16 (Actual)</th>
<th>CY’17 (Actual)</th>
<th>CY’20 (Target)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deposition system</td>
<td>38%</td>
<td>37%</td>
<td>36%</td>
<td>40%+</td>
</tr>
</tbody>
</table>

Focus on high value added deposition processes, aim for 40%+ share in CY2020
Approach to Deposition Market

ALD system

- In semi-batch systems, make high quality film required for miniaturization and shift to 3D structure, and raise productivity

CVD system

- Use our huge productivity advantage in batch systems to differentiate in memory
- Achieve high quality metal deposition to enable further miniaturization

Aim to grow profit through and new technology for further miniaturization and next-generation semiconductors
Initiatives in the Deposition Market

**ALD system**

- **Semi-batch ALD system NT333™**
- **ALD system market share (CY2017)**: 31.4% (No.1 ranked)
  - YoY +2.4%pts
- **TEL** and **Others**

**CVD system**

- **Single wafer CVD system market share (CY2017)**: 33.8% (No. 2 ranked)
  - YoY +5.0%pts
- **Metal deposition system Trias™**

**Focus on growing share in market segment expanding due to miniaturization**

Dielectric Film Deposition Technology for High Aspect Ratio Structure

Realized high productivity deposition technology that forms high quality, uniform dielectric film without pattern dependence.
Metal Deposition Technology for High Aspect Ratio

DRAM
- Bottom electrode deposition
- Upper electrode deposition
- Word line, contact barrier deposition

3D NAND
- ASFD: Advanced sequential flow deposition

- ✓ High throughput
  - Minimizes chamber volume
  - High speed, high concentration gas injection system
- ✓ Uniformity
  - Symmetrical gas flow design

ASFD: Advanced sequential flow deposition

Φ30 nm
Aspect ratio = 40:1

Non-uniformity < 1.0% @ 1 sigma

Step coverage > 90%

Optimized deposition chamber design for ASFD provides high performance and high productivity
Deposition Systems: Striving for Further Growth

- Next generation thermal processing system
  - Introduce SLB* product with high productivity and efficiency
  - Adoption of new, high precision controller will contribute to enhance tool matching and increasing uptime
  
- New single wafer platform
  - Smaller footprint, higher productivity
  - Enables diverse cluster processes

* SLB: Super large batch

Expand market share in areas where we already participate in by increasing productivity and responding to diverse process needs
Deposition Systems: Initiatives Towards New Materials and Applications

- Evaluation of new materials for metal deposition systems
  - Achieve low resistance with thin wire
  - Excellent gap fill capabilities

- Develop anisotropic deposition and selective deposition
  - Achieving gap fill and bottom up processes by using TEL’s unique deposition technique

Expanding SAM through the development of new applications for miniaturization
Augmenting Production System

New building at Yamanashi (Fujii) Plant

- Construction start (scheduled): January 2019
- Completion (scheduled): April 2020
- Products: Single wafer deposition, gas chemical etch, and test systems

New building at Tohoku Plant

- Construction start (scheduled): October 2018
- Completion (scheduled):
  - September 2019 (First phase)
  - December 2020 (Second phase)
- Products: Thermal processing systems

Expand production system, flexibly respond to future growth in demand
Summary

- Deposition market continues to expand, especially in memory
- Expand our market share in the fields of ALD, single wafer CVD and thermal processing systems, by raising the competitiveness of our existing products and introducing new products
- Start construction of new factory buildings in FY2019, increase production capacity for sustainable growth
FPD Business Strategy

May 29, 2018

Tsuguhiko Matsuura
VP & GM, General Manager, FPD BU
FPD Medium-term Plan

Progressing according to plan towards achieving 20% operating margin target in medium-term plan

Data based on IHS Markit, Technology Group, Display Supply Demand Equipment Tracker Q4 2017. Results are not an endorsement of Tokyo Electron Limited. Any reliance on these results is at the third party's own risk. Visit technology.ihs.com for more details.
Medium-term Plan Progress: Highlights

- Established our leading position in G10.5
- Introduced new Betelex™ platform etch system
- Expansion of PICP™* etch system going well

* PICP: Plasma source for producing extremely uniform high density plasma on substrate
### Display Trends

#### Increasing screen size
- [Image of increasing screen size]

#### Increasing resolution
- **TV**
  - FHD
  - 4K
  - 8K
- **Mobile, VR**
  - 300 ppi
  - 1000 ppi

#### OLED vs. LCD
- **OLED**
  - Color filter
  - LCD
  - TFT
  - Backlight
- **LCD**
  - TFT
  - Emissive layer

#### Design flexibility
- Flexible, edge bent, free format

---

**Technological change in displays increasing business opportunities**
Business Opportunity: G10.5 Equipment Market

- Greater-than-expected growth in investment
- Maintain high market share through technological differentiation (large area plasma control, air floating coater)

Increased sales far beyond market growth by meeting customers’ technological needs

Data based on IHS Markit, Technology Group. Display Supply Demand Equipment Tracker Q4 2017. Results are not an endorsement of Tokyo Electron Limited. Any reliance on these results is at the third party’s own risk. Visit technology.ihs.com for more details.
### Business Opportunity: Metal Oxide/LTPS

<table>
<thead>
<tr>
<th>TFT array</th>
<th>a-Si</th>
<th>Metal Oxide</th>
<th>LTPS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Representation of structure</strong></td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
<td><img src="image3.png" alt="Image" /></td>
</tr>
<tr>
<td><strong>Application</strong></td>
<td>LCD TV Monitor</td>
<td>OLED TV Tablet</td>
<td>Smartphone (LCD/OLED)</td>
</tr>
<tr>
<td><strong>Number of masks</strong></td>
<td>5</td>
<td>6-8</td>
<td>9-13</td>
</tr>
<tr>
<td><strong>Dry etch processes</strong></td>
<td>3 a-Si, SiNx</td>
<td>3 SiO, SiNx</td>
<td>~11 SiO, metal</td>
</tr>
</tbody>
</table>

**Further new needs**

- Flexible displays + 2 processes
- OLED process (G6 Half Size) + 3-4 processes

**Number of etch processes increased as more advanced technology sought**
Business Opportunity: Growth of OLED TV Market

- Material utilization significantly more efficient than current evaporation method
- Companies improving functionality of ink

Data based on IHS Markit, Technology Group, Display Long-Term Demand Forecast Tracker Q4 2017. Results are not an endorsement of Tokyo Electron Limited. Any reliance on these results is at the third party’s own risk. Visit technology.ihs.com for more details.

Differentiate with inkjet printing system towards growth in the OLED TV market
Summary

- Increase share and profitability in growing market, business progressing according to plan
- New medium-term plan FY2021 target: sales ¥100.0B, operating margin over 20%
- For leading-edge production processes, focus on areas where we have technological superiority
  - High performance PICP™ etch system
  - Etch system and coater/developer for G10.5 substrate
  - Inkjet printing system for OLED TVs