Medium-term Management Plan Progress and TEL Initiatives

May 31, 2017

Toshiki Kawai
Representative Director, President & CEO
FY2017 Financial Highlights

- Net sales increased by 20% YoY, highest ever SPE* sales
- Set new record highs for GPM, OPM and net income
- ROE of 19.1% (+6.1pts YoY). Further increased capital efficiency
## FY2018 Financial Estimates

(Billion Yen)

<table>
<thead>
<tr>
<th></th>
<th>FY2017 (Actual)</th>
<th>FY2018 (Estimates)</th>
<th>Full year YoY change</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1st half</td>
<td>2nd half</td>
</tr>
<tr>
<td>Net sales</td>
<td>799.7</td>
<td>480.0</td>
<td>500.0</td>
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<tr>
<td>SPE</td>
<td>749.8</td>
<td>451.0</td>
<td>459.0</td>
</tr>
<tr>
<td>FPD*</td>
<td>49.3</td>
<td>29.0</td>
<td>41.0</td>
</tr>
<tr>
<td>Gross profit</td>
<td>322.2</td>
<td>202.0</td>
<td>210.0</td>
</tr>
<tr>
<td>Gross profit margin</td>
<td>40.3%</td>
<td>42.1%</td>
<td>42.0%</td>
</tr>
<tr>
<td>Operating income</td>
<td>155.6</td>
<td>104.0</td>
<td>112.0</td>
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<tr>
<td>Operating margin</td>
<td>19.5%</td>
<td>21.7%</td>
<td>22.4%</td>
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<tr>
<td>Net income attributable to owners of parent</td>
<td>115.2</td>
<td>79.0</td>
<td>84.0</td>
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<tr>
<td>Net income per share (Yen)</td>
<td>702.26</td>
<td>481.48</td>
<td>511.96</td>
</tr>
</tbody>
</table>

* FPD: Flat Panel Display Production Equipment

Expect sales growth to exceed market growth, generating record high profits for second consecutive year.
### Current Progress with Medium-term Financial Targets

<table>
<thead>
<tr>
<th>WFE*</th>
<th>Market size</th>
<th>FY2015 (Actual)</th>
<th>FY2016 (Actual)</th>
<th>FY2017 (Actual)</th>
<th>FY2018 (Estimate)</th>
<th>Medium-term financial targets</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$31.9B</td>
<td>$31.4B</td>
<td>$35B</td>
<td>$38B</td>
<td>$30B</td>
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<tr>
<td>Net sales</td>
<td></td>
<td>¥613.1B</td>
<td>¥663.9B</td>
<td>¥799.7B</td>
<td>¥980.0B</td>
<td>¥720.0B</td>
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<tr>
<td>Operating margin</td>
<td></td>
<td>14.4%</td>
<td>17.6%</td>
<td>19.5%</td>
<td>22.0%</td>
<td>20%</td>
</tr>
<tr>
<td>ROE</td>
<td></td>
<td>11.8%</td>
<td>13.0%</td>
<td>19.1%</td>
<td>-</td>
<td>15%</td>
</tr>
</tbody>
</table>

*WFE (Wafer Fab Equipment): The semiconductor production process can be divided into two sequential sub-processes: front-end (wafer fabrication) and back-end (assembly and test) production. WFE is used in the front-end production process. Equipment for wafer-level packaging is not included in the WFE market size here.

**Steady improvement in results.**

**Continue to focus on improving profit margins**
Outperform the Market

- Continue to achieve earnings increases greater than market growth

  FY2017 results (compared to FY2016)
  ⇒ TEL sales growth +20.4% (WFE market growth* +11.5%)
  Operating income growth +33.3%

  FY2018 plan (compared to FY2017)
  ⇒ TEL sales growth +22.5% (WFE market growth* +8.6%)
  Operating income growth +38.7%

- Expand market share for etching system, thermal processing system, and cleaning system

  * WFE market growth rates are for the calendar year
Era of IoT

The amount of data is dramatically increasing with the growing number of connected devices
Infrastructure Evolution Supporting the IoT Era

5G Network

Compared to 4G: Speed: 100x
Data latency: 1/50th
# of connectable devices: 100x

5G, the next generation communications standard, will establish the infrastructure for an IoT society
The Evolution of Society

Real time systems will be built on society’s cloud systems

Semiconductors will be increasingly integrated throughout society
Expansion of WFE Market

Equipment for wafer-level packaging is not included in the WFE market size here

Semiconductor industry is heading for its next growth phase

Source: 2001-2013 SEMI
Growing Use of Displays as Interface Devices

Functionalities sought in displays:
ultra-high resolution • large scaled • low power consumption • flexibility

Further growth expected in the display market
## New Medium-term Financial Targets (toward FY2020)

Equipment for wafer-level packaging is included in the WFE market size here.

<table>
<thead>
<tr>
<th>WFE Market size</th>
<th>$42B</th>
<th>$45B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Net sales</td>
<td>¥1,050B</td>
<td>¥1,200B</td>
</tr>
<tr>
<td>Operating margin</td>
<td>24%</td>
<td>26%</td>
</tr>
<tr>
<td>ROE (Return on Equity)</td>
<td>20-25%</td>
<td></td>
</tr>
</tbody>
</table>

Targets adjusted due to changes in market conditions.
New Organization: Development & Production Group  
As of June 1, 2017

- Improve development flexibility as we enter new growth phase
- Merge Yamanashi and Tohoku plants, establish TTS*  
  - Combine technology and increase efficiency
  - Move process integration functions to plants, accelerate commercialization
- Technology Strategy Division to advance future technologies/technological integration focused on the IoT era

* TTS: Tokyo Electron Technology Solutions Ltd.
Miyagi Plant: New Development/Logistics Buildings

New development building: construction scheduled for completion by the end of August, 2018

Create and optimize customer value through joint R&D with customers, R&D integration, and continued improvement

Tokyo Electron Miyagi Ltd.
New development building and logistics building
Summary

- **Semiconductors and FPDs entering a new growth phase**
  - Revised WFE market outlook and financial targets (market outlook of $42B-$45B)

- **Optimize R&D structure to adapt to future business environment**
  - Establish five development divisions, ensure a flexible development structure
  - Establish TTS to strengthen deposition business (technology integration/efficiency)
  - Move Process Integration Center to TTS, accelerate product development

- **Expand etching business to respond to further growth**
  - Increase production, improve efficiency by constructing logistics building
  - Accelerate development of added-value products by constructing new development building
SPE R&D Strategy

Sadao Sasaki
Representative Director, Executive Vice President & General Manager, Development & Production Division
Contents

- Growing demand for leading-edge technology: Opportunities for TEL
  - TEL Technology Vision 2030

- R&D strategy progress
  - Demand for leading-edge technology and TEL R&D strategy
  - Unifying development to integrate TEL proprietary technologies

- Medium-term plan: Progress on business focus areas (Etching, Deposition, Cleaning Systems)
Growing Demand for Leading-edge Technology: Opportunities for TEL
TEL Technology Vision 2030
Energize discussion of future technologies achievable by 2030 and TEL’s contribution to these
Rapid growth in semiconductor applications in a range of areas, more sophisticated technology requirements.
TEL technology contributes to the evolution of semiconductors, the importance of which is growing in all industries.
R&D Strategy Progress
Demand for Leading-edge Technology and TEL Strategy

**3D NAND**
- Enhance multi-layering & production capacity
  - High selectivity process
  - Pursue further process accuracy and improve productivity

**DRAM**
- Deliver 1X miniaturization
  - Improve capacitor performance to further increase storage
  - Apply high aspect ratio etching and new materials

**Logic**
- Develop leading-edge 5 & 3nm
  - Develop patterning technology for scaling
  - Develop new materials, selective deposition

Pursue internal and external collaboration to accelerate development of innovative integrated technologies (process solution development, next-generation platform development)
Increase R&D Spend (R&D Investment in Focus Areas)

¥94.0B

Active investment in creating further integrated technologies and growth areas

FY18(E)

SPE business

Cross-BU development and collaboration
Other businesses: development of fundamental technologies

New product/technology R&D investment

Cross-BU R&D investment

FY13 FY14 FY15 FY16 FY17
(Billion Yen)

<table>
<thead>
<tr>
<th>Year</th>
<th>R&amp;D Spend (Billion Yen)</th>
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</thead>
<tbody>
<tr>
<td>FY13</td>
<td>73.2</td>
</tr>
<tr>
<td>FY14</td>
<td>78.6</td>
</tr>
<tr>
<td>FY15</td>
<td>71.3</td>
</tr>
<tr>
<td>FY16</td>
<td>76.2</td>
</tr>
<tr>
<td>FY17</td>
<td>83.8</td>
</tr>
</tbody>
</table>

Increase R&D Spend (R&D Investment in Focus Areas)

Actively invest in creating further integrated technologies and growth areas

FY18 (Estimated)
Establish self-aligned patterning technologies with multiple major customers

Advance R&D in close communication with customers
Expand on-site evaluation

Collaborate with leading-edge consortia and equipment/materials manufacturers
imec, SRC, AIST, simulation tool vendors, etc.

Enhance internal evaluation/R&D facilities

Established Process Integration Center
R&D by function at three facilities (TTCA***, Koshi, Hosaka)

* EPE: Edge placement error
** CDU: Critical dimension uniformity
*** TTCA: TEL Technology Center, America
**3D NAND Key Process Technologies and TEL’s Solutions**

**Plasma dry etch**
- Word line isolation
- Channel hole
- Multi-level contact

**Chemical dry etch**
- Source line pre-clean

**Wet etch**
- Replacement word line

**Wet clean**
- Bevel clean

**Single wafer deposition**
- Word line barrier
- Multi-level contact barrier
- Source line barrier

**Lithography**
- Word line isolation
- Channel hole
- Multi-level contact
- Staircase

**Thermal process (batch deposition)**
- Block oxide (high-k)
- Charge trap (ALD SiN)
- Channel Si
- Cap Si

**Atomic layer deposition**
- Core oxide

**Lithography**
- Word line isolation
- Channel hole
- Multi-level contact
- Staircase

**Thermal process (batch deposition)**
- Block oxide (high-k)
- Charge trap (ALD SiN)
- Channel Si
- Cap Si

**Atomic layer deposition**
- Core oxide

**CELLESTA™-i**

**CLEAN TRACK™ LITHIUS Pro™ Z**

**EXPEDEUS™+i**

**TELINDY PLUS™**

**Certas™**

**NT333™**

**Trias™+**

**Tactras™**

**3D NAND Key Process Technologies and TEL’s Solutions**

**CORP IR / May 31, 2017**
Expanding Business Opportunities in the 3D NAND Market

2D miniaturization

3D NAND stacking

Equipment ratio for previous NAND capex :

- Lithography
- Coating/developing
- Cleaning
- Deposition
- Others
- Etching < 15%

Equipment ratio for 3D NAND:

- Deposition
- Etching > 50%

Multi-layering, high A/R:
- Increase in number of layers etched
- Pursuit of high process accuracy decreases productivity
  ⇒ More equipment units needed

* TEL estimate
CORP IR / May 31, 2017
SPE Business Strategy: Strengthen Deposition Technology R&D

- **Establish Tokyo Electron Technology Solutions**
  - Unify development resources by merging Tokyo Electron Yamanashi and Tokyo Electron Tohoku

- **Established Process Integration Center (PIC)**
  - Cross-BU process module development

- **Develop next-generation platform**
  - Incorporate new controllers (AI software)
SPE Business Strategy: Deposition Systems

ALD system
NT333™

Thermal processing system
TELINDY PLUS™

Single wafer deposition system
Triase+™

Sputtering system for next-generation devices
EXIM™

Atomic layer deposition
¥111B

Oxidation/diffusion CVD (batch)
¥120B

Metallization (Ti/TiN)
¥30B

MRAM deposition

Aim to expand earnings based on new technologies for further miniaturization, new structures, and next-generation semiconductors

* Figures reflect TAM estimated by TEL
SPE Business Strategy: Cleaning Systems

- Expand sales of CELLESTA™ single wafer cleaning system
  - Expand applications based on backside and bevel cleaning* and drying technology that prevents pattern collapse during the post-etch cleaning processes

- Secure key 3D NAND processes through batch cleaning
  - Provide high quality and productivity in the metal etching, polysilicon etching, and nitride film removal processes required for precise controllability

- Apply best known coater/developers methods to cleaning system business
  - Share leading-edge technology and expertise by unifying R&D

<table>
<thead>
<tr>
<th>Market share</th>
<th>CY14 (Actual)</th>
<th>CY15 (Actual)</th>
<th>CY16 (Actual)</th>
<th>CY19 (Target)</th>
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</thead>
<tbody>
<tr>
<td>Cleaning system</td>
<td>19%</td>
<td>18%</td>
<td>20%</td>
<td>&gt;24%</td>
</tr>
</tbody>
</table>

* Bevel cleaning: process for removing film from the outer part of the wafer
Summary

- Formulated TEL Technology Vision 2030 to facilitate further business growth
  - Capture growth from diversifying semiconductor demand

- Aim for growth through strategic advancement of collaborations with customers and consortia, further strengthening of existing products, and cross-BU synergistic effects
  - Advance patterning solution R&D
  - Integrate technologies (3D NAND development solutions, integrate deposition facilities)

- Strengthen business through strategic investment in focus areas
  - Deposition business: speed up new product development through selection and concentration
  - Cleaning business: enhance products and improve market share by applying best known coater/developers methods
Corporate Development Strategy: Growth Opportunities through Integration

Akihisa Sekiguchi, PhD
Vice President & General Manager
Advanced Semiconductor Technology Division
Contents

- Device roadmap and issues in integration
  - Memory technology roadmap: DRAM, 3D NAND
  - Logic technology roadmap: FEOL, MOL, BEOL

- The importance of Process Integration Center (PIC) within our worldwide R&D
Device Evolution

3D structure

Planar

FinFET

High A/R DRAM

3D NAND

Nano-wire

resolution

wavelength

i-Line

KrF

ArF

immersion

scaling


180 130 110 90 65 45 32 22 14 10 7 5
Device Roadmap and Issues in Integration

**Memory:** DRAM, 3D NAND

**Logic:** FEOL, MOL, BEOL
<table>
<thead>
<tr>
<th>Node</th>
<th>2Y</th>
<th>1X</th>
<th>1Y</th>
<th>1Z</th>
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</thead>
<tbody>
<tr>
<td>Cell layout</td>
<td></td>
<td></td>
<td>6F²</td>
<td></td>
</tr>
<tr>
<td>Lithography</td>
<td></td>
<td>i-ArF</td>
<td>EUV</td>
<td></td>
</tr>
<tr>
<td>Cell transistor</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Structure</td>
<td></td>
<td></td>
<td>Buried WL, FinFET</td>
<td></td>
</tr>
<tr>
<td>Material</td>
<td></td>
<td></td>
<td>W/TiN/SiON</td>
<td></td>
</tr>
<tr>
<td>Cell capacitor</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Structure</td>
<td></td>
<td></td>
<td>Cylinder structure</td>
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</tr>
<tr>
<td>Material</td>
<td></td>
<td></td>
<td>TiN/ZAZ/TiN</td>
<td></td>
</tr>
</tbody>
</table>

Difficulty level of scaling has risen beyond 1Y
DRAM Challenge

**Dry etching**
- High aspect ratio capacitor (HARC) hole formation
- High selectivity etch (for insulator etch)

**Film deposition**
- High selectivity hard mask (for insulator etch)
- Conformal & low leakage insulator for capacitor
- Conformal & low resistance electrode for capacitor

**Cleaning/wet etching**
- Prevention of pattern collapse
- High aspect ratio structure cleaning

Challenges involving high aspect ratio structures dominate
## 3D NAND Roadmap

<table>
<thead>
<tr>
<th>Layer</th>
<th>48 layers</th>
<th>64 layers</th>
<th>96 layers</th>
<th>128 layers</th>
<th>&gt; 128 layers</th>
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</thead>
<tbody>
<tr>
<td>ONON stack</td>
<td>ONON</td>
<td>ONON</td>
<td>ONON</td>
<td>ONON</td>
<td>ONON</td>
</tr>
<tr>
<td>O-SiO₂ N-SiN</td>
<td>ONON</td>
<td>ONON</td>
<td>ONON</td>
<td>ONON</td>
<td>ONON</td>
</tr>
<tr>
<td>Adjacent CMOS circuit &amp; memory cell layout</td>
<td>ONON film stack optimization</td>
<td>ONON film stack optimization</td>
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<td>ONON film stack optimization</td>
<td>ONON film stack optimization</td>
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<tr>
<td>OPOP stack</td>
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<tr>
<td>O-SiO₂ P-Poly-Si</td>
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<tr>
<td>OPOP film stack optimization/Memory cell on CMOS (cell on CMOS)</td>
<td>OPOP film stack optimization/Memory cell on CMOS (cell on CMOS)</td>
<td>OPOP film stack optimization/Memory cell on CMOS (cell on CMOS)</td>
<td>OPOP film stack optimization/Memory cell on CMOS (cell on CMOS)</td>
<td>OPOP film stack optimization/Memory cell on CMOS (cell on CMOS)</td>
<td></td>
</tr>
</tbody>
</table>

Increasing layers drives high aspect ratio and process challenges

- Charge trap structure
- Floating gate structure
- Adjacent CMOS circuit & memory cell layout
- ONON film stack optimization
- OPOP film stack optimization/Memory cell on CMOS (cell on CMOS)

Vertical gate NAND 3D ReRAM Stack
Triple level ⇒ Quad level cell

> 128 layers

96 layers

64 layers

48 layers
3D NAND Challenges

**Dry etch**
- High aspect ratio etch
- High selectivity (versus stack films)

**Depositon**
- Reduction of ONON/OPOP stack warpage
- High selectivity hardmask
- Conformal functional film for flash
- High mobility channel
- Metal gate

**Clean/wet etch**
- Removal of nitride films in 3D structures

**Hardware**
- Handling warped wafers

Etch and deposition of films for high aspect ratio structures challenging
Device Roadmap and Issues in Integration

Memory: DRAM, 3D NAND
Logic: FEOL, MOL, BEOL
# FEOL Roadmap

<table>
<thead>
<tr>
<th>Node</th>
<th>16-14 nm</th>
<th>10 nm</th>
<th>7 nm</th>
<th>5 nm</th>
<th>&lt; 3.5 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Transistor structure</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Reducing short channel effect</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Channel material</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Higher mobility</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

- **FinFET**
- **Lateral nanowire**
- **Vertical nanowire**

**Reducing short channel effect**
- Higher mobility

**Structural changes in transistor concurrent with scaling**
FEOL Challenges

- Short channel effect control (on/off ratio)
  - New structure

- Channel mobility
  - New channel material

- Parasitic resistance reduction
  - Source/Drain activation enhancement
  - Low resistance silicide

- Parasitic capacitance reduction
  - Low dielectric constant material

- Variability reduction
  - Chamber matching, physical dimension control

Changes in transistor structure leading to changes in device performance
## MOL Roadmap

<table>
<thead>
<tr>
<th>Node</th>
<th>16-14 nm</th>
<th>10 nm</th>
<th>7 nm</th>
<th>5 nm</th>
<th>&lt; 3.5 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source/Drain shape</td>
<td>Diamond epi</td>
<td>Contact</td>
<td>Wrap around contact</td>
<td>Contact</td>
<td></td>
</tr>
<tr>
<td>Contact scheme</td>
<td>Self aligned contact</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact metal</td>
<td>W</td>
<td>W</td>
<td>Co</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Scaling, overlay, and contact resistance increase are issues
MOL Challenges

- Parasitic resistance
  - New structure, lower resistance material needed for reduction

- Narrow trench gap fill
  - High aspect ratio structure gapfill

- Overlay
  - Self aligned process

- Variability
  - Chamber matching

Scaling causes problems such as contact resistance increase
**BEOL Roadmap**

<table>
<thead>
<tr>
<th>Node</th>
<th>16-14 nm</th>
<th>10 nm</th>
<th>7 nm</th>
<th>5 nm</th>
<th>&lt; 3.5 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wiring formation scheme</td>
<td>Dual damascene</td>
<td>Self aligned via (SAV)</td>
<td>Self aligned via formation</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Non SAV</td>
<td>SAV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal wiring</td>
<td>Cu : ECD Ta/TaN PVD</td>
<td>Cu alternatives Ru, Co, CoAl</td>
<td>Post Cu</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Estimated using IEDM, VL, IITC papers

Scaling & overlay issues leading to evaluation of new integration schemes
BEOL Challenges

- Low resistance
  - Cu: thinner barrier layer
  - Cu alternatives: Ru, Co, CoAl,

- Parasitic capacitance reduction
  - Low dielectric constant film, air gap
  - Etch damage reduction: low temp etch, replacement schemes
  - Lower dielectric constant etch stop layer

- Narrow trench gap fill
  - Liner layer, alternative metals

- Overlay
  - Self aligned process

- Reliability (migration etc.)
  - Wiring cap layers

Migration period from Cu to other metals, parasitic capacitance still an issue
Importance of Process Integration Center (PIC) in the Context of Worldwide Development
Global Development Locations

imec (Belgium)

CEA-Leti (France)

Taiwan

Korea

Japan

United States

Albany NanoTech

TEL Technology Center Korea

TEL Technology Center, Taiwan

TEL Technology Center, America

IME (Singapore)

TEL Technology Solutions Process Integration Center (PIC)

Tokyo Electron Kyushu

Tokyo Electron Miyagi

Worldwide development accelerated due to strengthening of PIC function
Process Integration Center (PIC) Mission

- Expand business through collaboration with customers
- Add value to TEL products by synchronizing product development and PIC solutions
- Develop competitive solutions in advance in order to make solid proposals based on proven solutions
- Support overall TEL development by making sample wafers with high quality and short lead time, and by providing insights with knowledgeable analysis

Higher level technical collaboration with partners
Process Integration Center (PIC) Function

**Process tools**

- **Clean**
  - CELLESTA™
  - CLEAN TRACK™
  - LITHIUS Pro™ Z

- **Etch**
  - Tactras™ Vigus™
  - Certas™

- **Deposition**
  - TELINDY PLUS™
  - NT333™

**Analytical tools**

- **Analysis and measurement**
  - (Particle, ellipsometer, XRF, overlay)

- **Cross sectional analysis**
  - (SEM, STEM, FIB, others)

- **Surface analysis**
  - (TXRF, XPS, XRD, AFM, others)

Faster development by centralizing process and analytical tools
Summary

- How to plan ahead and develop new tools based on device evolution is key
- The success of the Patterning Solutions Project has led to the kickoff of Process Integration Center (PIC). It expands on the scope of activities beyond just patterning
- Enhancement of the worldwide development organization by strengthening PIC will lead to TEL’s competitiveness
- Continue to create technology innovation through close collaboration with our customers and partners
Etching System: Business Strategies

Yoshinobu Mitano
Vice President & General Manager, ES BU
**Etching System Market Outlook**

3D NAND driving 70% growth in etching system market from CY15 to CY19

**Etching system market by application**

- Significant NAND market expansion
- NAND
- DRAM
- Logic, other

**Overall WFE market +25% on CY15**

**Etching system market +70% on CY15**

TEL estimates (new equipment only)
3D NAND Business Opportunities

Ratio of etching systems in NAND

<table>
<thead>
<tr>
<th>CY12-14</th>
<th>CY19</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etching systems 15%</td>
<td>Etching systems 50%</td>
</tr>
<tr>
<td>Other systems 85%</td>
<td>Other systems 50%</td>
</tr>
</tbody>
</table>

Increase in 3D NAND HARC* processes (Greenfield, TEL estimates)

<table>
<thead>
<tr>
<th>Investment per 10k/wspm** ($M)</th>
<th>6X</th>
<th>9X</th>
<th>12X</th>
</tr>
</thead>
<tbody>
<tr>
<td>HARC processes (multi-level contact/word line isolation/channel)</td>
<td>30</td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>Other etching processes</td>
<td>80</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td>Etching process total</td>
<td>110</td>
<td>120</td>
<td>130</td>
</tr>
</tbody>
</table>

3D NAND HARC* processes

<table>
<thead>
<tr>
<th>CY17</th>
<th>CY18</th>
<th>CY19</th>
</tr>
</thead>
<tbody>
<tr>
<td>6X</td>
<td>6X/9X</td>
<td>9X</td>
</tr>
</tbody>
</table>

Expand HARC processes by increasing number of stacked layers

* HARC (High aspect ratio contact) process: a process for forming holes that requires advanced processing technology
** wspm: wafer starts per month
3D NAND: Approach and Results

- Maintained a 100% share of the multi-level contact processes. Plan to further increase revenues by integrating mask process to improve productivity.
- Captured new customer PORs with 9X generation word line isolation. Aim to increase our position by integrating mask process.
- Realize the capture of channel processes through new technology.

Expand our position by dramatically improving profile and productivity.
Logic: Approach and Results

- Maintained high interconnecting dielectric etching process market share
- Aim to expanded advanced patterning applications

RLSA™ plasma source

Plasma etch systems Tactras™ RLSA™

Realize high selectivity through low electron temperature plasma

ALE concept process

Achieve high-level of control over dimension variation

Aim to increase sales by differentiating our technology in 7nm and finer advanced patterning
DRAM: Approach and Results

- Captured BEOL processes by leveraging expertise in logic through our strength in damascene processes
- Captured development PORs with all customers using 1Y generation capacitor process (HARC)
- Realized reduced patterning costs for customers by combining etching steps. Currently using successes with strategic customers to expand market share in other customers

Currently achieving success in all DRAM focus processes in line with plan
Action to Increase Profitability

- New products focused on the high-end market
  ➔ Active capex in R&D
- Reduce customer support expenses through products with improved added-value
- Optimize logistics
- Further reduce fixed cost ratio

Plan to raise sales and profits through technological differentiation and improving production efficiency
Summary

- Expect significant expansion of etching system market driven by 3D NAND and patterning
- We are enhancing our positions in logic and memory focus areas
- Actively investing in R&D in response to further market expansion
- Focus on HARC, patterning, and BEOL processes that utilize our strengths. Aim to raise profitability by increasing market share to over 30% by CY19

<table>
<thead>
<tr>
<th>Market share</th>
<th>CY14 (Actual)</th>
<th>CY15 (Actual)</th>
<th>CY16 (Actual)</th>
<th>CY19 (Target)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etching system</td>
<td>28%</td>
<td>21%</td>
<td>23%</td>
<td>&gt;30%</td>
</tr>
</tbody>
</table>
FPD Business Strategy

Tsuguhiko Matsuura
Vice President & General Manager, FPD BU
Display Trends

Technology inflection creates greater business opportunities

<table>
<thead>
<tr>
<th>Increasing screen size</th>
<th>Increasing resolution</th>
<th>Design flexibility</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OLED</strong></td>
<td><strong>LCD</strong> ---&gt; <strong>OLED</strong></td>
<td>Flexible, edge bent, free format</td>
</tr>
<tr>
<td>Color filter</td>
<td>LCD</td>
<td>TFT</td>
</tr>
<tr>
<td>TFT</td>
<td>Backlight</td>
<td></td>
</tr>
<tr>
<td>TV</td>
<td>FHD</td>
<td>4K</td>
</tr>
<tr>
<td>Smartphones</td>
<td>300 ppi</td>
<td>700 ppi</td>
</tr>
</tbody>
</table>

CORP IR / May 31, 2017
FPD Business Medium-term Plan

- Increase share and profitability in market that has begun to grow again
- FY2020 target: sales ¥80.0B, operating margin over 20%
Medium-term Plan Progress: Highlights

- TEL’s product strategy for a new PICP™ etching system is progressing according to plan
- Expanding the G10.5 equipment business

<table>
<thead>
<tr>
<th></th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
<th>2018</th>
<th>2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>G10.5</td>
<td></td>
<td></td>
<td>Coater/developers and etching system</td>
<td></td>
<td></td>
</tr>
<tr>
<td>G8.5</td>
<td></td>
<td></td>
<td>PICP etching system for large-sized panels</td>
<td></td>
<td></td>
</tr>
<tr>
<td>G6</td>
<td></td>
<td></td>
<td>PICP etching system for small- and medium-sized panels</td>
<td>New Betelex™ platform</td>
<td>OLED process (G6H)</td>
</tr>
</tbody>
</table>

Higher profitability for all panel generations

* PICP: Plasma source for producing extremely uniform high density plasma on substrate
Opportunity – G10.5 Equipment Market

- Greater than expected investment and market expansion
- Maintain high market share through technological differentiation (large area plasma suppression, air floating coater)

> Eight 65 inch TV panel substrate possible

---

Results based on IHS Markit, Technology Group “Display Supply Demand & Equipment Tracker, Q1 2017”. Results are not an endorsement of Tokyo Electron. Any reliance on these results is at the third party’s own risk. Visit technology.ihs.com for more details.

CORP IR / May 31, 2017
## Opportunity – Metal Oxide/LTPS

- Higher sophistication of etching technology and increased number of processes

<table>
<thead>
<tr>
<th>TFT</th>
<th>a-Si</th>
<th>Metal oxide</th>
<th>LTPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Representation of structure</td>
<td>![image]</td>
<td>![image]</td>
<td>![image]</td>
</tr>
<tr>
<td>Application</td>
<td>LCD TV Monitor</td>
<td>OLED TV Tablet</td>
<td>Smartphone (LCD/OLED)</td>
</tr>
<tr>
<td>Number of masks</td>
<td>5</td>
<td>6 - 8</td>
<td>9 - 13</td>
</tr>
<tr>
<td>Dry etch processes</td>
<td>3 a-Si, SiNx</td>
<td>3 SiO, SiNx</td>
<td>11 SiO, Metal</td>
</tr>
</tbody>
</table>

Further new needs:
- Flexible displays
  - +2 processes
- OLED process
  - (G6 half size)
  - +3-4 processes
Opportunity – Growth of OLED TV Market

- Introduced inkjet printing system to meet production demand from 2018
- Material utilization significantly more efficient than current evaporation method

Increase in OLED TV manufacturers

New manufacturers in Japan

Toshiba
  REGZA X910 series
  Launched March 2017

Sony
  BRAVIA A1
  To be launched June 2017

Panasonic
  VIERA TH-65EZ1000/EZ950 series
  To be launched June 2017

OLED TV area demand

Results based on IHS Markit, Technology Group “Display Supply Demand & Equipment Tracker, Q1 2017”. Results are not an endorsement of Tokyo Electron. Any reliance on these results is at the third party’s own risk. Visit technology.ihs.com for more details.
Summary

- Increase share and profitability in market that has begun to grow again
  Greater than expected business expansion
  FY2020 target: sales ¥80.0B, operating margin over 20%

- For leading-edge production process, focus on areas where we have technological superiority
  – High performance PICP etching system
  – G10.5 compatible etching system and coater/developers
  – Inkjet printing system for OLED TV
Financial Model

Tetsuro Hori
Representative Director, Executive Vice President & General Manager
Financial Model: Concept

- TEL is changing its financial model to match the larger scale of the semiconductor market

- Financial model: Change in WFE* market scale
  - In our financial model announced in 2015 we presented a range according to economic conditions (WFE $37B-$30B)
  - Our new financial model presents a forecast range for FY2020. We expect the WFE market to reach a size of $42B to $45B

* WFE (Wafer Fab Equipment): The semiconductor production process can be divided into two sequential sub-processes: front-end (wafer fabrication) and back-end (assembly and test) production. WFE is used in the front-end production process.
<table>
<thead>
<tr>
<th></th>
<th>FY2017 (Actual)</th>
<th>FY2018 (Estimate)</th>
<th>FY2020 (Medium-term plan)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>WFE $37B</td>
<td>WFE $40B</td>
<td>WFE $42B</td>
</tr>
<tr>
<td>Net sales</td>
<td>799.7</td>
<td>980.0</td>
<td>1,050.0</td>
</tr>
<tr>
<td>SPE</td>
<td>749.8</td>
<td>910.0</td>
<td>970.0</td>
</tr>
<tr>
<td>FPD</td>
<td>49.3</td>
<td>70.0</td>
<td>80.0</td>
</tr>
<tr>
<td>Gross profit</td>
<td>322.2</td>
<td>412.0</td>
<td>452.0</td>
</tr>
<tr>
<td>Gross profit margin</td>
<td>40.3%</td>
<td>42.0%</td>
<td>43.0%</td>
</tr>
<tr>
<td>SG&amp;A expenses</td>
<td>166.5</td>
<td>196.0</td>
<td>200.0</td>
</tr>
<tr>
<td>SG&amp;A expense ratio</td>
<td>20.8%</td>
<td>20.0%</td>
<td>19.0%</td>
</tr>
<tr>
<td>Operating income</td>
<td>155.6</td>
<td>216.0</td>
<td>252.0</td>
</tr>
<tr>
<td>Operating margin</td>
<td>19.5%</td>
<td>22.0%</td>
<td>24.0%</td>
</tr>
<tr>
<td>Net income attributable to owners of parent</td>
<td>115.2</td>
<td>163.0</td>
<td>180.0</td>
</tr>
</tbody>
</table>
SPE Sales (WFE $45B)

- TEL continues to plan for growth in sales above market growth

<table>
<thead>
<tr>
<th></th>
<th>FY2017 (Actual)</th>
<th>FY2018 (Estimate)</th>
<th>FY2020 (Medium-term plan)</th>
<th>Growth (FY17-FY20)</th>
</tr>
</thead>
<tbody>
<tr>
<td>WFE $37B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sales</td>
<td>749.8</td>
<td>910.0</td>
<td>1,120.0</td>
<td>+49%</td>
</tr>
<tr>
<td>New equipment</td>
<td>550.3</td>
<td>660.0</td>
<td>810.0</td>
<td>+47%</td>
</tr>
<tr>
<td>Field solutions</td>
<td>199.4</td>
<td>250.0</td>
<td>310.0</td>
<td>+55%</td>
</tr>
<tr>
<td>WFE $40B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WFE $45B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sales</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>New equipment</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Field solutions</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WFE +22%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Differentiate our technology in products and continue to win PORs
- Meet expanding demand for field solutions
FPD Sales

- Plan to expand sales based on differentiated technology and high-market-share products

<table>
<thead>
<tr>
<th></th>
<th>FY2017 (Actual)</th>
<th>FY2018 (Estimate)</th>
<th>FY2020 (Medium-term plan)</th>
<th>Growth (FY17-FY20)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sales</td>
<td>49.3</td>
<td>70.0</td>
<td>80.0</td>
<td>+62%</td>
</tr>
<tr>
<td>New equipment</td>
<td>40.5</td>
<td>60.0</td>
<td>70.0</td>
<td>+73%</td>
</tr>
<tr>
<td>Field solutions</td>
<td>8.8</td>
<td>10.0</td>
<td>10.0</td>
<td>+13%</td>
</tr>
</tbody>
</table>

- In OLED panels where high level technology is in demand, differentiate with cutting-edge PICP™* technology
- Further expand sales for G10.5, where TEL has a high market share
- Continue development of inkjet printing system for OLED TVs

* PICP: Plasma source for producing extremely uniform high density plasma on substrate
Gross Profit (WFE $45B)

- Gross profit margin: up 3.2pts

<table>
<thead>
<tr>
<th></th>
<th>FY2017 (Actual)</th>
<th>FY2018 (Estimate)</th>
<th>FY2020 (Medium-term plan)</th>
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</tr>
</thead>
<tbody>
<tr>
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<td>412.0</td>
<td>522.0</td>
<td>+62%</td>
</tr>
<tr>
<td>Gross profit margin</td>
<td>40.3%</td>
<td>42.0%</td>
<td>43.5%</td>
<td>+3.2pts</td>
</tr>
</tbody>
</table>

- Raise marginal profit ratio of core SPE products
  - Timely introduction of new products to an expanding market
  - Lower cost ratio through product quality improvements

- Raise marginal profit ratio of FPD production equipment
SG&A Expenses (WFE $45B)

- SG&A expense ratio: improve by 3.3pts

<table>
<thead>
<tr>
<th></th>
<th>FY2017 (Actual)</th>
<th>FY2018 (Estimate)</th>
<th>FY2020 (Medium-term plan)</th>
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<td>+26%</td>
</tr>
<tr>
<td>SG&amp;A expense ratio</td>
<td>20.8%</td>
<td>20.0%</td>
<td>17.5%</td>
<td>-3.3pts</td>
</tr>
</tbody>
</table>

- Cost reductions through integration of development units
  - Establish Tokyo Electron Technology Solutions Ltd.
  - Realized benefits of integration of Coater/Developers and Cleaning System business units

- Raise business productivity, control fixed costs
  - Improve business efficiency of service divisions
  - Control development expenses at level appropriate to balance with current profitability
R&D Expenses, Capex Plans

- Implement product development needed for growth, while raising efficiency and maintaining profits
- Capex (development + production facilities) to be limited to around ¥15.0B annually
Assets and Capital Efficiency (Sales ¥1,200B Model)

- Accounts receivable turnover
  - Current approx. 60 days: Appropriate

- Inventory turnover
  - Current 108 days → Target 95 days

- ROE
  - Current 19% → Target 20-25%

\[ \text{ROE} = \frac{\text{Net income attributable to owners of parent}}{\text{Average total equity}} \times 100\% \]
Medium-term Financial Targets (toward FY2020)

Aim for sustained growth in corporate value and continue to develop next-generation products while maintaining a global standard level of profitability.

<table>
<thead>
<tr>
<th><strong>WFE</strong></th>
<th><strong>Market size</strong></th>
<th>$42B</th>
<th>$45B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Net sales</td>
<td>¥1,050B</td>
<td>¥1,200B</td>
</tr>
<tr>
<td></td>
<td>Operating margin</td>
<td>24%</td>
<td>26%</td>
</tr>
<tr>
<td></td>
<td>ROE (Return on Equity)</td>
<td>20-25%</td>
<td></td>
</tr>
</tbody>
</table>

- WFE (Wafer fab equipment): The semiconductor production process can be divided into two sequential sub-processes: front-end (wafer fabrication) and back-end (assembly and test) production. WFE is used in the front-end production process. Front-end production equipment includes equipment for wafer-level packaging.
Capital Policy, Shareholder Returns

- Approach to capital policy
  - While closely monitoring the business environment and our necessary cash balance, we will strive to raise ROE through earnings maximization and asset turnover improvement to efficiently utilize shareholders equity

- Approach to shareholder policy
  - Business trends in our industry can be volatile and our policy is to link dividend payments to business performance
  - However, to assure stable returns to our shareholders, we will utilize our sound financial foundation to establish a minimum DPS payment

**Dividend payout ratio: 50%**

**Annual DPS of not less than ¥150**

We will review our policy if the company does not generate net income for 2 consecutive fiscal years

We will flexibly consider share buybacks
Summary

- Steadily work to achieve our FY2020 financial model
- Further strengthen product competitiveness, aim for sales growth greater than market growth
- Raise development efficiency and business productivity, further improve profitability

Pursue a global standard level of profitability, aim for sustained growth in corporate value
Field Solutions (FS) Business: Medium-term Plan

Increase earnings in both the used equipment/modification and parts/service segments through a business model that utilizes makers’ strengths

- Respond to new customer needs driven by IoT
  - Provide upgrades and remanufactured equipment that handle new applications
- Contribute to improving customer productivity
  - Provide added-value services using remote connections

(Installed base of 62,000 units)
SPE Business Strategy: Deposition System

Aim to expand earnings based on new technologies for further miniaturization and next-generation semiconductors

**ALD system**
- Achieve both high quality film formation and high productivity needed for miniaturization and for 3D structure with semi-batch system

**CVD system**
- Differentiate in memory through our clear lead in batch system productivity
- Achieve high quality metallization to enable further miniaturization

<table>
<thead>
<tr>
<th>Market share</th>
<th>CY14 (Actual)</th>
<th>CY15 (Actual)</th>
<th>CY16 (Actual)</th>
<th>CY19 (Target)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deposition system</td>
<td>38%</td>
<td>38%</td>
<td>37%</td>
<td>&gt;47%</td>
</tr>
</tbody>
</table>

Deposition System: Tube CVD + Atomic layer deposition tools + Oxidation/diffusion furnaces + Nontube LPCVD
### Adjustment to Share Results due to Product Recategorization
(etching system, cleaning system)

- From CY2016 dry cleaning systems have been recategorized under etching system, and actual shares for etching system and cleaning system for CY2014, CY2015 and CY2016 have been adjusted to reflect this.

<table>
<thead>
<tr>
<th>Market share</th>
<th>CY2014</th>
<th>CY2015</th>
<th>CY2016</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etching system</td>
<td>26%</td>
<td>19%</td>
<td>21%</td>
</tr>
<tr>
<td>Cleaning system (Including dry cleaning systems)</td>
<td>24%</td>
<td>23%</td>
<td>25%</td>
</tr>
</tbody>
</table>

Before adjustment

<table>
<thead>
<tr>
<th>Market share</th>
<th>CY2014</th>
<th>CY2015</th>
<th>CY2016</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etching system</td>
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<td>21%</td>
<td>23%</td>
</tr>
<tr>
<td>Cleaning system</td>
<td>19%</td>
<td>18%</td>
<td>20%</td>
</tr>
</tbody>
</table>

After adjustment

---

CORP IR / May 31, 2017
Disclaimer regarding forward-looking statement
Forecast of TEL's performance and future prospects and other sort of information published are made based on information available at the time of publication. Actual performance and results may differ significantly from the forecast described here due to changes in various external and internal factors, including the economic situation, semiconductor/FPD market conditions, intensification of sales competition, safety and product quality management, and intellectual property-related risks.

Processing of numbers
For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.

Exchange risk
In principle, export sales of Tokyo Electron’s mainstay semiconductor and FPD panel production equipment are denominated in yen. While some settlements are denominated in dollars, exchange risk is hedged as forward exchange contracts are made individually at the time of booking. Accordingly, the effect of exchange rates on profits is negligible.

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