TOKYO ELECTRON

Investors' Guide

November 9, 2026

Tokyo Electron Limited



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Updates

Slide Title	Updates
TEL's Growth	Updated with the latest data
Financial Performance: Sales and Operating Margin	Updated with the latest data
Semiconductor Manufacturing Process	Updated with the latest data
TEL Overview（P12～17）	New Slides: Equipment Overview
Outlook for the Semiconductor Market	Updated with the latest data
Business Environment and Financial Estimates	Updated with Q2 FY2027 earnings briefing presentation
DRAM Technology Roadmap (Generic)	Updated with the latest data
Appendix: Data Section	Updated with Q2 FY2027 results

1. TEL Overview

Company Profile

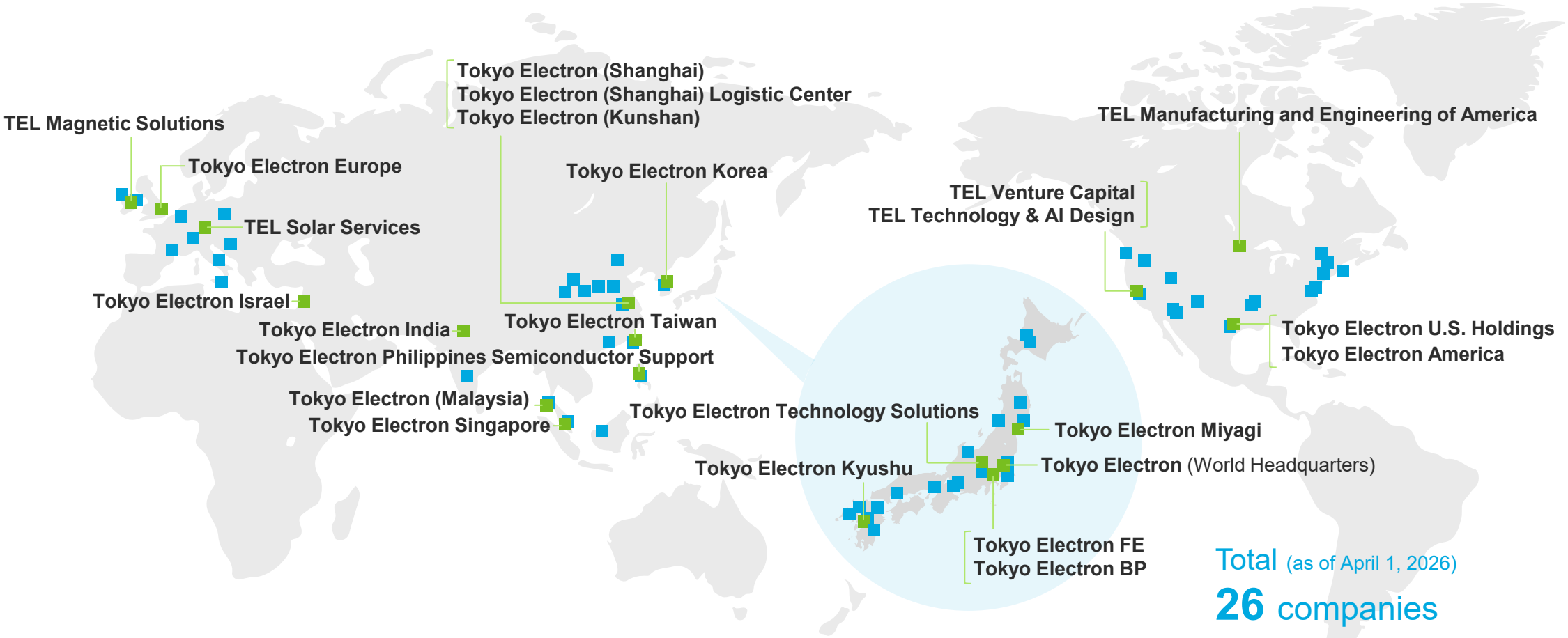
Established	November 11, 1963
Major Products and Services	Semiconductor Production Equipment
Capital	54.9 Billion Yen
Sales/Profit	Net sales 2,443.5 Billion Yen / Operating income 624.9 Billion Yen / Operating margin 25.6% (Fiscal 2026)
Number of Employees	2,436 (non-consolidated) 20,812 (consolidated) (as of April 1, 2026)
Global Network	Japan: 6 companies / 30 sites Overseas: 20 companies / 17 countries and regions / 72 sites Total: 26 companies / 18 countries and regions / 102 sites (consolidated) (as of April 1, 2026)



Source: TEL

Worldwide Operations

(As of Jul 1, 2026)



Total (as of April 1, 2026)

26 companies

18 countries and regions

102 sites

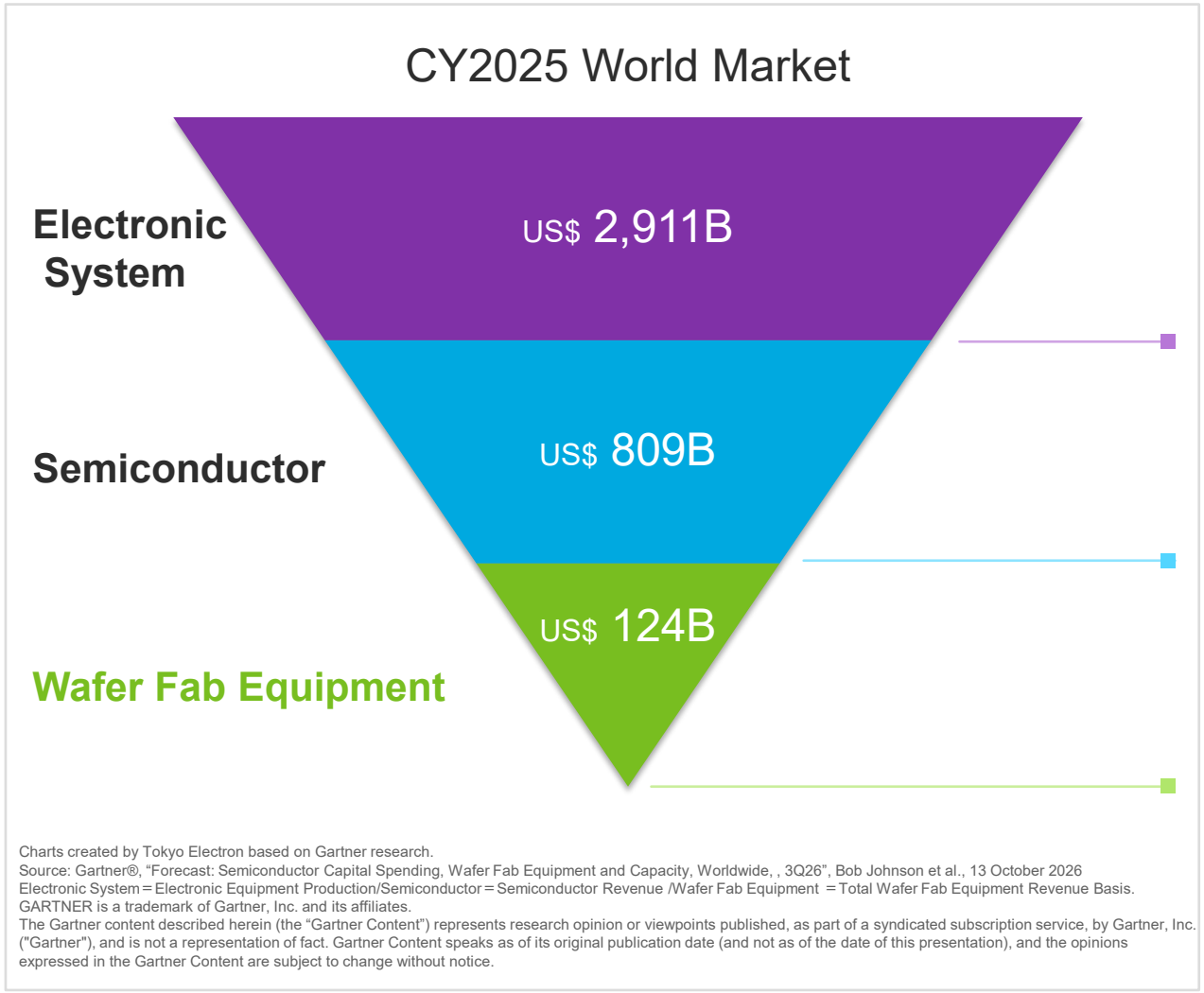
Source: TEL

- Head Office
- Branch, Office (including Field Service), Sales Office

*Group companies in the process of being wound up are not shown on the map.

The Market TEL Participates in

The market TEL participates in



Charts created by Tokyo Electron based on Gartner research.
Source: Gartner®, "Forecast: Semiconductor Capital Spending, Wafer Fab Equipment and Capacity, Worldwide, , 3Q26", Bob Johnson et al., 13 October 2026
Electronic System＝Electronic Equipment Production/Semiconductor＝Semiconductor Revenue /Wafer Fab Equipment ＝Total Wafer Fab Equipment Revenue Basis.
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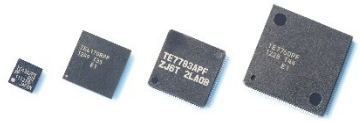
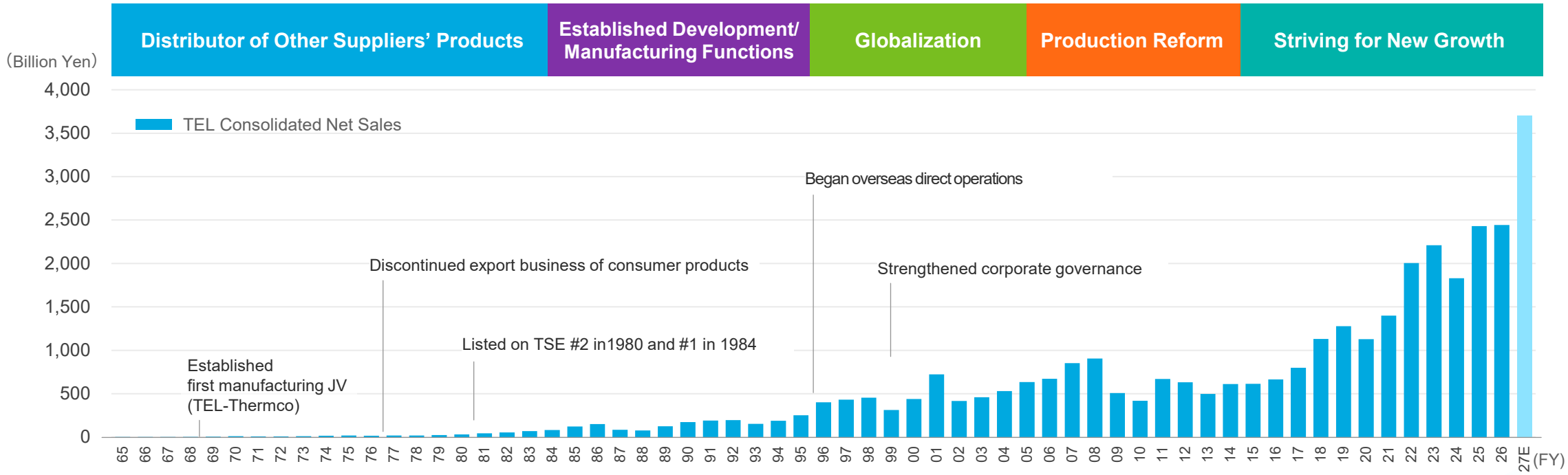
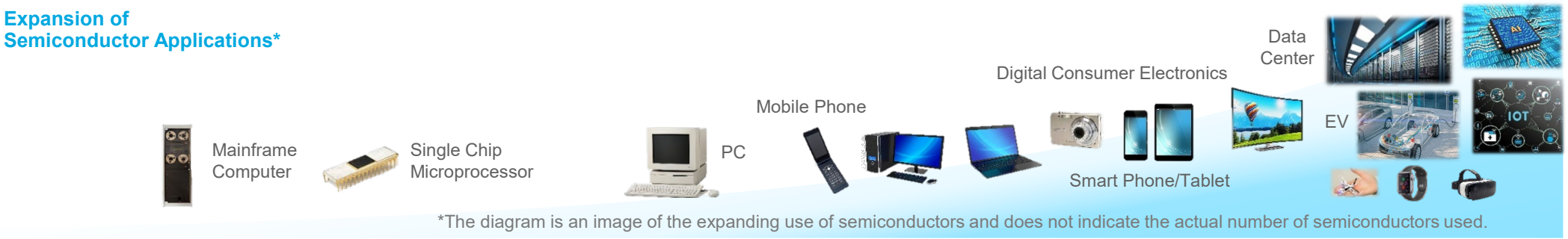




Source: Licensed Image

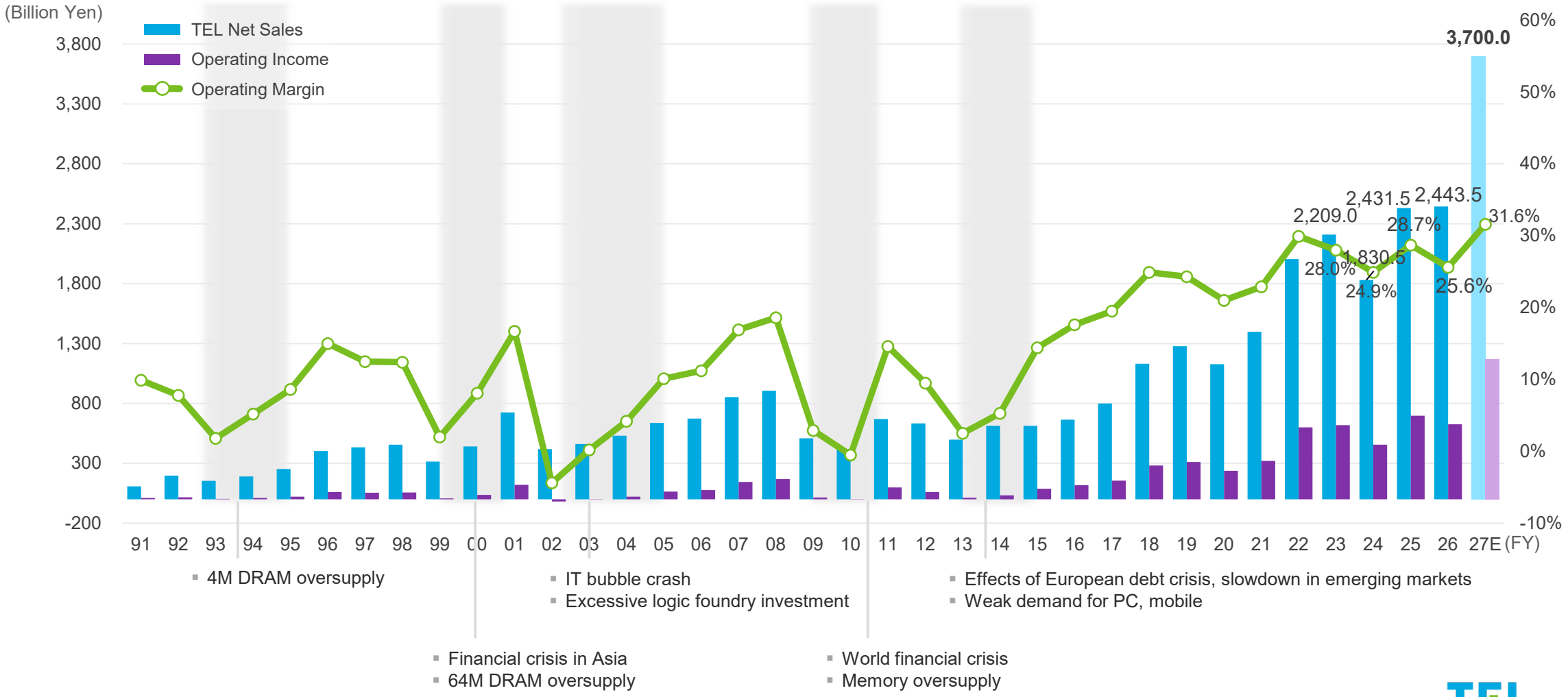
TEL's Growth





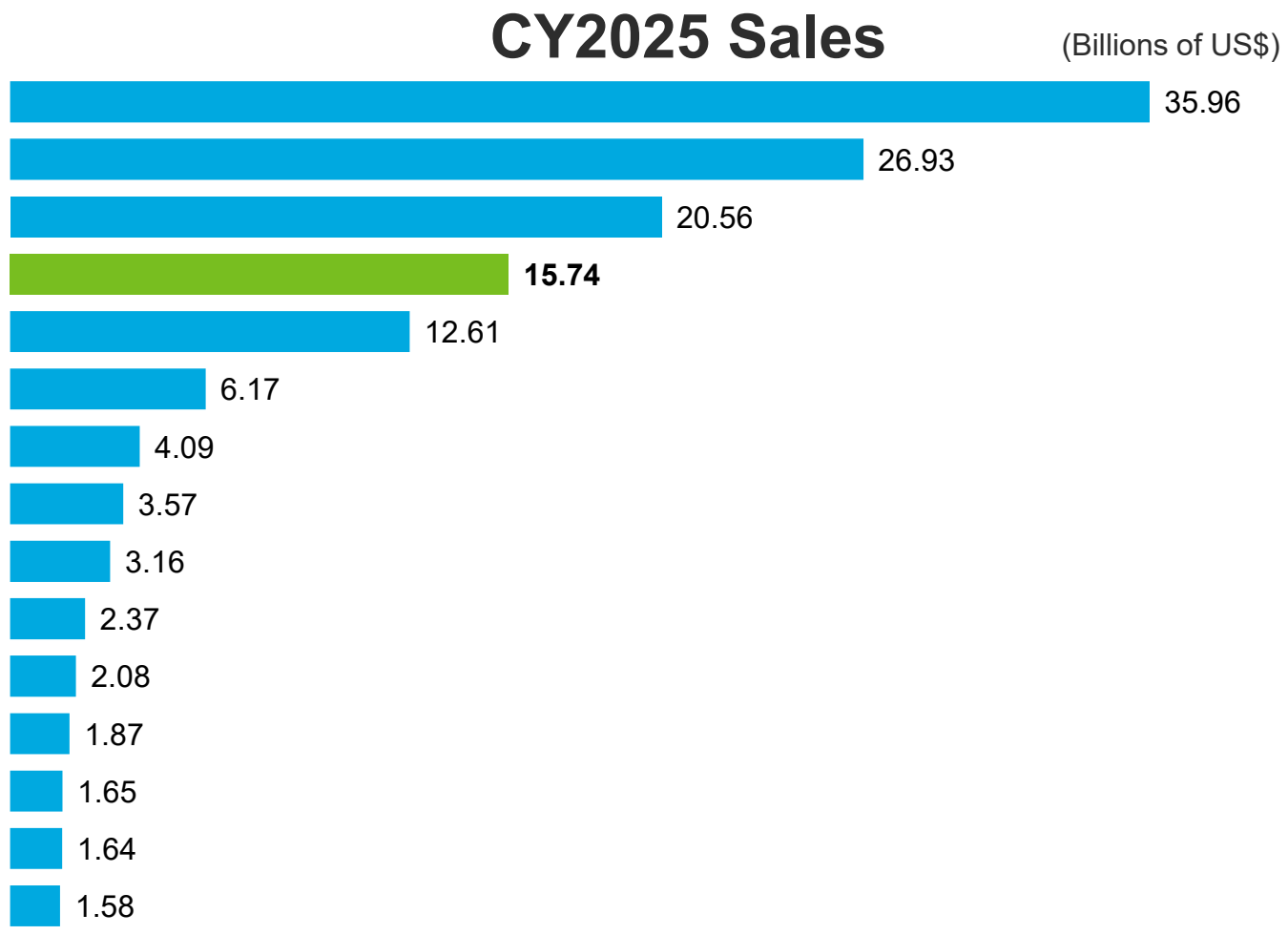
Source: Licensed Image

Financial Performance: Sales and Operating Margin



CY2025 SPE Makers Top 15

1	ASML	35.96
2	Applied Materials	26.93
3	Lam Research	20.56
4	**Tokyo Electron**	**15.74**
5	KLA	12.61
6	Advantest	6.17
7	NAURA	4.09
8	ASM International	3.57
9	SCREEN	3.16
10	Teradyne	2.37
11	DISCO	2.08
12	Hitachi High-Tech	1.87
13	AMEC	1.65
14	SEMES	1.64
15	KOKUSAI ELECTRIC	1.58



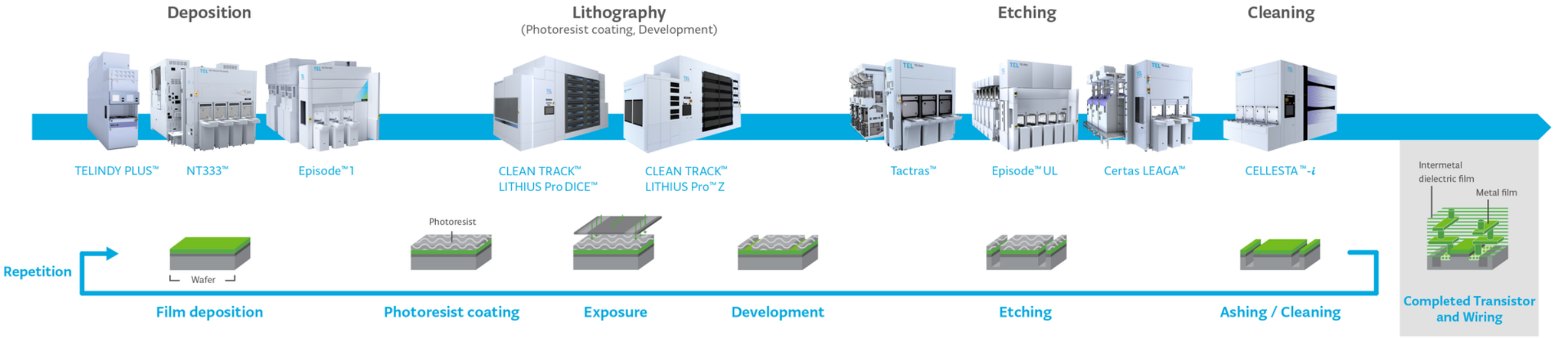
Source: Licensed Image

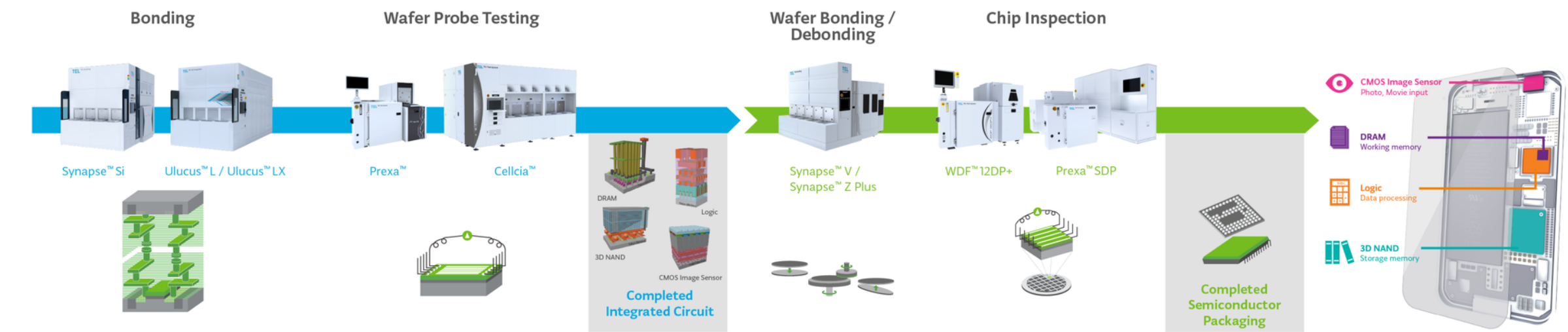
Source：TechInsights Inc., May 2026

Semiconductor Manufacturing Process

TELCBC-SMP-002

Wafer Process (Front-end)
Assembly and Test Process (Back-end)

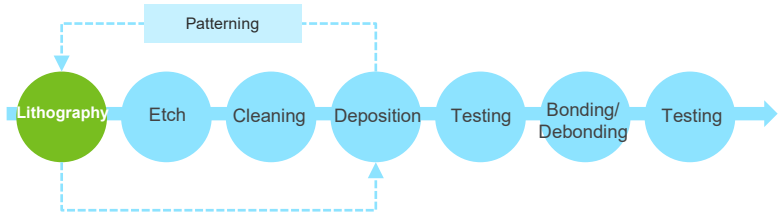




Lithography（Coater/Developer）

Lithography serves as the starting point of patterning that determines device dimensions and is a fundamental process for forming fine circuit patterns. A circuit pattern on a photomask is transferred onto a uniformly coated photoresist using a scanner, after which selected portions are dissolved and removed during development to form the resist pattern. Because coating, exposure, and development are typically performed continuously in an inline system, the coating/developing process requires high throughput, high reliability, and precise control.

TEL's Process Coverage



Major Manufacturers

Exposure Tool	Coater/Developer
ASML	**TEL**
CANON	Kingsemi
NICON	SCREEN
	SEMES

Lithography Systems: Primary Light Sources

- DUV (Deep Ultraviolet)
  - KrF: Broad range of applications
  - ArF Dry: Logic, DRAM, NAND
  - ArF Immersion: Logic, DRAM, NAND
- EUV (Extreme Ultraviolet):
  Leading-edge logic, DRAM
  →Widely adopted in leading-edge logic, expanding into DRAM

Main Products



CLEAN TRACK™ LITHIUS Pro DICE™
Coater/Developer

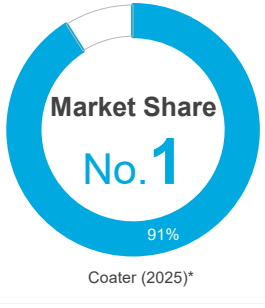


CLEAN TRACK™ LITHIUS Pro™ Z
Coater/Developer



CLEAN TRACK™ LITHIUS Pro™ AP
Coater/Developer

Manufacturing Base: Kumamoto



Coater (2025)*

FY2026 Sales Mix



Expected Items

- Evaluation of Ultimate Wet Development technologies for metal oxide resist ongoing with multiple customers
- Logic/memory: CLEAN TRACK™ LITHIUS Pro DICE™ for EUV/KrF applications (POR by multiple customers)

Source
* Gartner®, Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2025, Bob Johnson and Menglin Cao, 2 April 2026, Revenue from Shipments basis. Chart created by TEL based on Gartner research. Gartner research. Calculations performed by TEL.
Coater/Developer: Photoresist Processing (Track).
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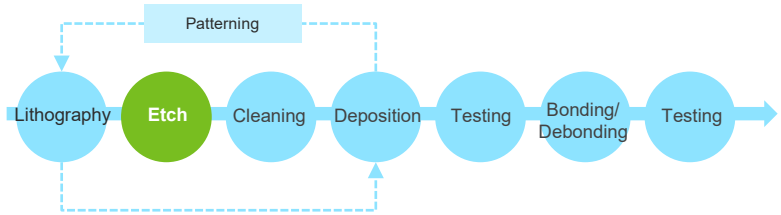
Etch

Etching transfers fine circuit patterns formed by lithography and selectively removes underlying films. As semiconductor devices scale, structures become more complex and target materials more diverse. Because EUV photoresists have low etch resistance, the etch process requires high selectivity and precise profile control. As technology advances, demands on etch systems continue to increase.

TEL's Process Coverage



Major Manufacturers

- **TEL**
- Lam Research
- Applied Materials
- NAURA
- AMEC

Primary Etch Methods

- Dry Etch (Plasma Etch)
- Wet Etch

Primary Etch Materials

- Dielectric Films
  SiO, SiN, low-k, SiON, SiCN
- Conductive Films
  Ti, W, Al, Co, Mo, Ta, Ru
- Silicon-Based Materials
  Si, Poly-Si, SiGe
- Organic Films
  Spin on carbon, amorphous carbon

Main Products



Episode™ UL
Plasma Etch System



Tactras™
Plasma Etch System



Certas LEAGA™
Gas Chemical Etch System

Manufacturing Base: Miyagi / Yamanashi



Dry Etch (2025)*

FY2026 Sales Mix



Expected Items

- Over 50% market share in dielectric etch
- DRAM: HBM interconnect etch (POR) / Capacitor (POR by all major customers)
- NAND: Slit (POR) / Channel hole (POR)
- Logic: TDV for advanced packaging (POR)

Source
* Gartner®, Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2025, Bob Johnson and Menglin Cao, 2 April 2026, Revenue from Shipments basis. Chart created by TEL based on Gartner research. Gartner research. Calculations performed by TEL.
Dry Etch System: Dry Etch

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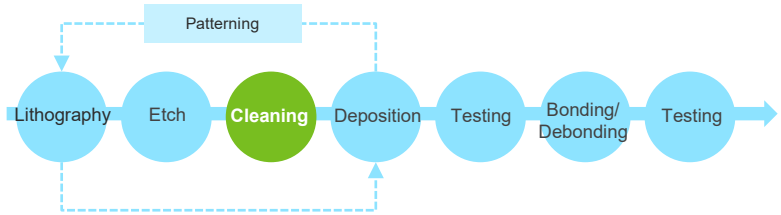
Cleaning

Cleaning is a critical process step performed between other process steps. It removes particles deposited on the circuit as well as by-products remaining on the surface after etching, thereby reducing defects. When etching creates fine structures, pattern collapse caused by surface tension during removal of the cleaning solution must also be prevented. Consequently, post-cleaning drying technology is equally important.

TEL's Process Coverage



Major Manufacturers

- TEL
- SCREEN
- Lam Research
- ACM Research
- SEMES

Primary Cleaning Methods

- Wet cleaning: chemicals and DI water

Major Cleaning Technologies

- Scrubber Cleaning: Removes particles and residues using brushes
- Bevel Cleaning: Removes contaminants from the wafer edge
- Supercritical Cleaning: Prevents pattern collapse while removing contaminants from fine structures

Main Products



CELLESTA™ -i MD
Single Wafer Cleaning System



EXPEDIUS™ -i
Auto Wet Station



NS300Z
Scrubber System

Manufacturing Base: Kumamoto



Clean Equipment(2025)*

FY2026 Sales Mix



Expected Items

- DRAM: Evaluation started with multiple customers for next generation super critical drying technology
- Logic/memory: Evaluation ongoing with multiple customers for resist stripping (one POR)
- Memory: Evaluation started for a hybrid batch and single-wafer system

Source
* Gartner®, Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2025, Bob Johnson and Menglin Cao, 2 April 2026, Revenue from Shipments basis. Chart created by TEL based on Gartner research. Gartner research. Calculations performed by TEL.
Cleaning System: Single Wafer Processors + Wet Stations + Batch Spray Processors + Scrubbers + Other Clean Equipment
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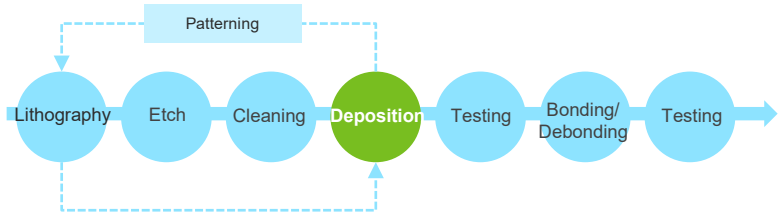
Deposition

Deposition is a core process for forming conductive materials that electrically connect devices on a wafer and insulating materials that isolate them. Film thicknesses range from several micrometers to several nanometers, with widely varying specifications. Recent requirements include the uniform deposition of materials with specified electrical properties at thicknesses of 1 to 10 nm over fine three-dimensional device structures. In addition, technologies for forming films with high resistance to dry-etching gases and wet-etching chemicals are also required.

TEL's Process Coverage



Major Manufacturers

- **TEL**
- ASM International
- Lam Research
- KOKUSAI ELECTRIC
- Applied Materials
- NAURA

Primary Deposition Methods

- CVD (Chemical Vapor Deposition)
- PVD (Physical Vapor Deposition)
- ALD (Atomic Layer Deposition)
- Oxide/Anneal

Materials for Deposition

- Dielectric Films

SiO_2, Si_3N_4 ,SiOC (low-k), HfO_2 (high-k)
Primary Technologies：CVD, PECVD, ALD

- Semiconductor Films

Si, SiC, GaN
Primary Technologies ：CVD, Epitaxy

- Metal Films

W, Ti, TiN, Al, Cu, Ta, TaN, Co, Ru, Mo
Primary Technologies ：CVD, PVD, ALD, ECD*

*ECD：Electrochemical Deposition

Main Products



NT333™
Atomic Layer Deposition System



Episode™
Chemical Vapor Deposition



EVAROS™
Thermal processing System

Manufacturing Base: Yamanashi / Iwate



CVD・ALD・Oxidation/Diffusion (2025)*

FY2026 Sales Mix



Expected Items

- Logic: High-k capacitor for advanced packaging (POR)
- Logic: Evaluation started for gap-filling process with single-wafer plasma CVD
- NAND: Metal for word line (POR)

Source
* Gartner®, Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2025, Bob Johnson and Menglin Cao, 2 April 2026, Revenue from Shipments basis. Chart created by TEL based on Gartner research. Gartner research. Calculations performed by TEL.
Deposition System: Tube CVD + Atomic Layer Deposition Tools + Oxidation/Diffusion Furnaces + Nontube LPCVD, ALD: Atomic Layer Deposition Tools, CVD: Tube CVD + Nontube LPCVD, Oxidation/Diffusion: Oxidation/diffusion Furnaces
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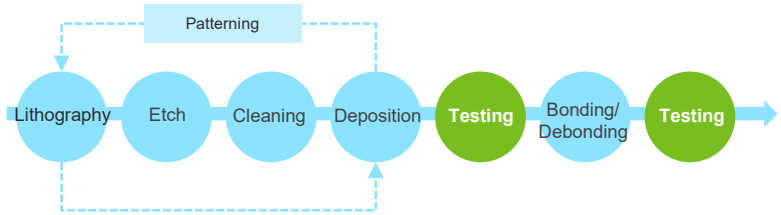
Test

As semiconductor performance advances, testing requirements are becoming increasingly sophisticated and comprehensive. In advanced packaging, securing Known Good Dies (KGDs) through highly accurate pre-assembly testing is critical to improving final yield. In addition, demand is growing for testing singulated packages before substrate assembly, creating new inspection opportunities beyond traditional wafer testing.

TEL's Process Coverage



Major Manufacturers

Prober	Tester
TEL	Advantest
ACCRETECH	Teradyne

Test Systems

- Prober
  Precisely positions wafers or device substrates and probe cards, while controlling test temperature for accurate electrical characterization
- Tester
  Inputs and outputs electrical signals through the probe card to evaluate chip performance and determine pass/fail

Main Products



Prexa™
Wafer Prober



Prexa™ SDP*
*Singulated Device Prober



CelIcia™
Multi-Cell Test System

Manufacturing Base: Yamanashi / Taiwan



Wafer Prober (2025)*

FY2026 Sales Mix



Expected Items

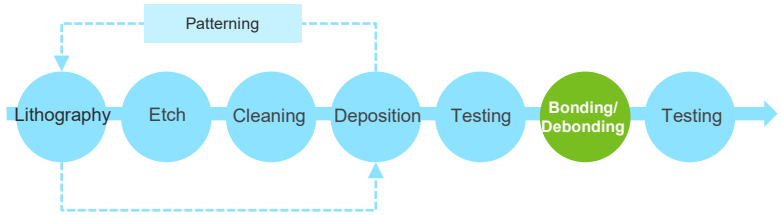
- Strong position in the AI/HPC advanced logic market; prober sales expected to exceed 100 billion JPY in 2027
- Device prober: Evaluation started with multiple customers
- Dominant position in advanced logic probers

Source
* SPE (Wafer Prober) : Auto Probers, TechInsights Inc., April 2026 Charts/graphics created by Tokyo Electron based on : TechInsights Inc.

Bonding/Debonding

In order to improve semiconductor performance, three-dimensional device stacking is becoming increasingly common. Demand for wafer bonding and debonding is growing to support these stacked structures. Interest is also increasing in alternatives to conventional laser-based processes due to their economic and environmental benefits.

TEL's Process Coverage



Major Manufacturers

Wafer Bonder	Die Bonder
TEL	Besi
EV Group	ASMPT
SUSS	

Bonding/Laser Technology

Temporary Bonding/Debonding
Permanent Bonding
- Fusion Bonding (Oxide-to-Oxide bonding)
- Hybrid Bonding
  (Simultaneous bonding of oxide layers and Cu interconnects)

Laser-related Equipment
- Laser Trimming
- Laser Lift Off

Main Products



Synapse™ V/ Synapse™ Z Plus
Temporary Bonder/ Temporary Debonder System



Synapse™ Si
Wafer Bonder



Ulucus™ LX
Laser Lift Off System

Manufacturing Base: Kumamoto



Wafer Bonder(2025)*

FY2026 Sales Mix

2%

Expected Items

- Bonder:
  Temporary bonder/debonder: HBM wafer thinning (POR)
  Permanent bonder: CMOS image sensors, NAND cell + peripheral circuit, logic backside PDN (POR)
- Laser trimming/lift off: Process evaluation progressing with multiple customers
- Bonder/laser related equipment: Expect 5-year cumulative sales of over 500 billion JPY by 2030

Source
* Gartner®, Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2025, Bob Johnson and Menglin Cao, 2 April 2026, Revenue from Shipments basis. Chart created by TEL based on Gartner research. Gartner research. Calculations performed by TEL.
Wafer Bonder: Wafer Bonder.
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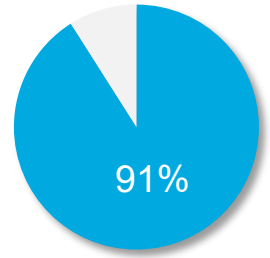
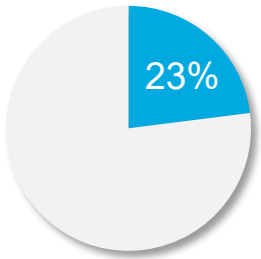
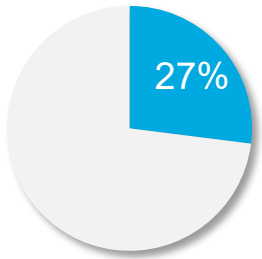
World Market Share of Major Products (CY2025)



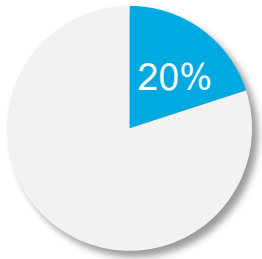
Coater/Developer



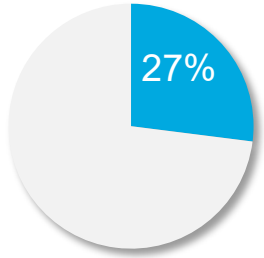
Dry Etch System



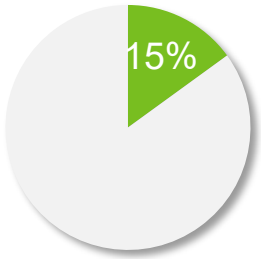
Deposition System



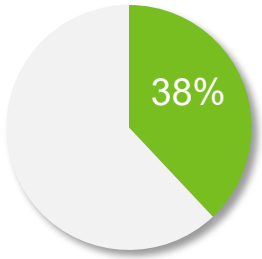
Cleaning System



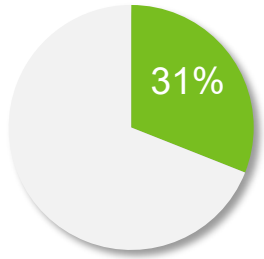
Wafer Bonder



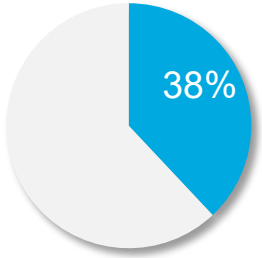
ALD



CVD



Oxidation/Diffusion



Wafer Prober

Source
Gartner®, Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2025, Bob Johnson and Menglin Cao, 2 April 2026, Revenue from Shipments basis. Chart created by TEL based on Gartner research. Gartner research. Calculations performed by TEL.
Coater/Developer: Photoresist Processing (Track), Dry Etch System: Dry Etch, Deposition System: Tube CVD + Atomic Layer Deposition Tools + Oxidation/Diffusion Furnaces + Nontube LPCVD, ALD: Atomic Layer Deposition Tools, CVD: Tube CVD + Nontube LPCVD, Oxidation/Diffusion: Oxidation/diffusion Furnaces, Cleaning System: Single Wafer Processors + Wet Stations + Batch Spray Processors + Scrubbers + Other Clean Equipment, Wafer Bonder: Wafer Bonder.
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Source
SPE (Wafer Prober) : Auto Probers, TechInsights Inc., April 2026
Charts/graphics created by Tokyo Electron based on : TechInsights Inc.

TEL's Strengths

Have advanced products for the 4 key process



Deposition | Coater/ Developer | Etch | Cleaning

Top market share

Major Products & Market Position*

#1	#3	#2	#1	#1	#1	#1	#1	#2
Coater/ Developer	Cleaning	Plasma Etch	Gas Chemical Etch	Diffusion Furnace	Batch Deposition	Metal Deposition	Prober	Bonding

*TEL estimate

100%

Market share of coater/developer for EUVL

*TEL estimate



Coater/ Developer | EUV Lithography

No.1

Worldwide installed base

Annual increase by about
4,000～6,000 units*

Industry's largest installed base
100,000～ units*



* As of March 2026

Source: Licensed Image

R&D Map

(As of Jul 1, 2026)



TEL Magnetic Solutions (Ireland)

imec (Belgium)

CEA-Leti (France)



TEL Technology Center, Taiwan (Taiwan)

Tokyo Electron India (India)

IME (Singapore)



TEL Technology Center Korea (Korea)

TEL Digital Design Square
Tokyo Electron Technology Solutions
Tokyo Electron Miyagi
Tokyo Electron Kyushu
(Japan)

National Institute of Advanced Industrial Science and Technology
(Japan)



TEL Manufacturing and Engineering of America (U.S.)

TEL Technology & AI Design (U.S.)

Tokyo Electron America (U.S.)

NY Creates Albany NanoTech Complex (U.S.)

BRIDG (U.S.)

Tokyo Electron America (U.S.)

TEL R&D base

Consortium

Source: TEL

Strengthen R&D Capabilities

Yamanashi R&D building
Deposition system, gas chemical etch system, corporate R&D
(Completed in July 2023)



Miyagi R&D building
Etch system
(Completed in April 2025)



Kumamoto R&D building
Coater/Developers, surface preparation system, Bonder
(Completed in October 2025)



Miyagi Technology Innovation Center
Etch system
(Completed in September 2021)



TEL Digital Design Square
DX, Software
(Began operation in November 2020)



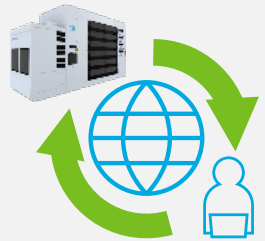
Source: TEL

Continually Pursuing the Best Products and Best Service

Front-loading



Advanced field solutions



- Share roadmap for next several generations with customers
- Promote early engagement
- Realize maximum yield of customer devices and equipment availability from early stage of customers' mass production and reduce burden on the environment
- Further increase investment in human resources/R&D by raising operational efficiency and driving higher per-employee productivity

- Business development leveraging industry's largest installed base of over 100,000 units*
- TELeMetrics™ remote maintenance
- Predictive maintenance with machine learning

* As of March 2026

Maximize Utilization of TEL's Comprehensive Strengths

Sales

Customer trust

Broad product coverage



Market-ing

Advanced data collection and analysis abilities

FS

- **Largest installed base in industry: over 100,000 units***
- **Advanced FS**

* As of March 2026

R&D

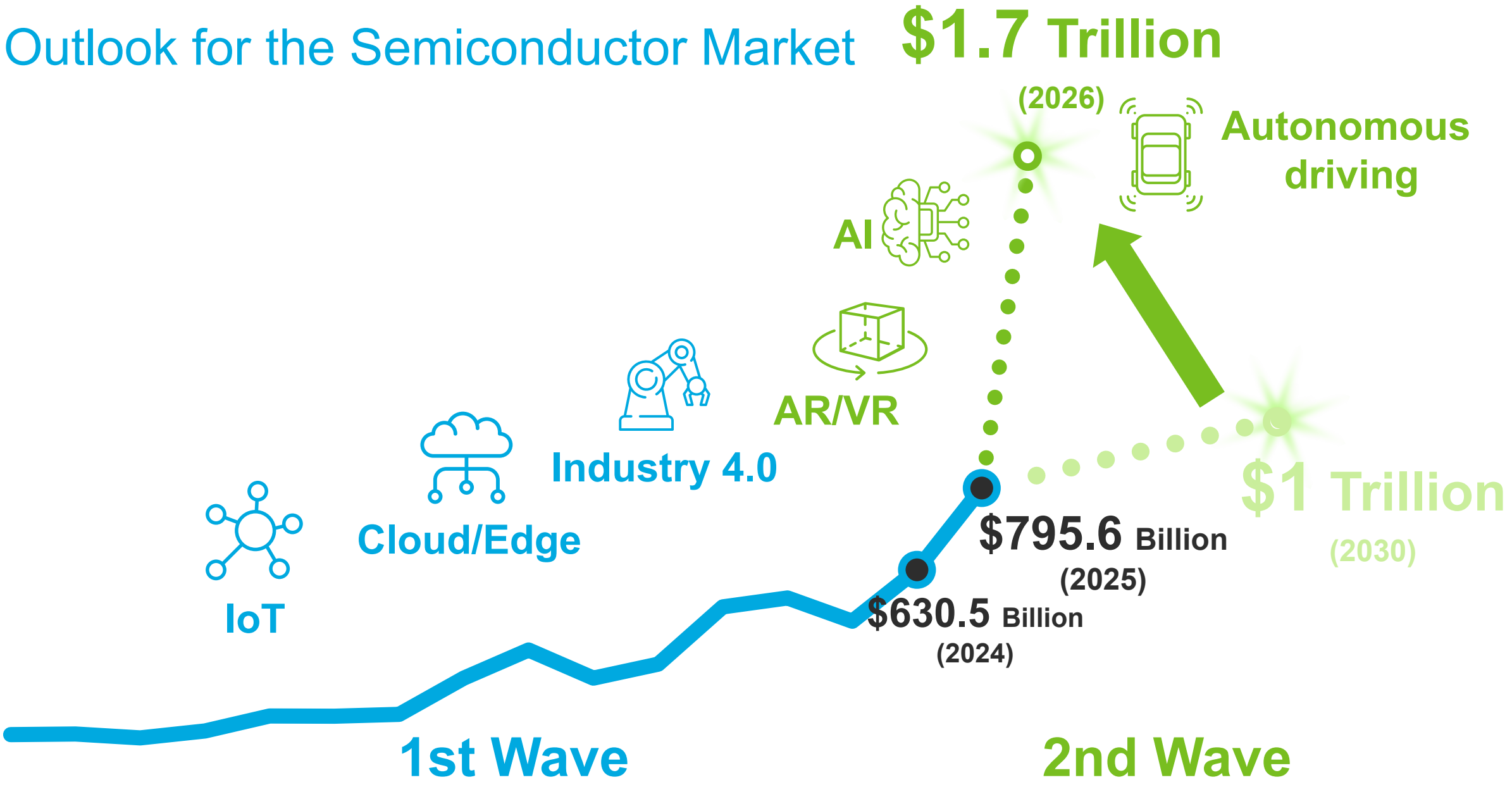
- **Strong next generation product development**
- **Process integration**

Manu-facturing

- **High quality**
- **Robust supply chain**

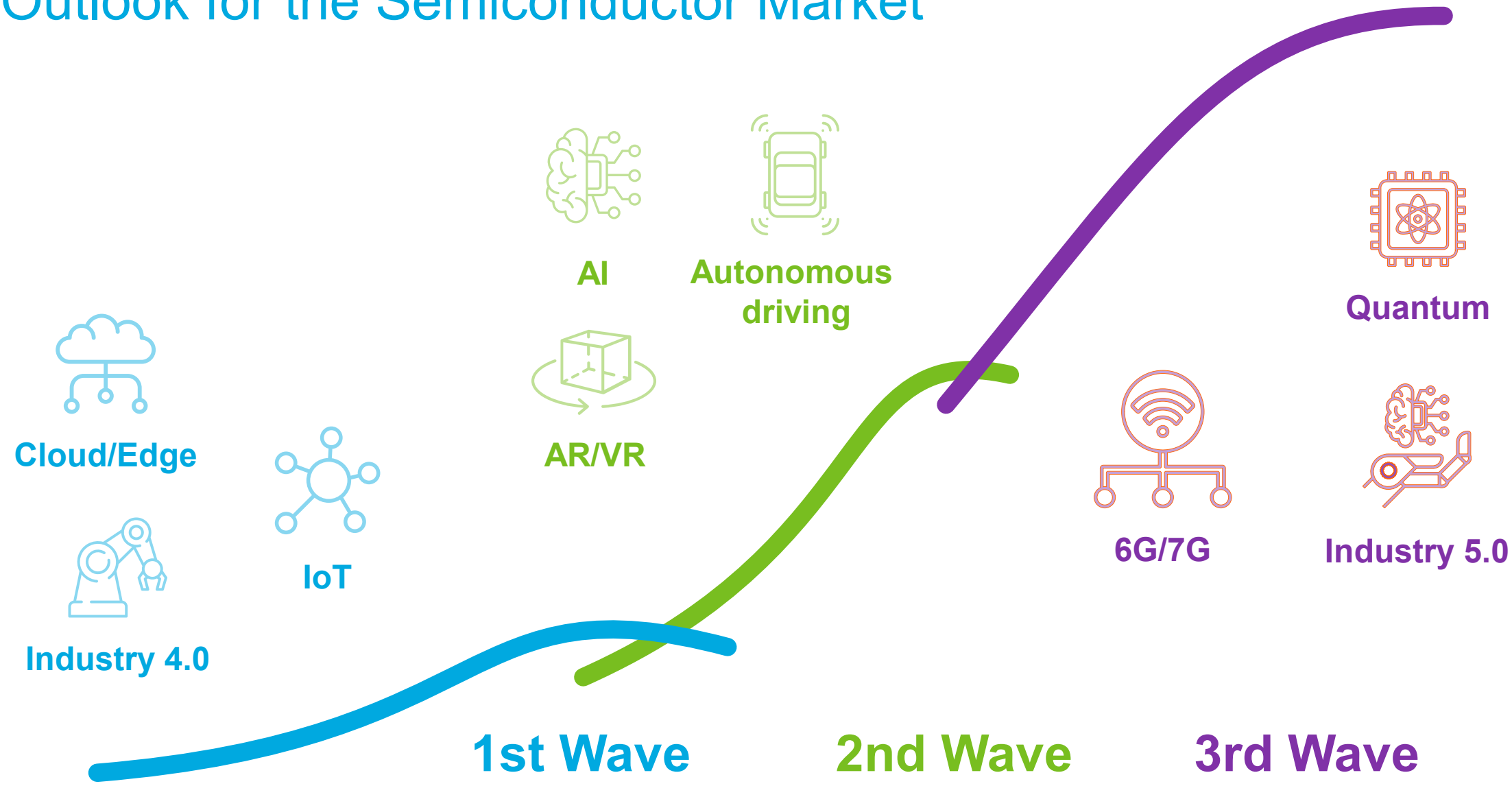
2. Semiconductor and SPE Market Outlook

Outlook for the Semiconductor Market



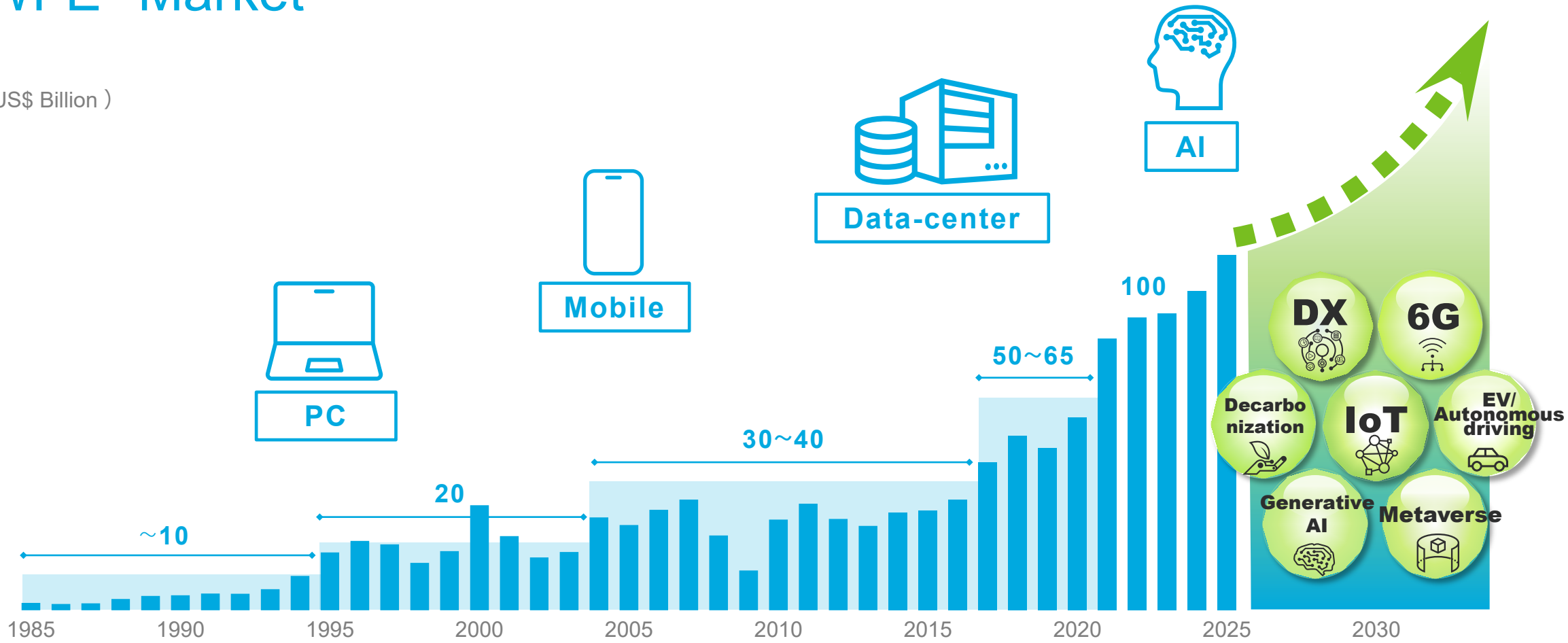
Source:2010-2026 (WSTS)

Outlook for the Semiconductor Market



WFE* Market

（US$ Billion ）



* WFE (Wafer Fab Equipment): The semiconductor production process is divided into front-end production, in which circuits are formed on wafers and inspected, and back-end production, in which wafers are cut into chips, assembled and inspected again. WFE refers to the production equipment used in front-end production and in wafer-level packaging production.

Source : TechInsights Inc. (1985~2025)

WFE Market will grow further with progress of digitalization and evolution of semiconductors

Green Future Through Semiconductor Evolution

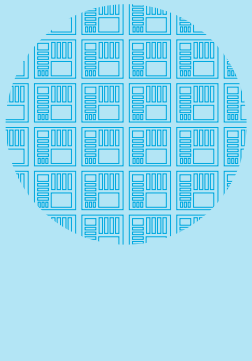
Digital & Green

Higher Speed

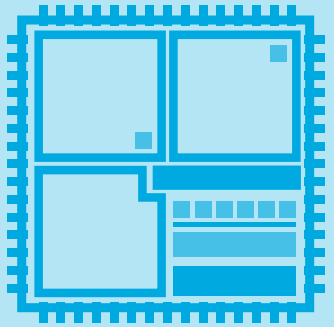
Larger Capacity

Superior Reliability

Lower Power Consumption



Physical Scaling



Heterogeneous Integration

Source: TEL

Physical Scaling x Heterogeneous Integration

Frontend

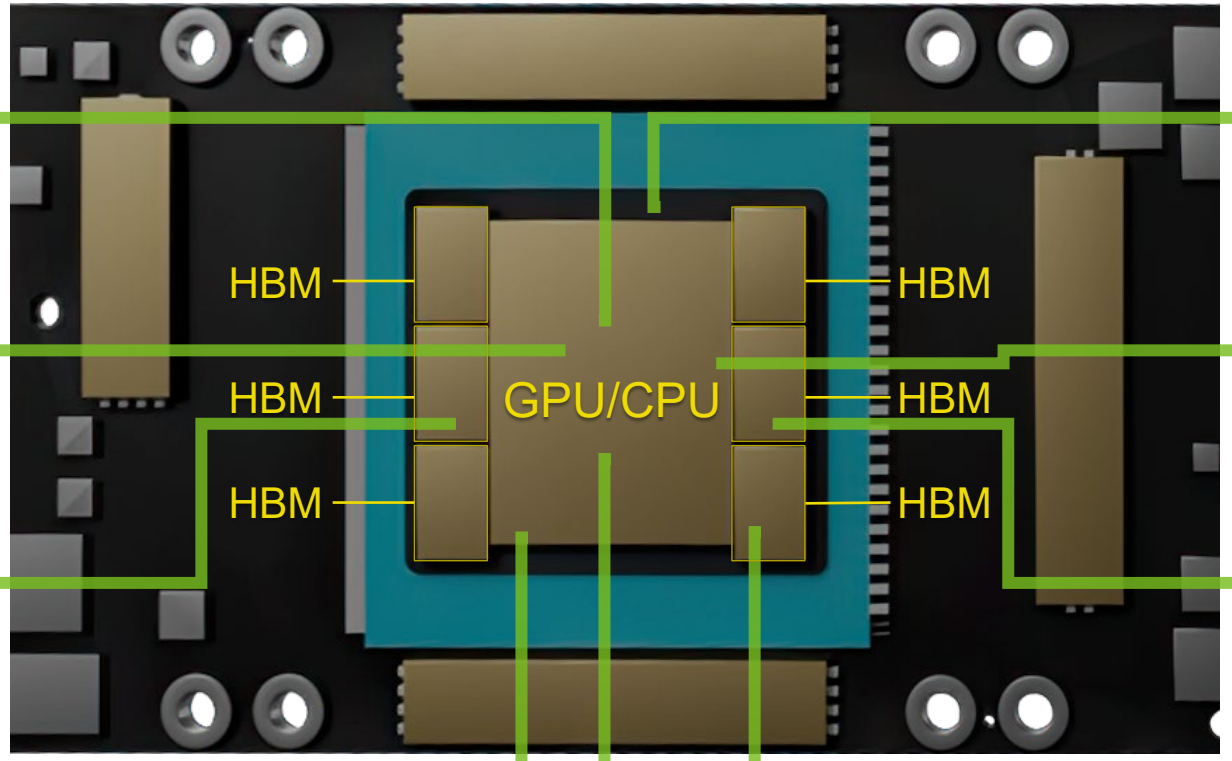
Logic
GAA * / CFET

Logic
Backside PDN *

DRAM
4F² VCT * / 3D DRAM

Super Flat Wafer

AI Semiconductor



Source: TEL

Advanced Packaging

Heat Spreader

3DIC
Chiplet Integration

Stack Memory
HBM, etc.

Known Good Die

* GAA : Gate All Around
* Backside PDN : Backside Power Delivery Network
* VCT : Vertical Channel Transistor

Expanding Opportunities: Wide Product Portfolio

Frontend | Advanced Packaging

Deposition | Lithography | Etch | Cleaning | Testing | Bonding / Debonding


Batch Deposition


Semi-batch Deposition


Single Deposition


Coater/ Developer


Plasma Etch


Gas Chemical Etch


Cleaning


Prober


Wafer Bonder/ Debonder


Wafer Edge Trimming/ XLO*

*XLO: Extreme Laser Lift Off

Strategic Technologies for Future Growth

Frontend

Logic : GAA, BSPDN

- EUV Coater/Developer
- Gas Chemical Etch
- Conductor Etch
- PVD Metal Overburden
- CFET/Inner Spacer Plasma CVD for filling film
- Double-sided scrubber
- Backside/bevel cleaning
- Pattern Shaping
- Wafer Bonder
- Laser Tool

DRAM: 2D & 3D DRAM

- EUV Coater/Developer
- Capacitor Mold Etch
- Batch High-k Capacitor deposition
- PVD Metal Hardmask
- Supercritical Cleaning
- Backside/bevel Cleaning
- Wafer Bonder
- Laser Tool

NAND: Beyond 4xx

- Slit Etch
- Channel Hole Etch (Plug)
- Batch low-resistance metallization
- Batch Cleaning WL Separation
- Wafer Bonder
- Laser Tool

Advanced Packaging

Logic Packaging

- Interposer, Polyimide & PR Coater/Developer
- TDV Etch
- Batch High-k Capacitor depo
- Wafer Bonder
- Laser Tool

HBM Packaging

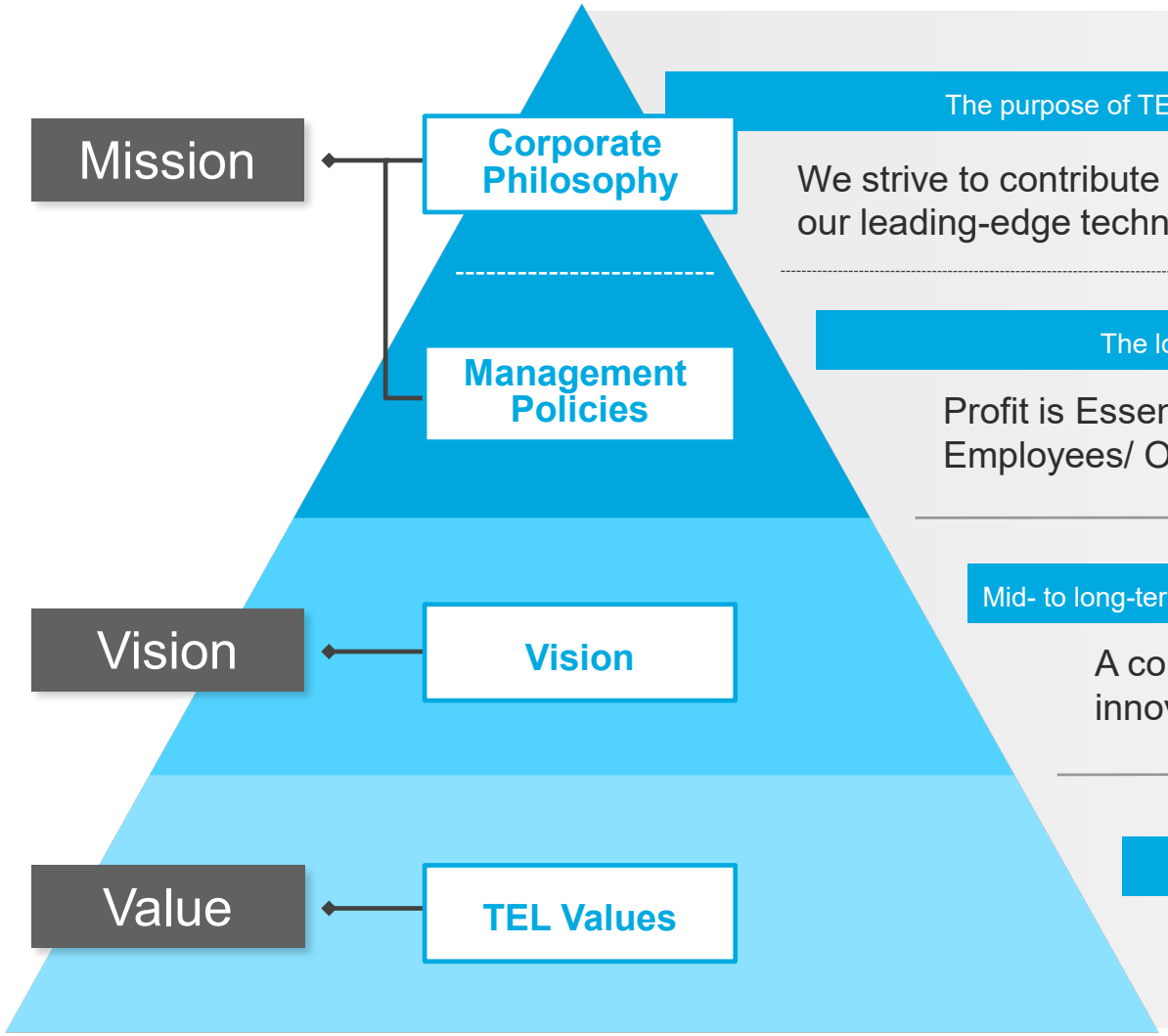
- Polyimide & PR Coater/Developer
- Metal Etch for HBM
- Aerosol Cleaning
- Temporary Bonder/Debonder

Advanced Logic / Memory Test

- Prober

3. Corporate Principles and New Medium-term Management Plan

Corporate Principles System



Corporate Philosophy

The purpose of TEL's existence and its mission in society

We strive to contribute to the development of a dream-inspiring society through our leading-edge technologies and reliable service and support

Management Policies

The logic that underscores general rules of management

Profit is Essential/Scope of Business/Growth Philosophy/Quality and Service/ Employees/ Organizations/Safety, Health, and the Environment/Social Responsibility

Vision

Mid- to long-term business aspirations based on our Corporate Philosophy and Management Policies

A company filled with dreams and vitality that contributes to technological innovation in semiconductors

TEL Values

Attitudes, codes of conduct, and values to be observed by each employee

Pride/Challenge/Ownership/Teamwork/Awareness

Vision

A company filled with dreams and vitality that contributes to technological innovation in semiconductors

Tokyo Electron pursues technological innovation in semiconductors that supports the sustainable development of the world.

We aim for medium- to long-term profit expansion and continuous corporate value enhancement by utilizing our expertise to continuously create high value-added leading-edge equipment and technical services.

Our corporate growth is enabled by people, and our employees both create and fulfill company values. We work to realize this vision through engagement with our stakeholders.

Technology Enabling Life

"Technology Enabling Life" is our corporate message that expresses the Corporate Principles which consist of our Corporate Philosophy, Management Policies, Vision and TEL Values.

CSV
(Creating Shared Value)

The concept is to create social and economic value by leveraging corporate expertise to solve social issues, hereby enhancing corporate value and achieving sustainable growth.

TSV
TEL's Shared Value

=

- Pursue technological innovation in semiconductors that supports the sustainable development of the world
- Continuously create high value-added leading-edge equipment and technical services
- Medium- to long-term profit expansion and continuous corporate value enhancement
- Engagement with our stakeholders

Realization of Vision = Creating Shared Value in TEL

Our Approaches to Social Issues

Sustainable development of the world / Diversification of values and happiness

Solutions

Online/Metaverse	AI diagnosis/Prevention/Robots	Smartification	EV/Autonomous driving/MaaS
			

Technologies

Higher speed communication (5G/6G)	Cloud/Edge Computing	AI	IoT	AR/VR/MR

Semiconductors

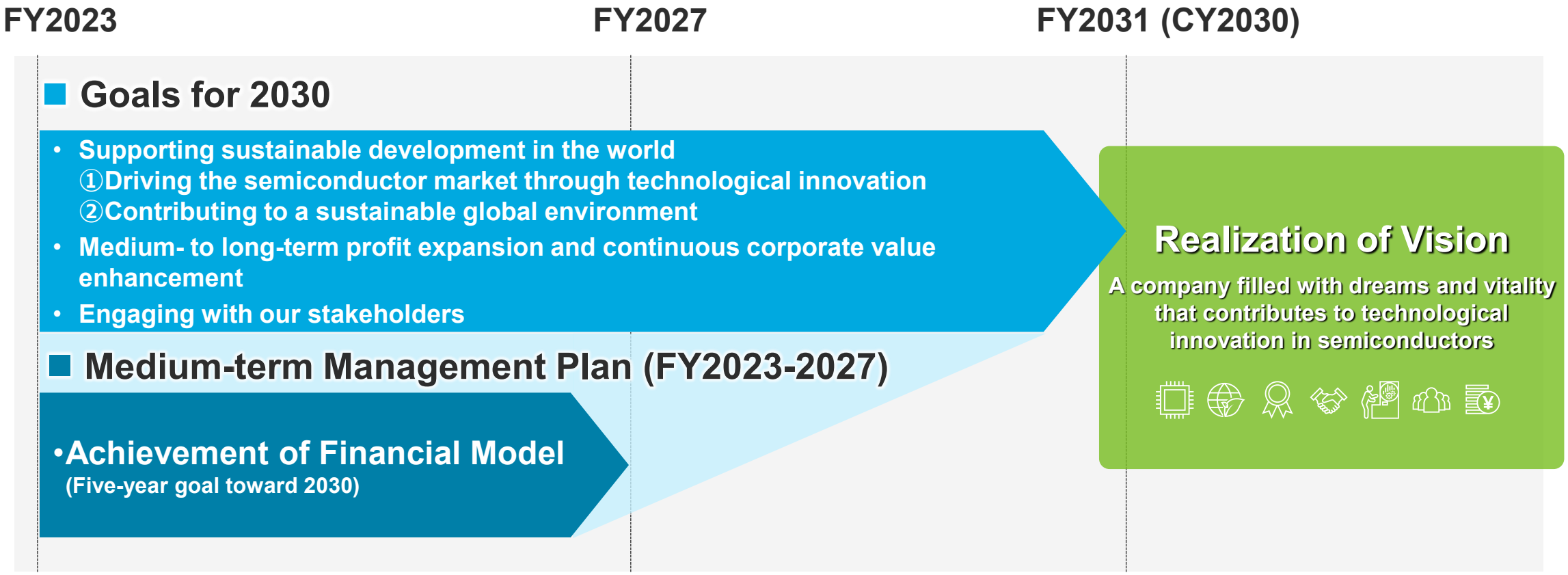
Logic	Memory	Power	Analog	Sensor	Display

Pursue technological innovation in semiconductors：
Larger capacity/Higher speed/Higher reliability/Lower power consumption

Higher definition/Flexible /Lower power consumption

Source: Licensed Image

Vision & Medium-term Management Plan

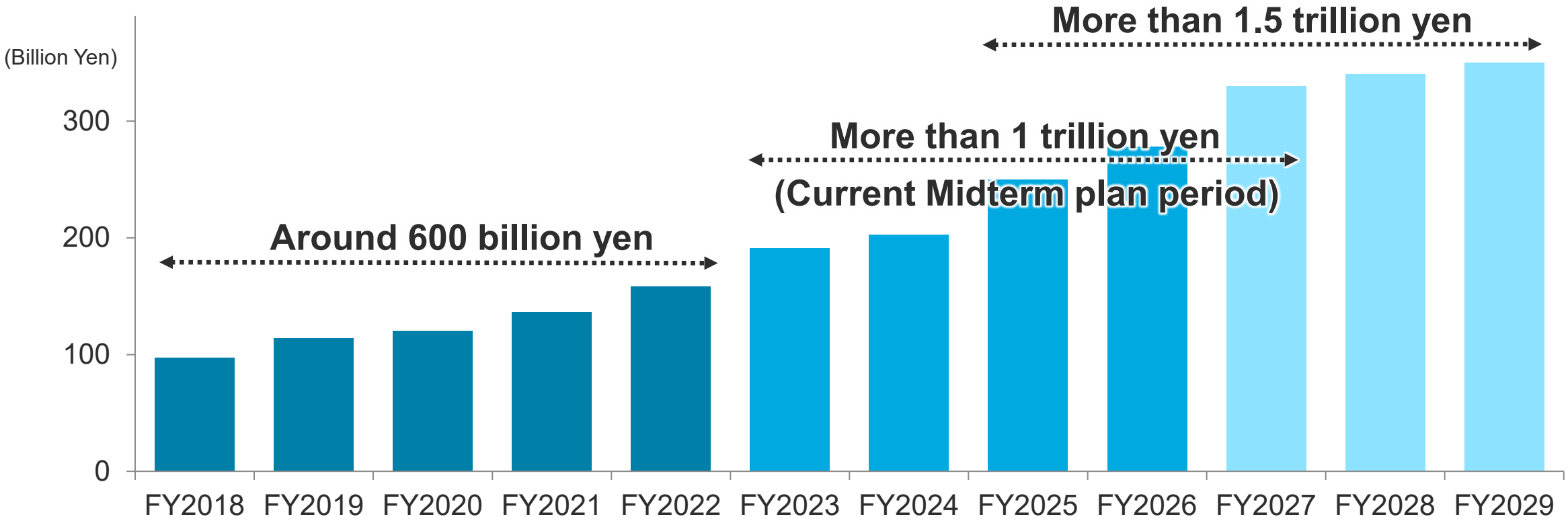


Aiming to achieve the Medium-term Management Plan
by FY2027 with a view to realizing Vision in 2030

The New Medium-term Management Plan : Financial Targets

Financial Targets (FY2023 - FY2027)	
Net sales	≧ 3 trillion yen
OP margin	≧ 35%
ROE	≧ 30%

Aggressive Investment in R&D

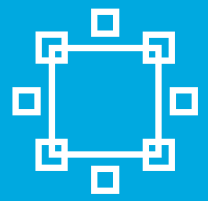


Driving the creation of high-value next-generation products through further growth investments

Investment for Future Growth (FY2025 to FY2029)

R&D Investment

1.5
trillion yen



Capex

700
billion yen



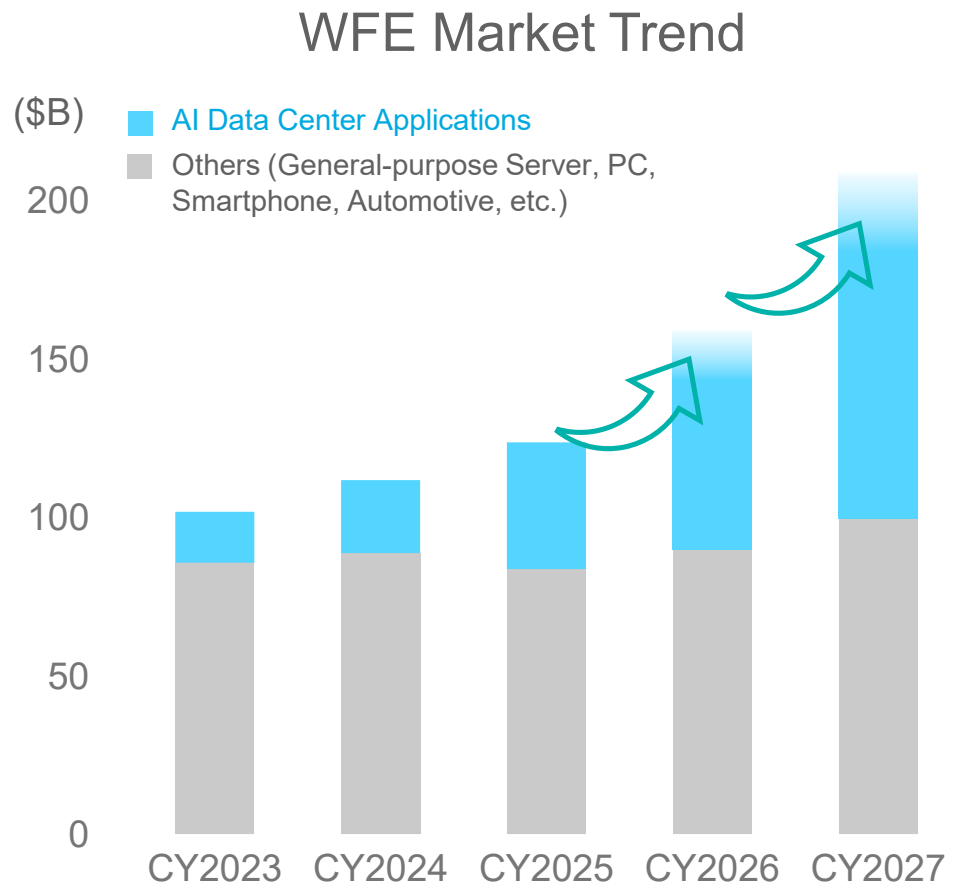
Recruitment

10,000
people
2,000 people/year



4. Business Environment and Financial Estimates

Business Environment (WFE Market Outlook as of October 2026)



WFE Market Outlook

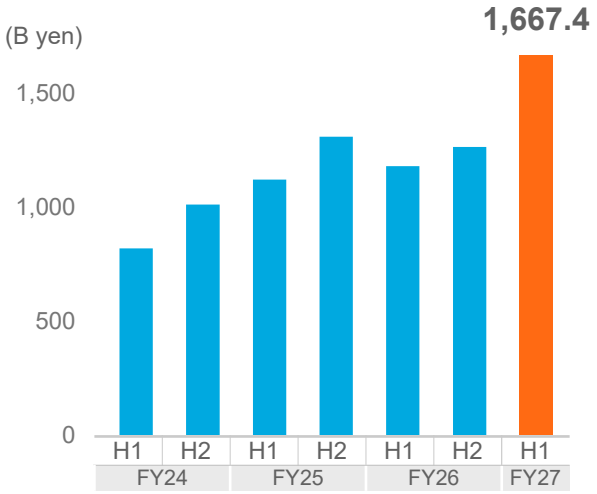
- CY2026: Approx. $160B
- CY2027: $210B+
- Adoption of generative and agentic AI **accelerating demand for leading-edge chips**
  - **GPU/HBM:** Addressing increasing compute and data volumes
  - **CPU:** Growing demand for preprocessing, data delivery to GPUs and peripheral control
  - **DRAM:** Growing capacity needs for temporary data storage around CPUs/GPUs
  - **NAND:** More storage per server for AI models and large-scale data

Rising token volumes and compute complexity driving chip demand across AI infrastructure

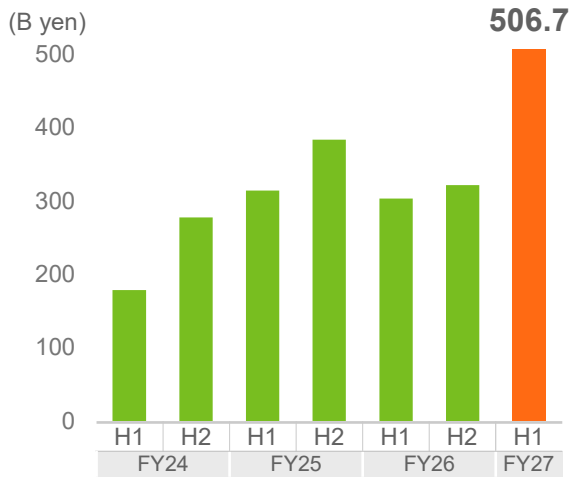
FY2027 Business Overview

- Record-high half-year performance driven by strong demand

Net Sales
1.6 trillion yen



Operating Income
506.7 billion yen



- Coater/Developer & Cleaning Systems BU:
  - Quick recovery from the Kumamoto earthquake impact; H1 sales up over +50% vs. H2 FY2026



FY2027 H1 Business & Product Progress

Etch	**DRAM capacitor mask etch (conductor etch):** 1 POR*[1] secured for the mask etch process in advanced generations, broad adoption in capacitor mold etch (dielectric etch) for current node **NAND channel hole etch (dielectric etch):** Steady progress in orders for cryogenic etch for volume production
Deposition	**Contact metal deposition (single-wafer CVD):** Development POR secured for a new process in leading-edge logic **Deep trench capacitor high-k deposition (batch ALD):** Growing demand for advanced packaging; over 200 units expected to ship in both FY2027 and FY2028
Prober	**No.1 market share in leading-edge logic:** Record-high **shipments** expected (approx. **+60% YoY**) capturing growing test demand **Volume production ramping for integrated optical/electrical testing of PICs***[2]

1 POR: Process of Record
2 PIC: Photonic Integrated Circuit



Financial Estimates for FY2027

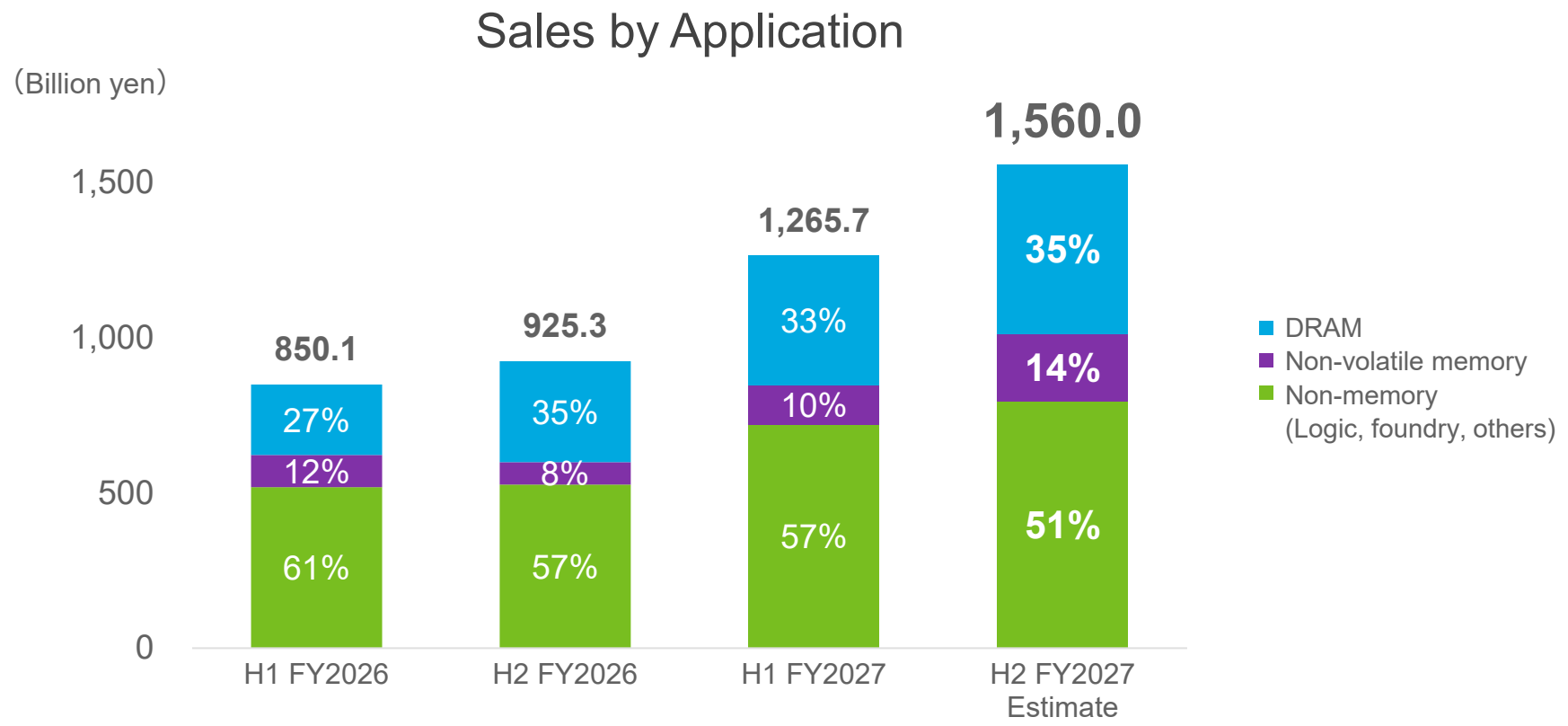
(Billion Yen)

	FY2026 (Actual)	FY2027			
		H1 (Actual)	H2 (Estimates)	Full Year (Estimates)	vs FY2026
Net sales	2,443.5	1,667.4	2,032.5	**3,700.0**	+51.4%
Gross profit	1,107.8	790.1	981.8	**1,772.0**	+59.9%
Gross profit margin	45.3%	47.4%	48.3%	**47.9%**	+2.6pts
SG&A expenses	482.9	283.3	319.6	**603.0**	+24.9%
R&D	277.8	157.3	177.6	**335.0**	+20.6%
Other than R&D	205.0	125.9	142.0	**268.0**	+30.7%
Operating income	624.9	506.7	662.2	**1,169.0**	+87.1%
Operating margin	25.6%	30.4%	32.6%	**31.6%**	+6.0pts
Income before income taxes	748.1	507.7	664.2	**1,172.0**	+56.6%
Net income attributable to owners of parent	574.4	376.9	488.0	**865.0**	+50.6%
Net income per share (Yen)	250.91	166.13		**381.69**	+130.78

- Tokyo Electron implemented a 5-for-1 common stock split on October 1, 2026.
- Net income per share is presented on the assumption that the stock split had been implemented at the beginning of FY2026.

Record-high sales, profits for full-year FY2027

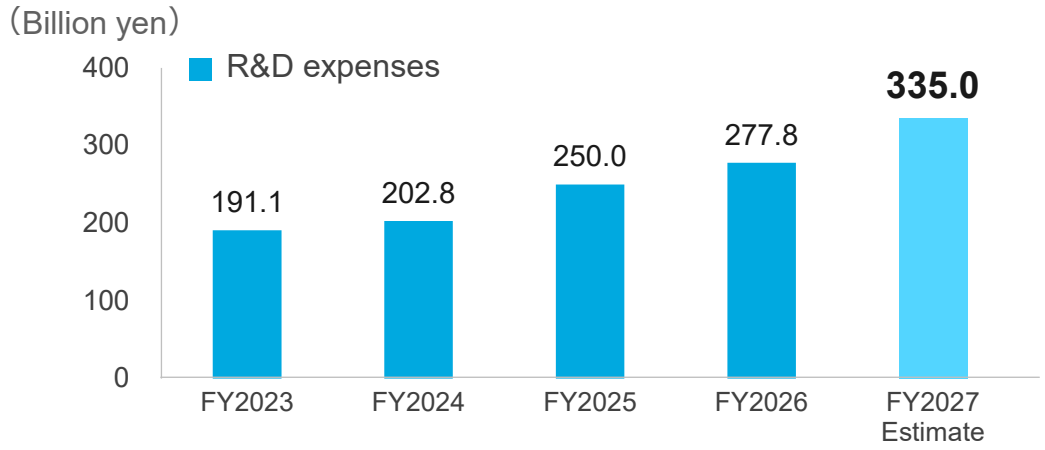
FY2027 SPE New Equipment Sales Forecast

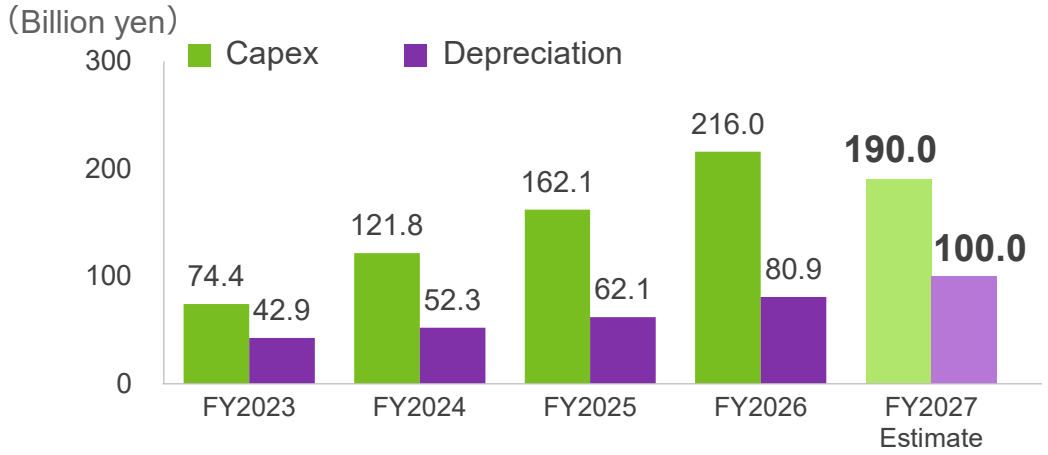


* Percentages on the graph show the composition ratio of new equipment sales. Field solutions sales are not included.

H2 SPE New Equipment sales forecast at 1 trillion 560.0 billion yen
Full-year FY2027 SPE New Equipment sales forecast to grow +59% YoY

FY2027 R&D Expenses and Capex Plan

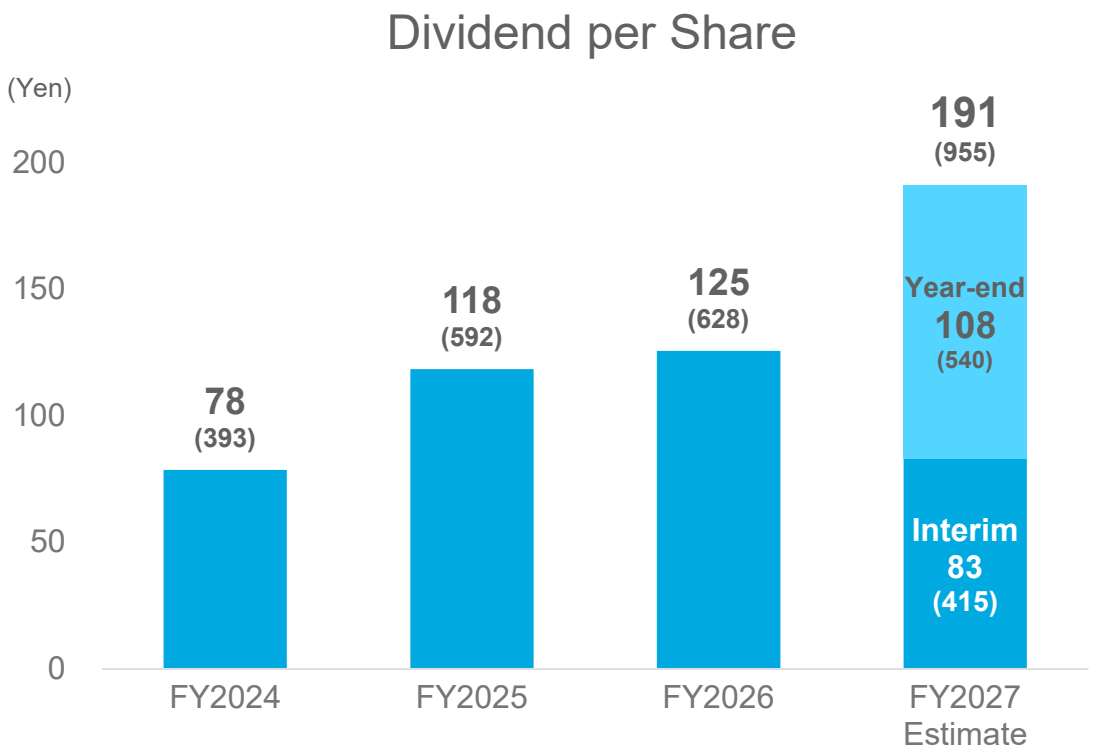






Taiwa-cho, Kurokawa-gun, Miyagi Prefecture
Completion scheduled for summer 2027

FY2027 Dividend Forecast



TEL shareholder return policy

Dividend payout ratio: 50%

Annual DPS of not less than 10 yen*

We will review our dividend policy if the company does not generate net income for two consecutive fiscal years

We will flexibly consider share buybacks

*Due to the stock split on October 1, 2026, the amount has been changed from 50 yen to 10 yen.

- Tokyo Electron implemented a 5-for-1 common stock split on October 1, 2026.
- Dividends per share from FY2024 to FY2026, and interim dividend of FY2027 are presented on the assumption that the stock split had been implemented at the beginning of FY2024.
- Amounts without taking the stock split into account are shown in parentheses.

Full-year dividend estimated at a record-high 191 yen per share

Regarding Share Repurchase

Established share repurchase facility of up to 150B yen

■ Type of shares to be repurchased	Shares of common stock
■ Total number of shares to be acquired	Up to 25 million shares (Equivalent to 1.1% of outstanding shares excluding treasury stock)
■ Total purchase amount for share repurchase	Up to 150 billion yen
■ Period of repurchase	From November 1, 2026 to March 31, 2027

TEL manages our balance sheet appropriately, considering our ability to generate cash, necessary cash on hand and growth investment capital

5. Sustainability

Sustainability Initiatives

The 14 material issues (key issues) that require prioritized attention and actions are identified to implement sustainability initiatives through our business operation and contribute to the resolution of industrial and social issues.

SUSTAINABLE DEVELOPMENT GOALS

- Respect for Human Rights
- Climate Change and Net Zero
- Product Energy Efficiency
- Best Products with Innovative Technology
- Best Technical Service with High Added Value
- Customer Satisfaction and Trust
- Supplier Relationship
- Employee Engagement
- Safety First Operation
- Quality Management
- Compliance
- Ethical Behavior
- Information Security
- Enterprise Risk Management

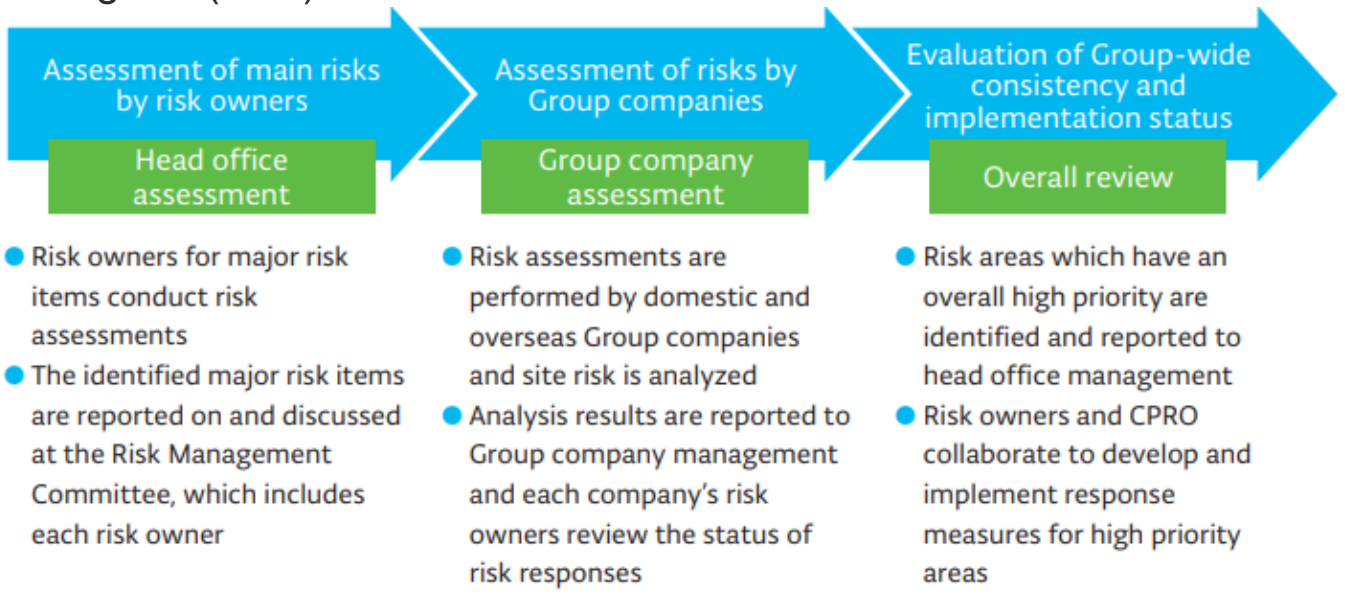


Source: TEL

Risk Management

Risk Management System and Implementation

- We established the Corporate Project & Risk Management Office (CPRO) in the Corporate Planning Division at the head office to promote more effective enterprise risk management* in the Group as a whole
- The Group's risk management activities are regularly reported to the Audit & Supervisory Board members and the Board of Directors, which oversees various initiatives implemented by each risk owner. In addition to oversight by the Board of Directors, the Group periodically undergoes audits by RBA-certified third-party organizations through the Validated Assessment Program (VAP)



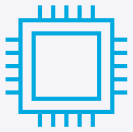
* Enterprise Risk Management (ERM): An integrated framework and continuous process for managing risks across the Group.
URL： https://www.tel.com/about/riskmanagement/index.html

Environmental Approaches in the Supply Chain

E-COMPASS

Environmental Co-Creation by Material, Process and Subcomponent Solutions

Semiconductors	Products	Business activities
Pursuing higher device performance and lower power consumption	**Achieving both high process performance and environmental performance of the equipment**	**Reduction of CO_2 emissions in all business activities**







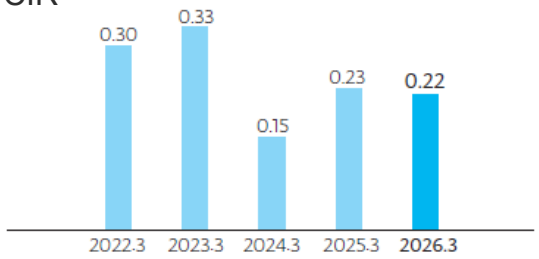
Promoting technological innovation of semiconductors
and reducing environmental impact throughout the supply chain

Safety & Quality

Safety

Under the “Safety First” slogan, everyone at Tokyo Electron, from top management to field representative, is actively and continuously improving safety and promoting health, giving safety and health the highest priority when carrying out different types of operations such as development, manufacturing, transportation, installation and maintenance.

TCIR



In fiscal 2025, through enhancement of safety training and continuous efforts toward safe design of equipment, we achieved a TCIR of 0.23, an industry-leading position in the semiconductor production equipment industry.

Safety Goals
(by FY2027)
TCIR ≤ 0.1

TCIR: Total Case Incident Rate（Number of workplace injuries per 200,000 work hours）

Incident Prevention Initiatives

- Experiential training and VR (Virtual Reality)
- Comprehensive safety inspections
- Feedback on safety specifications
- Safety activities for suppliers



Source: TEL

Quality

The Tokyo Electron Group seeks to provide the highest-quality products and services. This pursuit of quality begins at development and continues through all manufacturing, installation, maintenance, sales and support processes. Our employees must work to deliver quality products, quality services and innovative solutions that enable customer success.

Quality Policy

1 Quality Focus

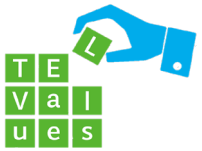
2 Quality Design and Assurance

3 Quality and Trust

4 Continual Improvement

5 Stakeholder Communication

TEL Values as codes of conduct



Engagement



Career



Corporate growth is enabled by people, and our employees both create and fulfill company values

Retention



Work-life balance



Diversity, Equity and Inclusion



3G
Global・Generation・Gender

Human Rights Initiatives

The five focus areas in human rights (Tokyo Electron Group Human Rights Policy)

- Freedom, equality & non-discrimination
- Freely chosen employment
- Product safety & workplace health and safety
- Freedom of association
- Appropriate working hours & breaks/ holidays/vacations

Human Rights Due Diligence



Commitment

Commitment to respecting human rights

- Revision of Tokyo Electron Group Human Rights Policy
- Awareness and implementation
- Education



Assessment

Assessment of human rights risks in business and supply chains

- Human rights risk assessment
- Human rights impact assessment



Remediation

Actions to reduce risks based on assessment results

- Feedback sheet publication
- Program development and review according to issues



Report

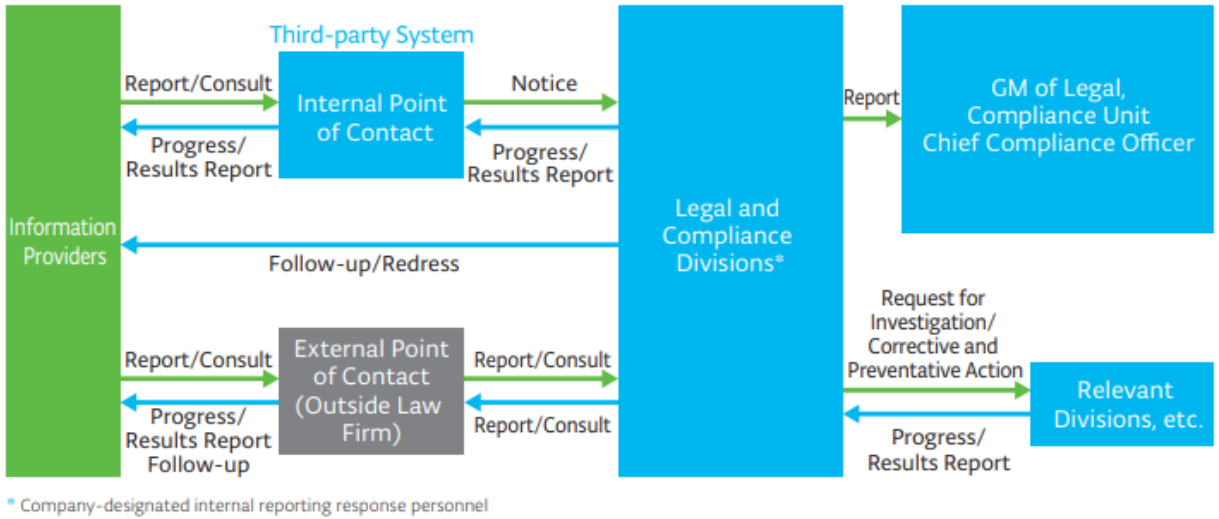
Regular disclosure of information

- Publication of the Integrated Report
- Postings on the website

Internal Reporting System

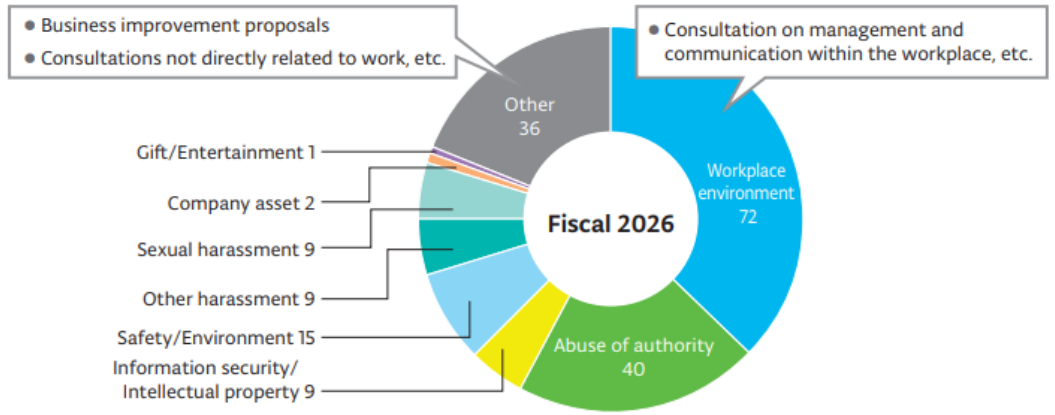
We have established an internal reporting system that allows employees to safely and securely raise concerns and seek redress outside the chain of command, and to report and consult any behavior that is, or may be, in violation of laws, regulations, or business ethics

Basic Global Response to Internal Reports



* Company-designated internal reporting response personnel

Breakdown of Report/Consultation Contents



Respect for human rights with a strong sense of integrity

Supply Chain Management

Procurement Policy

To build a sound and sustainable supply chain, we work with our suppliers to implement activities based on our procurement policy.



Supply Chain Management Initiatives

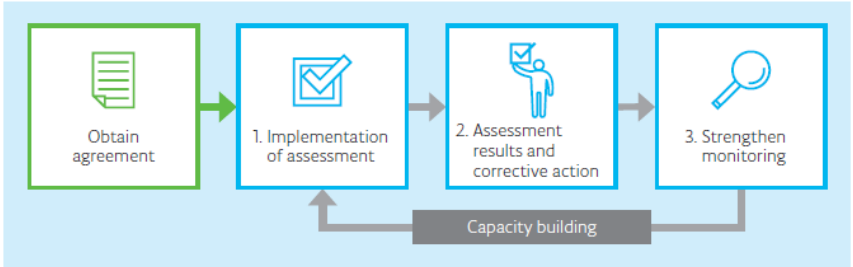
- Strengthening stable sourcing and risk management to address a wide range of risks, including geopolitical risks.
- Enhancing supply chain visibility.

Partnerships with Suppliers

- Creating communication opportunities, including “TEL Partners’ Day”.
- Publication of the “Declaration of Partnership Building”.

RBA Initiatives in the Supply Chain

- Obtaining supplier’s commitment to the RBA Code of Conduct.
- Conducting the TEL Supply Chain Sustainability Assessment (TSSA) and promoting corrective actions based on the assessment results.



Enhancing sustainable operations throughout the supply chain

RBA Initiatives

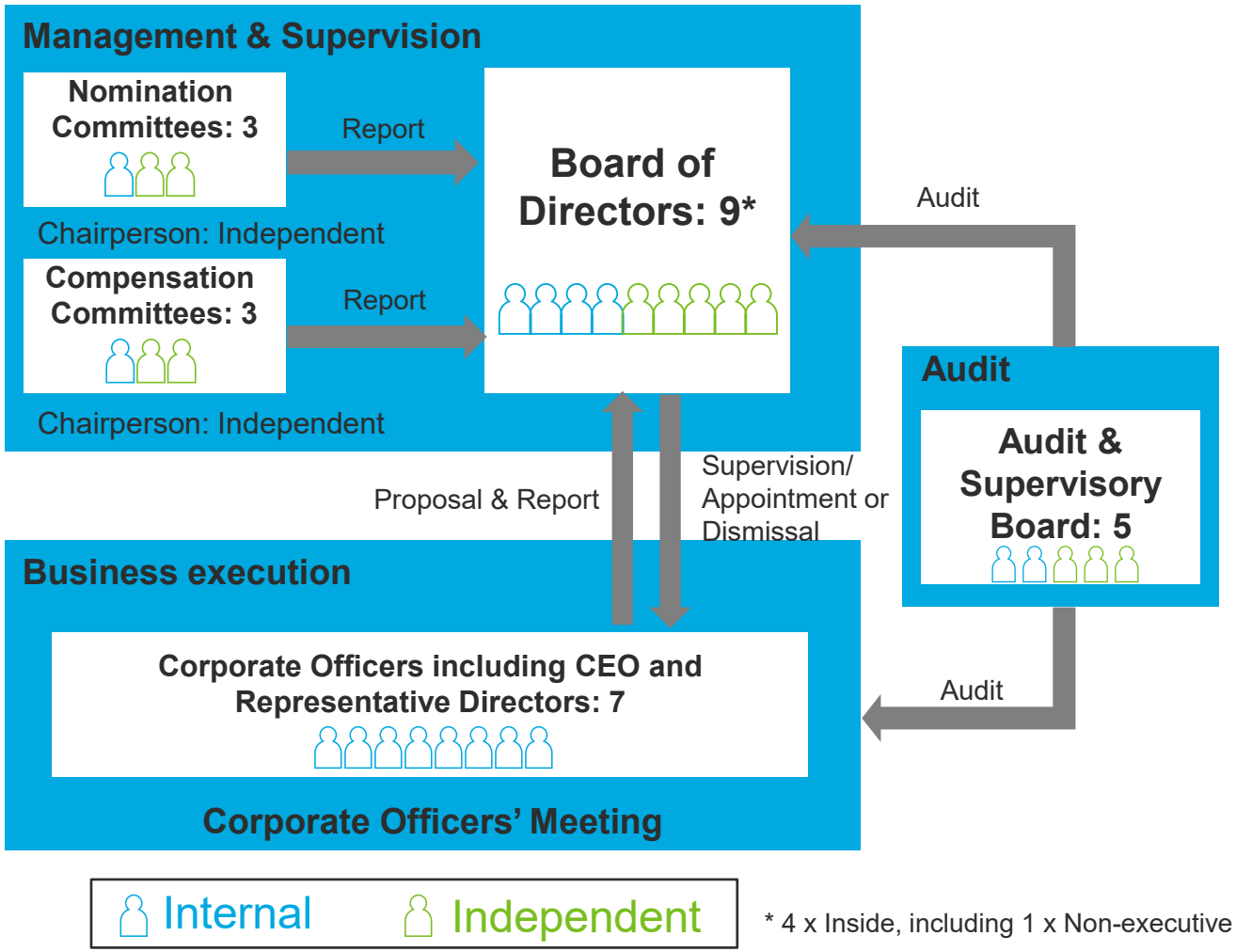
- Joined the Responsible Business Alliance (RBA) in June 2015
  - The RBA is a global initiative that promotes supply chain sustainability focused on the electronics industry.
- Implement initiatives across TEL Group and supply chain to ensure compliance with the RBA Code of Conduct
  - RBA Code of Conduct covers five areas: Labor, Health & Safety, Environment, Ethics, and Management Systems.
- Major manufacturing companies within the TEL Group continuously undergo third-party RBA audits (RBA Validated Assessment Program: VAP)

Manufacturing company	Site	Score / Status
Tokyo Electron Technology Solutions	Head Office, Hosaka	200・Platinum*
	Tohoku	200・Platinum
Tokyo Electron Kyushu	Head Office	200・Platinum
Tokyo Electron Miyagi	Head Office	200・Platinum

*Platinum: 200 points; Gold: 180-199 points; Silver: 160-179 points; Scores below 160 points are not eligible for certification.

Corporate Governance Framework (Audit & Supervisory Board System)

<Framework (Excerpt)>



* 4 x Inside, including 1 x Non-executive

The era of ultra VUCA

↓

Sharp growth of the semiconductor market

↓

Need to improve the **quality** and **speed** of decision making in both "**Management & Supervision**" and "**Business execution**"

↓

Strengthen and optimize 3 functions:
1) In-depth discussion of mid- to long-term growth strategies
2) Supervision of business execution
3) Decision-making on business execution

Accelerate "proactive management"

Growth of short-/mid-/long-term profits

Increase corporate value continually

Evaluation of the Effectiveness of the Board of Directors



Internal and external experts analyze and evaluate the effectiveness of the Board of Directors

Global Initiatives

Sustainable Development Goals (SDGs)

Clarify initiatives through business by materiality and deploy company-wide



Source: United Nations Information Centre（https://www.unic.or.jp/）

Tokyo Electron supports the SDGs

Participation in International Initiatives

Signed the UN Global Compact, joined the Responsible Business Alliance (RBA), endorsed the Task Force on Climate-related Financial Disclosures (TCFD)

WE SUPPORT UN GLOBAL COMPACT

Source: https://unglobalcompact.org/

Responsible Business Alliance
Affiliate Member

Source: https://www.responsiblebusiness.org/

SCIENCE BASED TARGETS
DRIVING AMBITIOUS CORPORATE CLIMATE ACTION

Source: https://sciencebasedtargets.org/

External Evaluation on our ESG Initiatives

Highly rated by evaluation organizations around the world

Dow Jones Best-in-Class Asia Pacific Index

FTSE4Good

Source: https://www.lseg.com/en/ftse-russell/indices/ftse4good

MSCI Selection Indexes Constituents 2025

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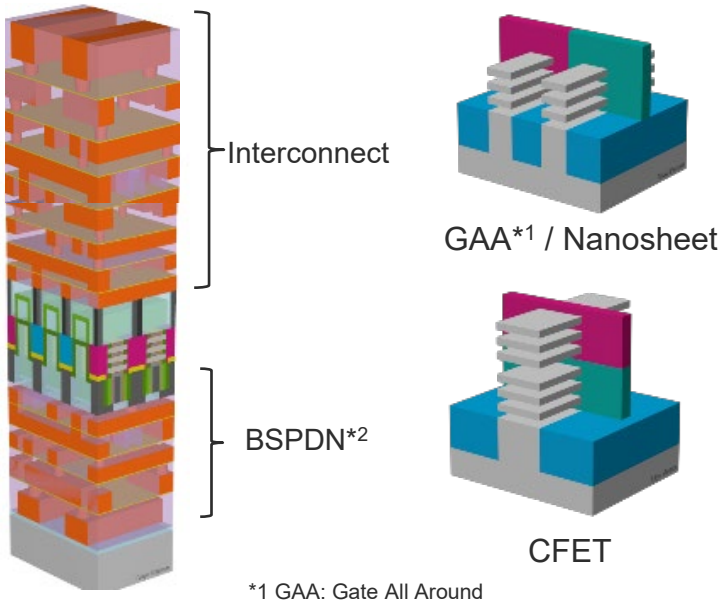
6. Diversity of Semiconductor Technology

~ Technology Roadmap~

Semiconductor Devices: Direction of Development

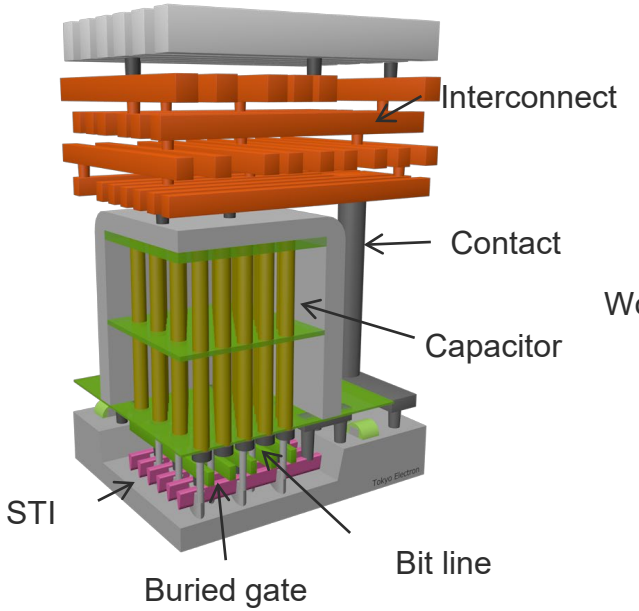
Logic



*1 GAA: Gate All Around
*2 BSPDN: Backside Power Delivery Network
*3 CD: Critical Dimension

Through miniaturization with structural changes
- Lowered cost per transistor
- Lower power consumption
- Higher speed

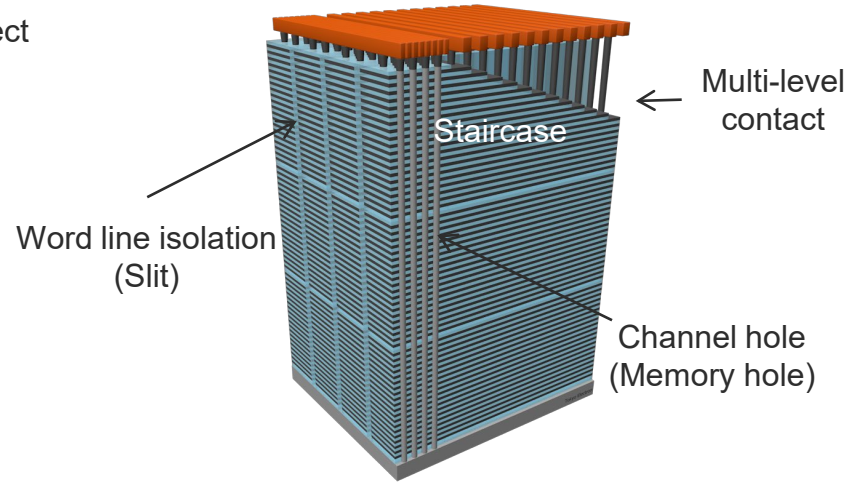
DRAM



Through miniaturization
- Lower cost per bit
- Lower power consumption
- Higher speed

Through new structures
- Lower cost per bit

NAND



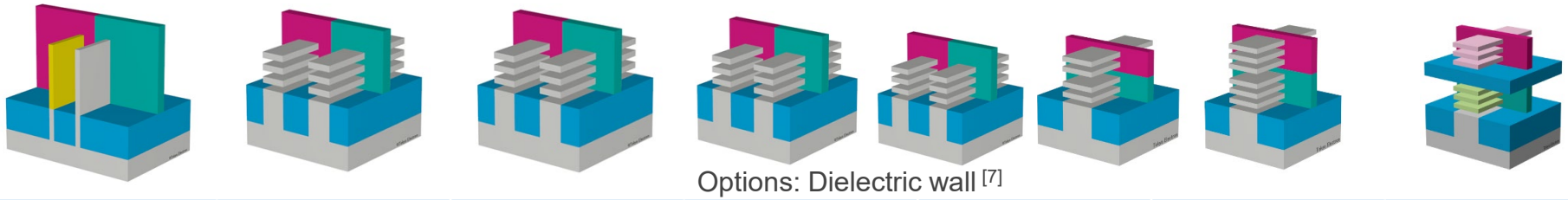
Through high stacking
- Lower cost per bit

Logic Technology Roadmap (Generic)

[1] Chih-Hao Chang (TSMC) et al., IEDM 2022
[2] Shien-Yang Wu (TSMC) et al., IEDM 2022
[3] Geoffrey Yeap (TSMC) et al., IEDM 2024
[4] Kevin Fischer (intel) et al., Symp. VLSI 2025
[5] Geoffrey Yeap (TSMC) et al., Symp. VLSI 2026
[6] Sandy Liao (TSMC) et al., IEDM 2024
[7] Mertens and Horiguchi (imec), EDTM 2024

Source: TEL estimates

Year of HVM (20k/month)	2022~24	2025~2027	2028~29	2030~31	2032~33	2034~35	2036~37	2038~39
Node	3nm	2nm/18A/16A	14A/12A	10A	7A	5A	3A	2A
Transistor	2~1 Fin	GAA NS	GAA NS scaling	GAA NS extension	NS or CFET	CFET	CFET extension	2D material stack
Poly Pitch [nm]	48~45 [1]		45~42		48 [6] ~39	45~39		36
Min. Metal Pitch [nm]	23 [2]		20	18	18~16	16	14	12
Interconnect booster	Cu Barrier/Seed CIP Backside PDN (HPC) [4,5]			Cu CIP or Ru subtractive	Ru subtractive AR>3, Airgap	New alloy AR>5, Airgap, BEOL Transistor (OS*5, 2D material)		
EUV Patterning Technology	EUV MP*1, SE*2			EUV MP, SE High-NA SE		High-NA MP, SE EUV MP, SE		
Resist	CAR*3			CAR (+MOR*4)	CAR+MOR			



*1 MP: Multi-Patterning, *2 SE: Single-Exposure, *3 CAR: Chemically Amplified Resist, *4 MOR: Metal Oxide Resist, *5 OS: Oxide Semiconductor

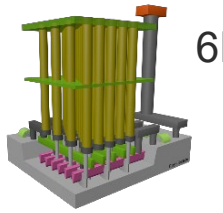
Logic scaling will continue by changing transistor structure and material evolution

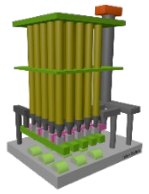
[1] S. Park (Samsung) et al., IEDM 2023
[2] D. Ha (Samsung) et al., IEDM 2023
[3] J. Park (SK hynix) et al., VLSI 2025
[4] K. Lee (Samsung) et al., VLSI 2024
[5] D. Biswas (imec) IMW26
[6] D. Ha (Samsung) et al., VLSI 2023
[7] J. Park(SK hynix) et al., VLSI 2024
[8] V. Tuong Pham et al., SPIE2026
[9] A. C. Marwitz et al., SPIE2026
[10] S. Kawakami (TEL Kyushu Ltd.) et al., SPIE 2022

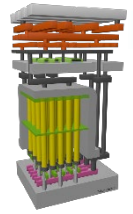
DRAM Technology Roadmap (Generic)

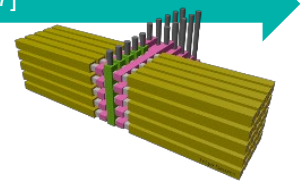
Source: TEL estimates

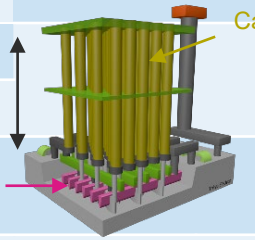
Year of HVM (20k/month)	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036
Node	1c		1d		0a	0b	0c		0d		0e	
Cell layout / Structure	$6F^2$			$4F^2$ VCT		$4F^2$ VCT[1,2,3] or $6F^2$ + Peri Bonding[4,5]			3D DRAM[6,7]			
F [nm]	12~11		10	($6F^2$)	9				(3D ~1xxL)		(3D >1yyL)	
				(VCT)	15	13.5	12					
Capacitor pitch [nm]	36~33		30	($6F^2$)	27							
				(VCT)	30	27	24					
Capacitor aspect ratio	40		>40		>40	>40	>50					
EUV Patterning	EUV MP,SE						EUV MP, SE, / hNA in R&D[8,9]			(No EUV for 3D DRAM)		
Resist	CAR + MOR[10]									CAR		
Word line	TiN			Low resistance metal								
Peri. CMOS	Gate First HKMG					w/ Bonding		Gate last Planer MOS or FinFET				
HBM		HBM4		HBM4E		HBM5	HBM5E	HBM6	HBM6E	HBM7	HBM7E	







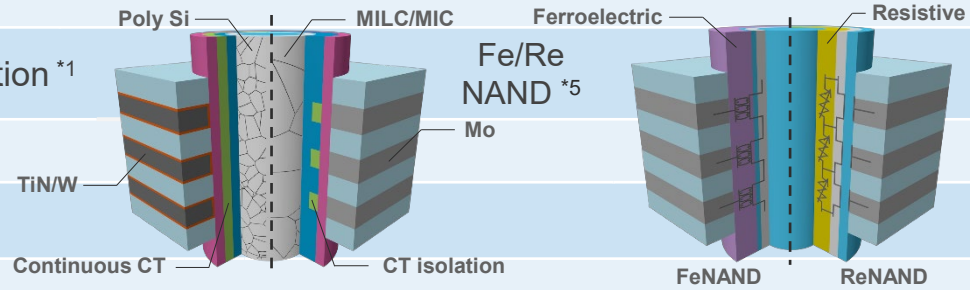


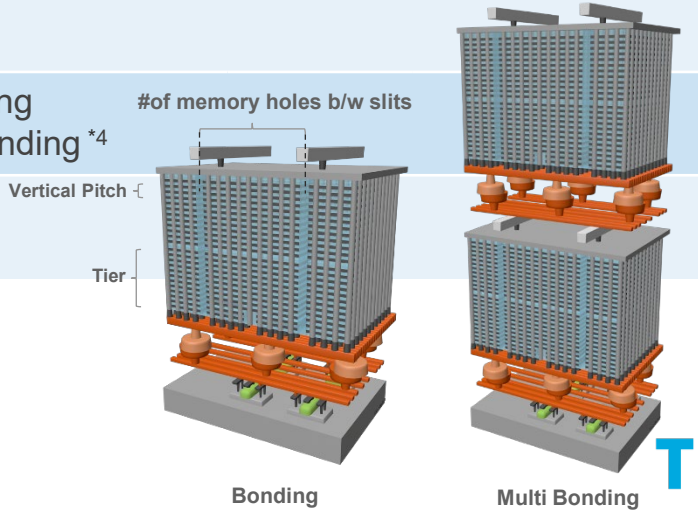


NAND Technology Roadmap (Generic)

Source: TEL estimates

Year of HVM (20k/month)	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036
Stack (~1.3x/1.5years)	3xxL	4xxL		5xxL		6xxL	8xxL	*1xxxL		*1yyyL	*1zzzL	
Tier	2 or 3	3		3 or 4		3 or 4	4 - 6					
Min vertical pitch	40 nm	39 nm		38 nm		37 nm	36 nm			~ 30 nm		
Max memory height	14 μm	19 μm		25 μm			40 μm	> 60 μm				
Charge trap (CT)	Continuous CT						CT isolation *1					
Channel	Poly Si grain CIP			MILC *2/MIC *3								
WL metal	W or Mo			Mo								
WL contact	Stair or Stairless					Stairless						
Layout/Structure	Under array or Bonding	Bonding					Bonding or Multi Bonding *4					
Peri. CMOS	Poly Si Gate			HKMG								

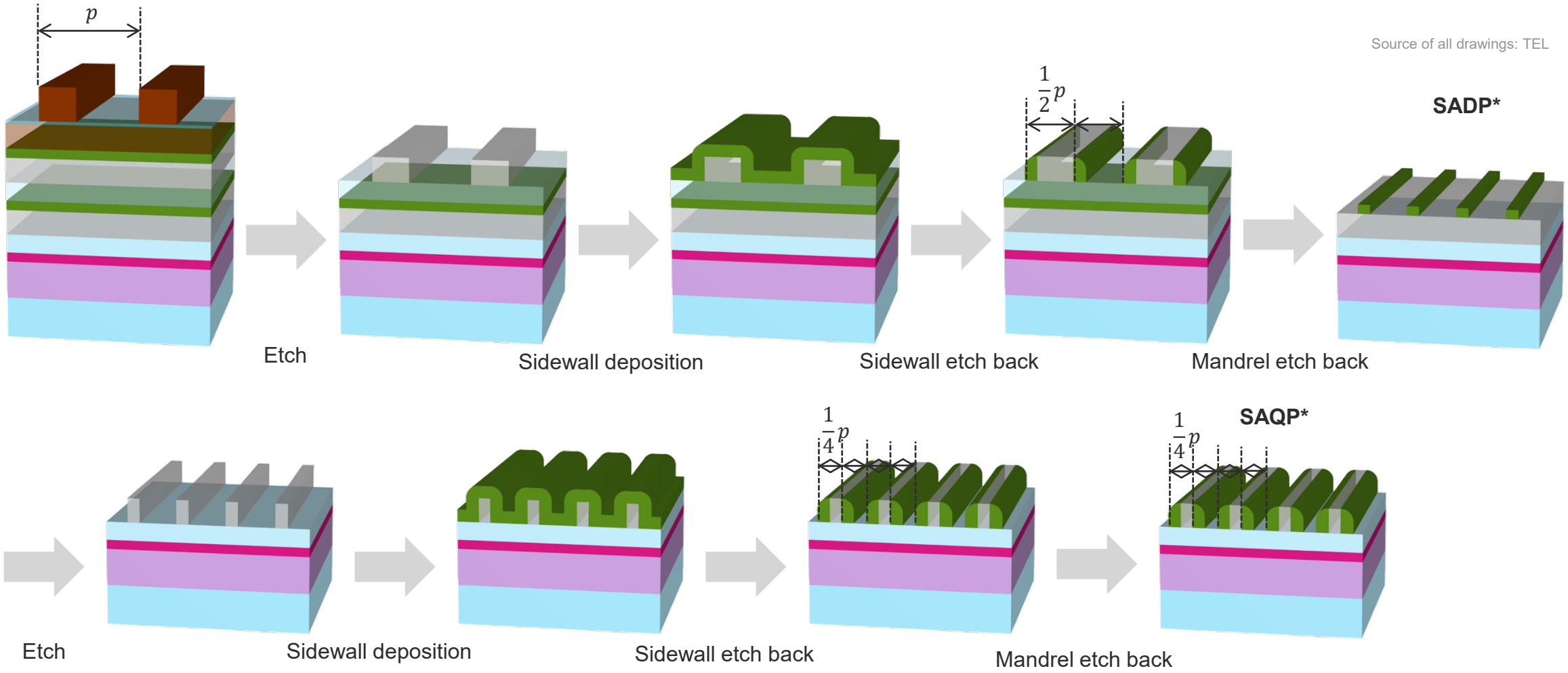




Source of all drawings: TEL

* Trend Extrapolation
[1] Sang-wan Jin (SK hynix) et al., IEDM 2025
[2] Metal Induced Lateral Crystallization
[3] Metal Induced Crystallization
[4] Mitsuhiko Noda (KIOXIA) et al., VLSI 2026
[5] Jeehoon Han (Samsung) et al., IEDM 2023

Self-aligned Multiple Patterning to Supplement Lithography

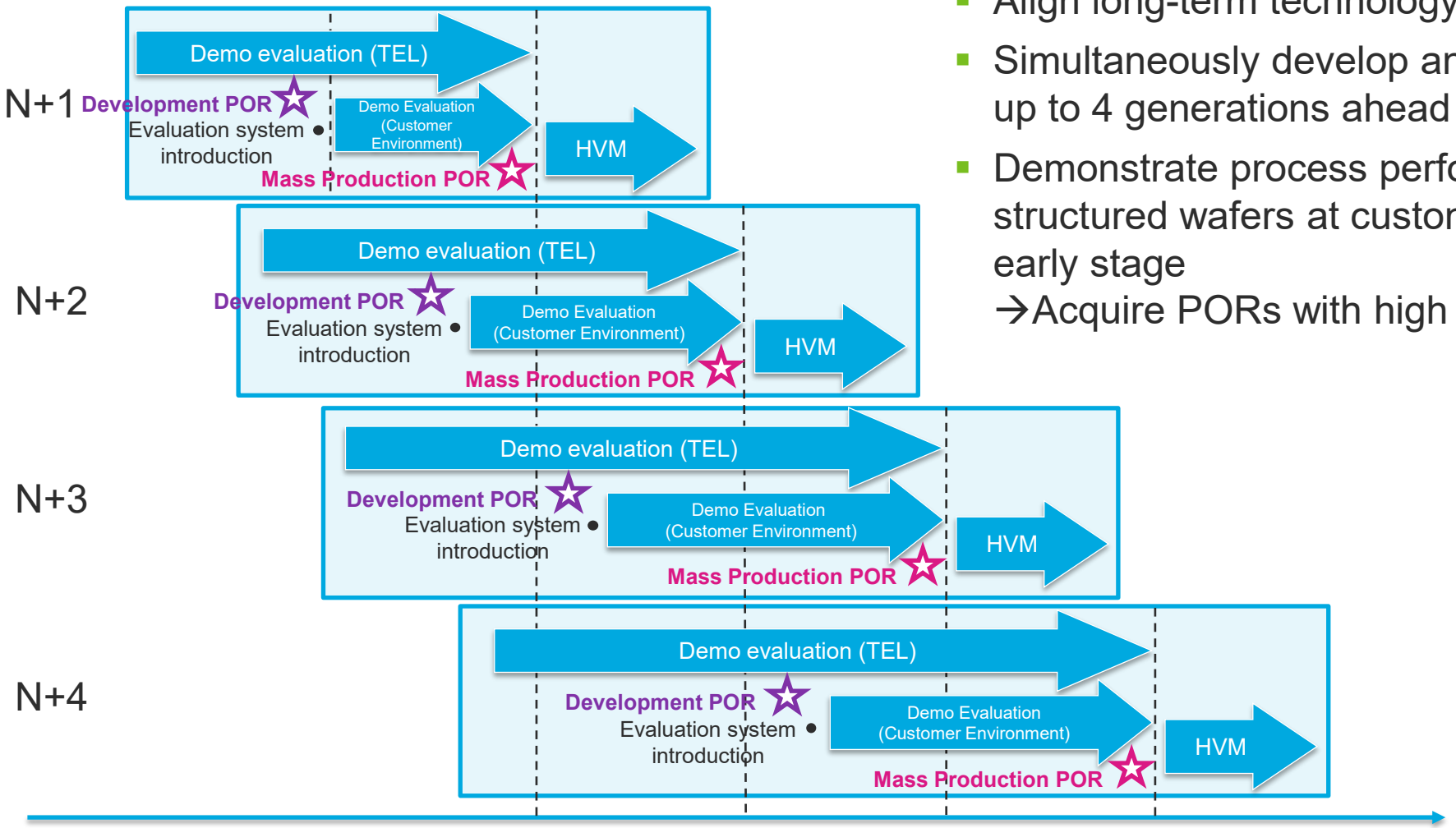


SADP: Self-aligned double patterning
SAQP: Self-aligned quadruple patterning

7. SPE New Equipment Initiatives

Development Efforts

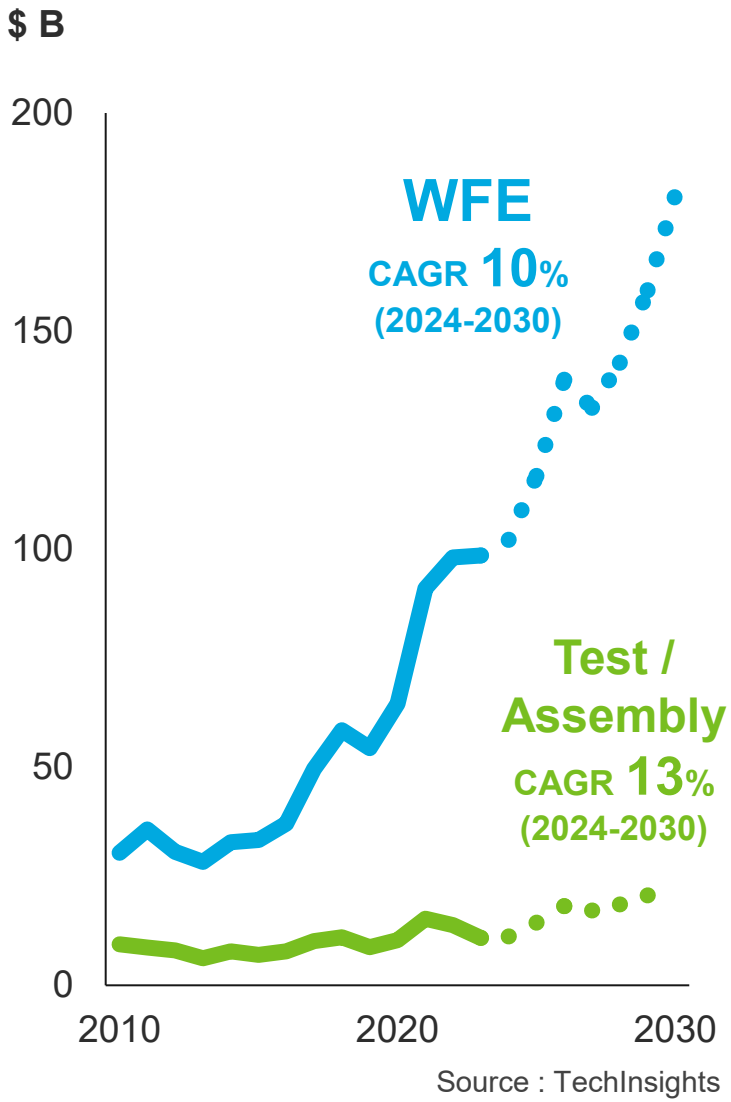
Simultaneous 4-Generation Developments



- Align long-term technology roadmap with customers
- Simultaneously develop and evaluate technologies up to 4 generations ahead
- Demonstrate process performance on customer structured wafers at customer's environments at early stage
  →Acquire PORs with high value-added products

Our Growth Opportunities in the Frontend Market

Presented at IR Day in February 2025



Source : TechInsights

- CAGR driven by AI-related devices to continue to drive high growth of WFE's CAGR
- Leveraging TEL's strengths to address high-growth market areas:
  - Leading-edge logic: The etch market is expected to grow by 2.7 times, the deposition market by 2.5 times*
  - DRAM: The etch market is expected to grow by 2.3 times, exceeding the CAGR of WFE*
- By introducing new products focused on the key technological inflection points, we aim to further expand our areas of entry

* TEL Estimates

Growth opportunities at Technological Inflection Points in Frontend Process

- Logic: GAA*1, BSPDN*2, CFET
  - Adaption of High-NA lithography, combined with multi-patterning and MOR technologies, presents opportunities for new technology Acrevia™
  - Adoption of multi-patterning to increase demand for deposition, etch, and cleaning processes.
  - GAA and CFET transistors to drive an increase in gas chemical etch processes
  - New materials like ruthenium and structural innovations such as air gaps to generate fresh opportunities
- DRAM: HBM, VCT*3, 3D DRAM
  - Adoption of multi-patterning driving increased demands in deposition and etch
  - Capacitor formation remains essential, driving ongoing demand for advanced etch and deposition
  - 3D DRAM leading to increased processes in deposition, etch and gas chemical etch
- NAND: Beyond 4xx
  - Increased layer counts leading to higher investments in deposition and etching processes
  - High aspect ratio etch to become increasingly important
  - New materials and low-resistance channel silicon to be utilized

*1 GAA: Gate All Around
*2 Backside PDN: Backside Power Delivery Network
*3 VCT: Vertical Channel Transistor

7-1. Frontend, Unit Process

7-1-1. Coater/Developer

Coater/Developer: CLEAN TRACK™ LITHIUS Pro™ Z for EUV

LITHIUS Pro™ Z released in 2012
(＞3000 systems shipped)

New features to support EUV CAR*1/MOR*2
to be released as on an ongoing basis

High Reliability
High share in EUV market

High Productivity
Maximizes output of EUV lithography tools, and reduces chemical consumption

High Versatility
Supports CAR, MOR and underlayers



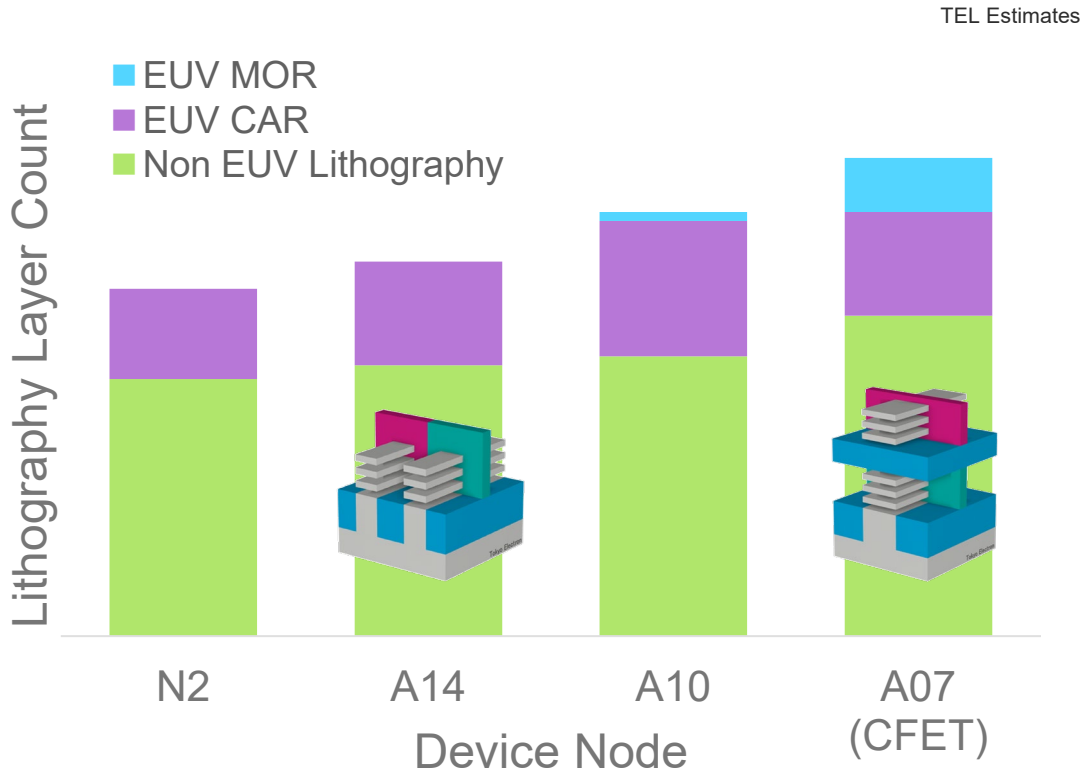
*1 CAR: Chemically Amplified Resist
*2 MOR: Metal Oxide Resist

LITHIUS Pro™ Z platform with its proven mass production for various litho tools, ensures high reliability and productivity for EUV litho, along with high versatility for next-generation EUV

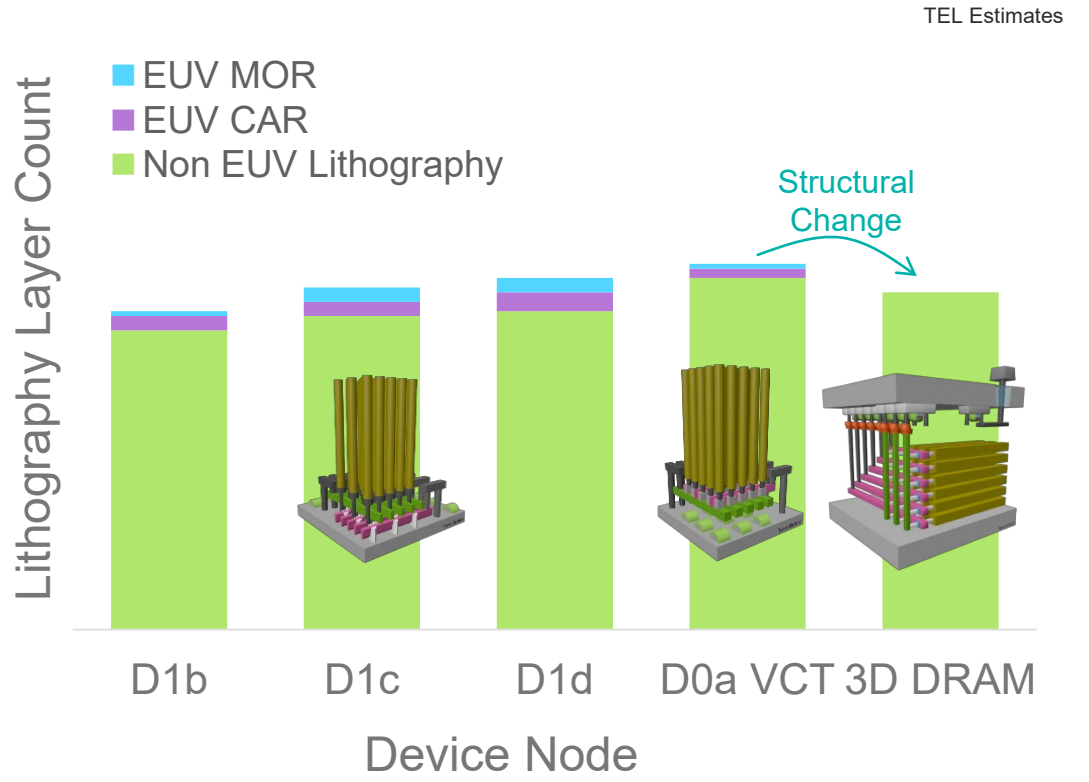
Outlook on Lithography Layer Count

Source of all drawings: TEL

Logic

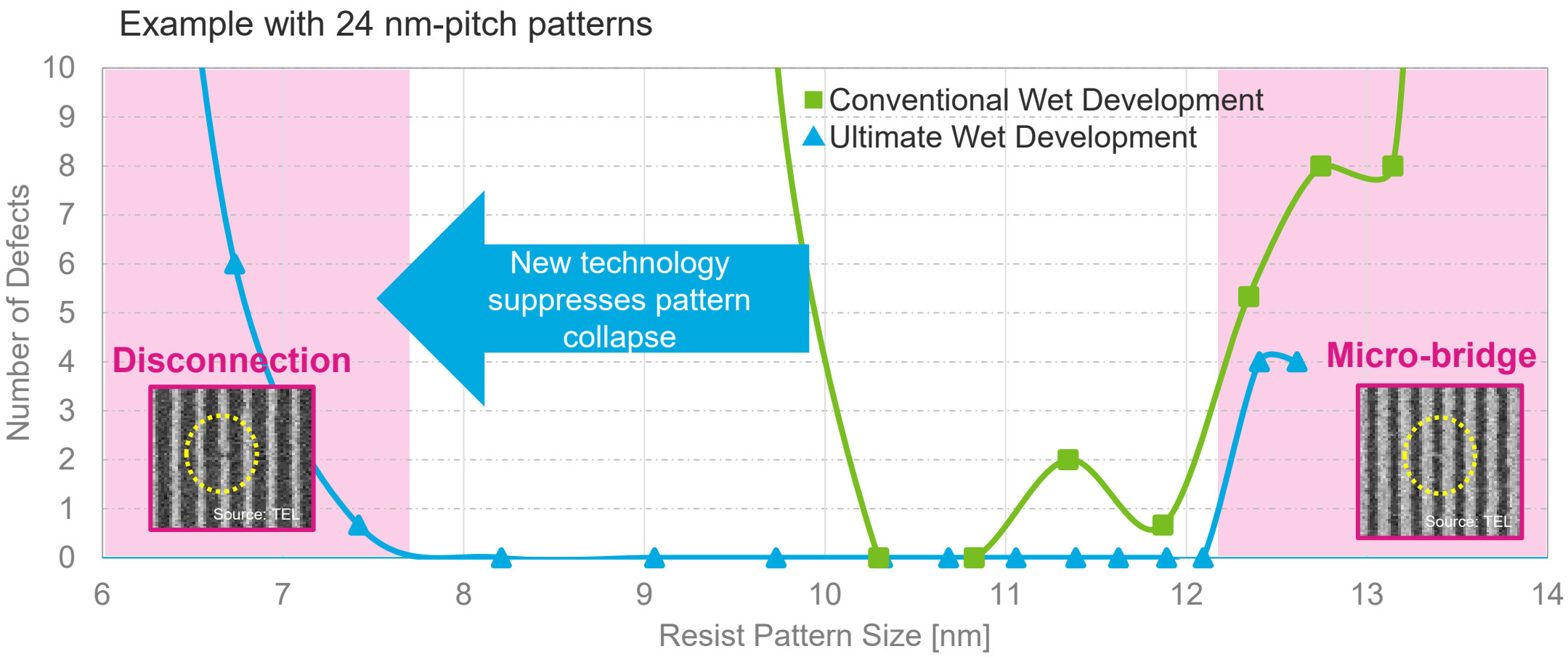


DRAM



MOR expected for Logic 10A/ DRAM D1b, development ongoing for MOR

Example of MOR Process: The Ultimate Wet Development



The Ultimate Development technology enables the suppression of pattern collapse

Example of MOR Solution: The Ultimate Wet Development

*1 Based on internal information and development targets
*2 Based on results of developing 24 nm-pitch lines

	Ultimate Wet Development Technology	Conventional Wet Technology	Alternative Technology
Base Technology	Coater/Developer	Coater/Developer	Etch
Process Ambient	Atmospheric	Atmospheric	Vacuum
Reaction	Chemicals	Chemicals	Corrosive Gas
Throughput*1	4x	4x	1x
Chemical Consumption*1	50% (vs. conventional)	100 %	N/A (uses gas) exhaust processed in combustion abatement post process
Anti-Pattern Collapse*1 Performance	< 8 nm*2	> 10 nm*2	< 8 nm*1
Footprint*1	In-Line	In-line	Additional Footprint

Evaluation of Ultimate Wet Development ongoing with key customers, with emphasis on productivity (throughput, footprint, maintainability, utilize existing facilities)

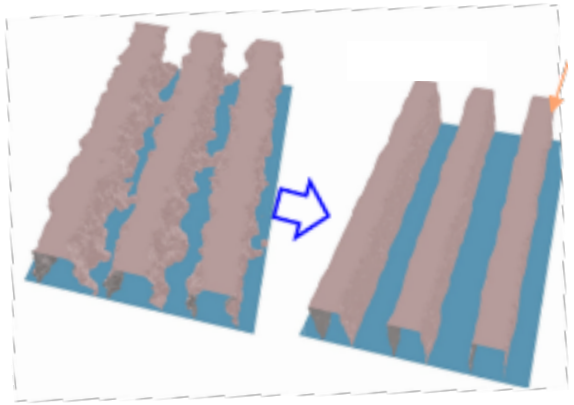
Acrevia™

TEL's Original Gas Cluster Beam (GCB) System

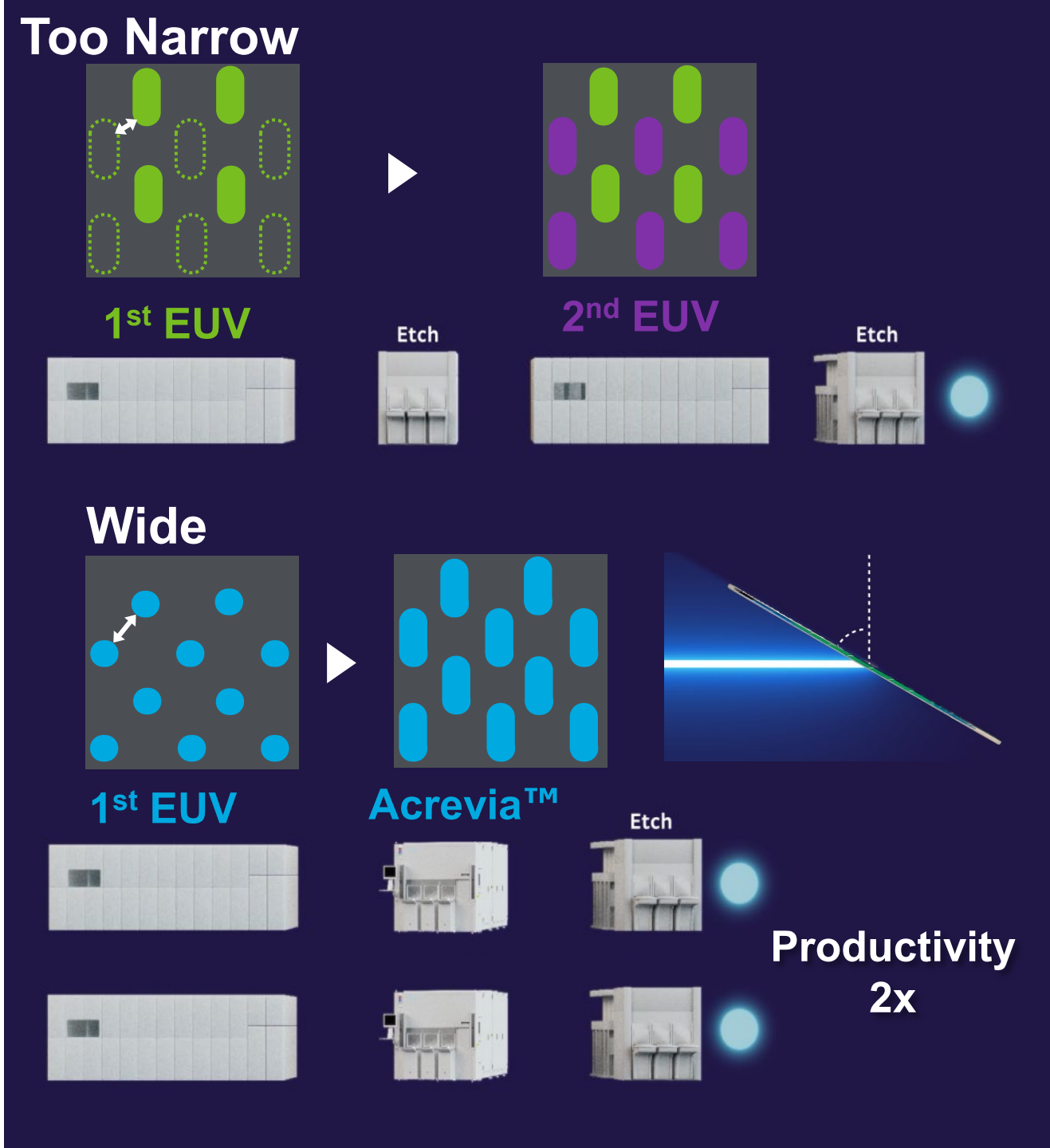
- Beam Angle is freely Adjustable
- LSP (Location Specific Processing) Wafer Scan
  → Enable 3 Dimetional Etching

✓ Drastically Improve EUV productivity by EUV step reduction with fine patterning

✓ Realize yield by removing defect between pattern and improving LER/LWR*



* LER/LWR: Line Edge Roughness / Line Width Roughness

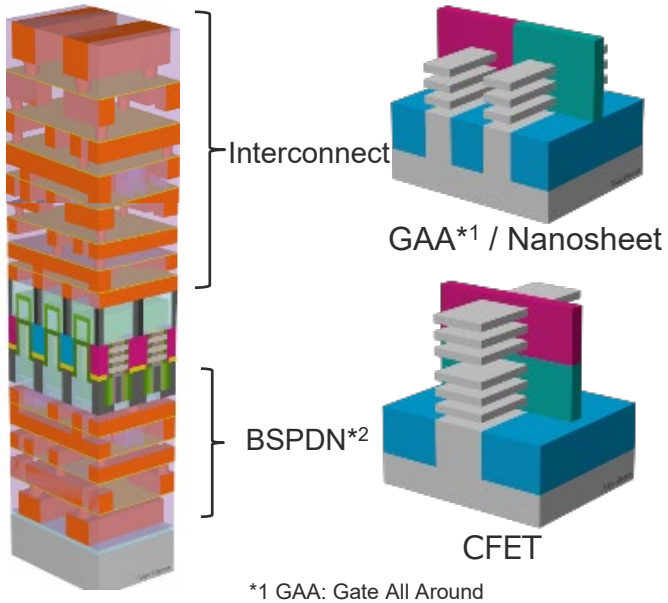


Source of all drawings: TEL

7-1-2. Etch System

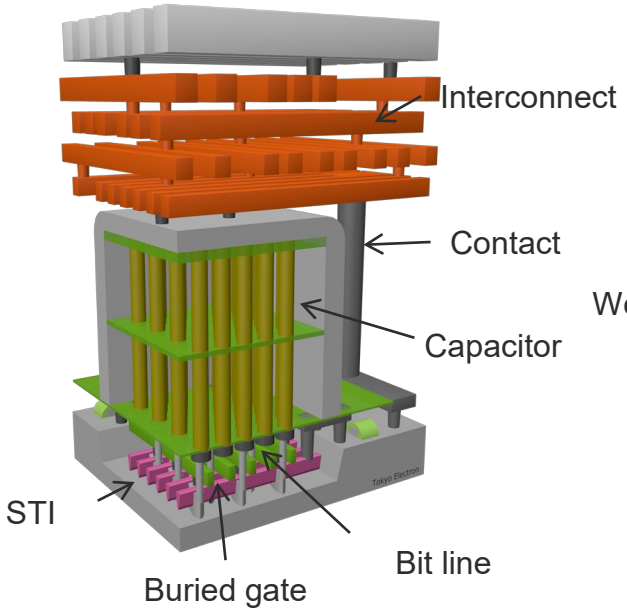
Requirements and Various Etch Technologies

Logic

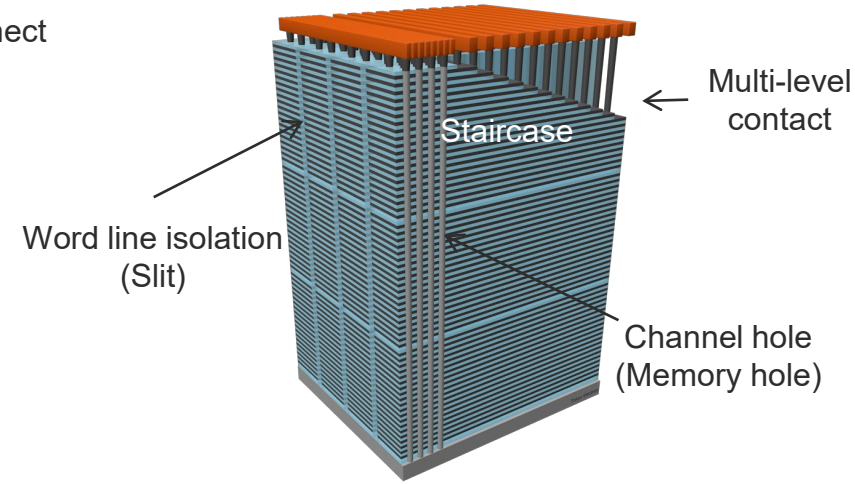


*1 GAA: Gate All Around
*2 BSPDN: Backside Power Delivery Network
*3 CD: Critical Dimension

DRAM



3D NAND

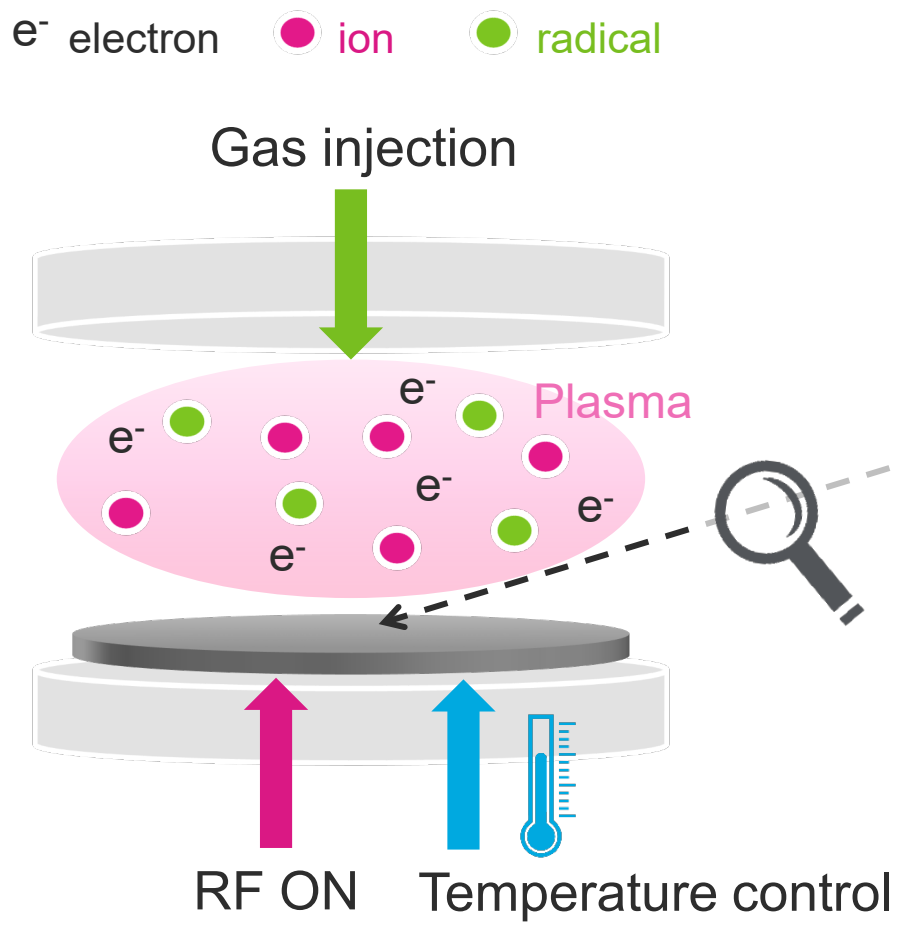


Device trend	Scaling/new structure	Scaling/new structure	Stacking
Technology Required	High selectivity through precise ion control Low-damage process Profile control (vertical, etc.)	Small CD*3, high aspect ratio capacitor etch Scaled mask etch (EUV, multi patterning) HBM (increase in interconnect, etc.)	Fast and vertical high aspect ratio etch Depth monitoring and process control Within wafer uniformity control

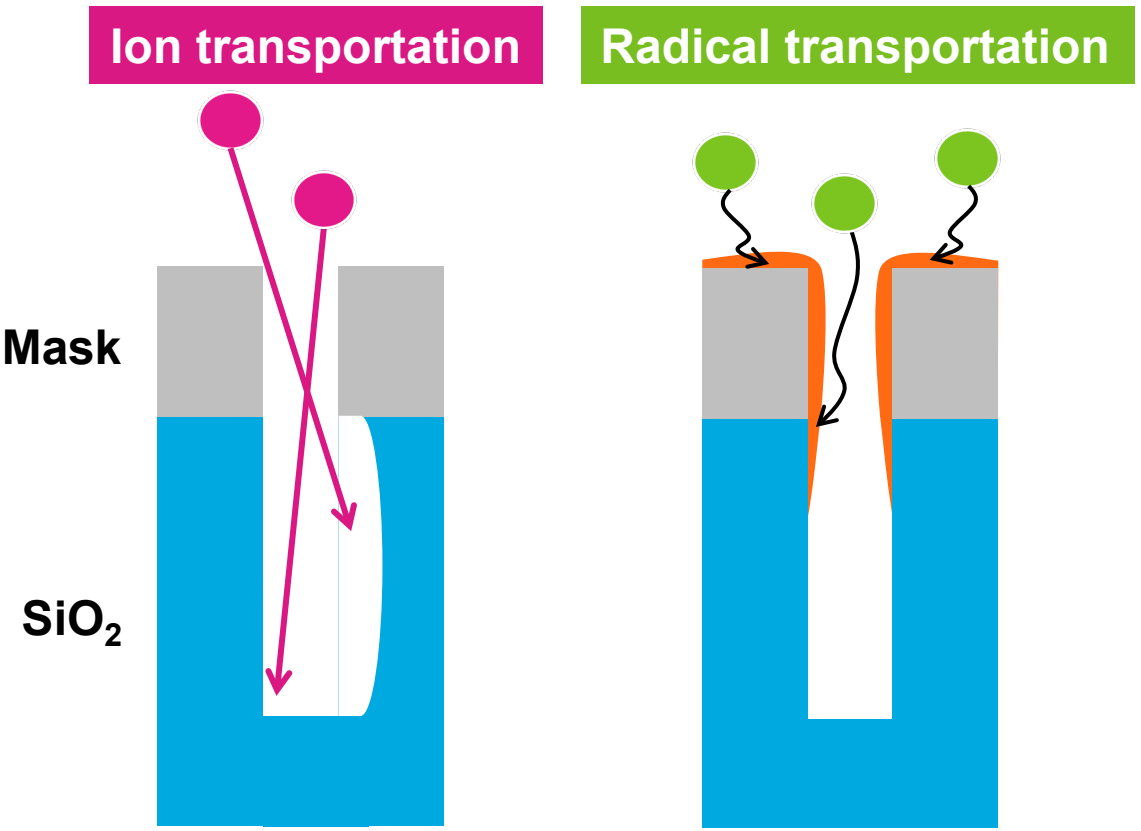
Etch technology with precise controllability is required for further evolution of devices

Overview of Etching and Key Parameters

Source of all drawings: TEL



Key Parameters for Etch Controllability



- Ion energy
- Ion incident angle

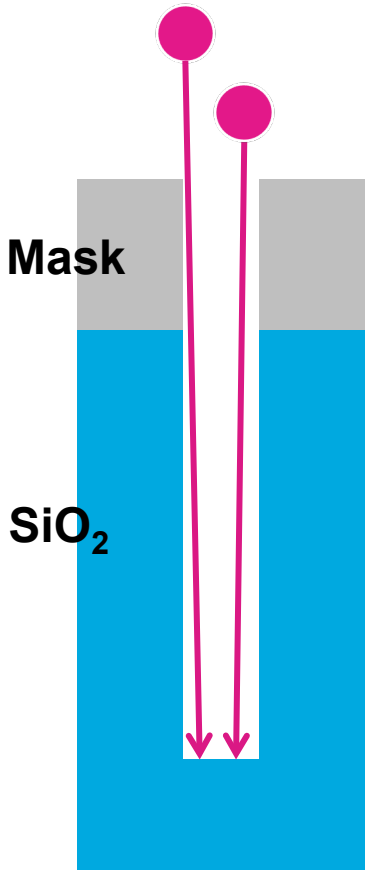
- Gas species
- Wafer temperature

Our Unique Technology 1: HERB™

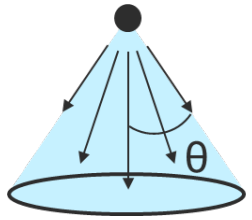
Source of all drawings: TEL

(HERB™: High Efficiency Rectangular Bias™)

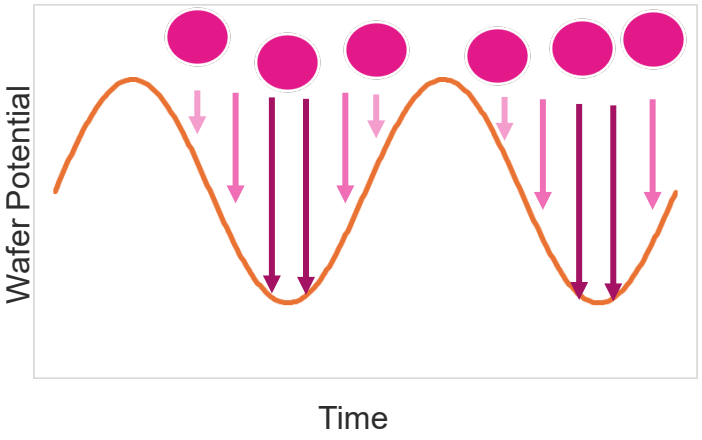
Ion transportation



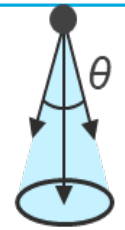
Conventional Technology (Sine wave)



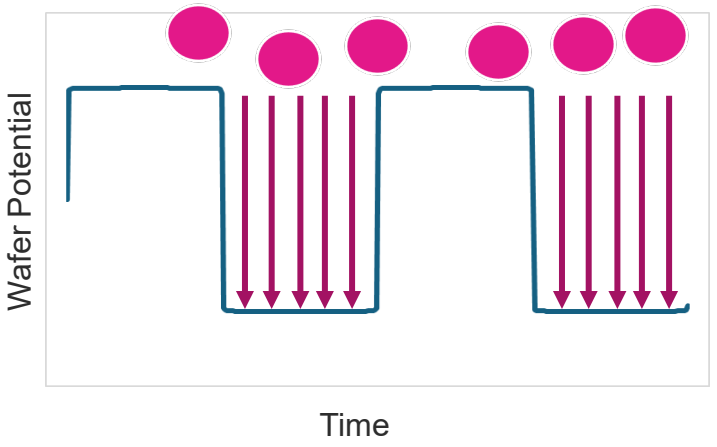
The force attracting ions varies
→incident angle varies



Novel Technology (HERB™)



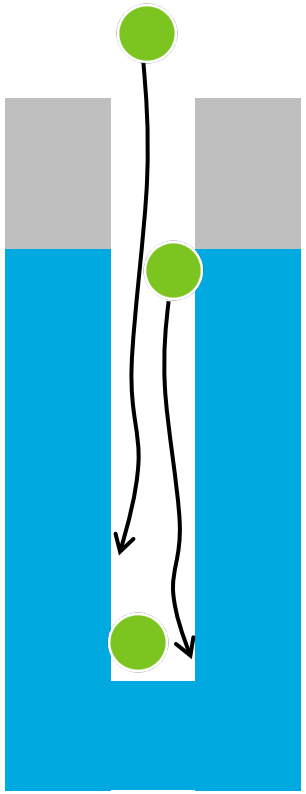
Force attracting ions are strong and consistent
→incidence angle becomes perpendicular



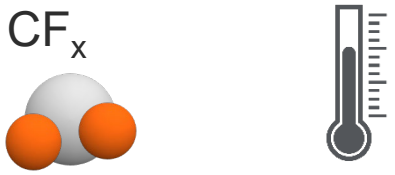
Our Unique Technology 2: PHastIE™

Source of all drawings: TEL

Radical transportation

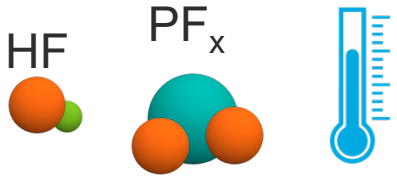


Conventional Technology (CF_x + room temp.)



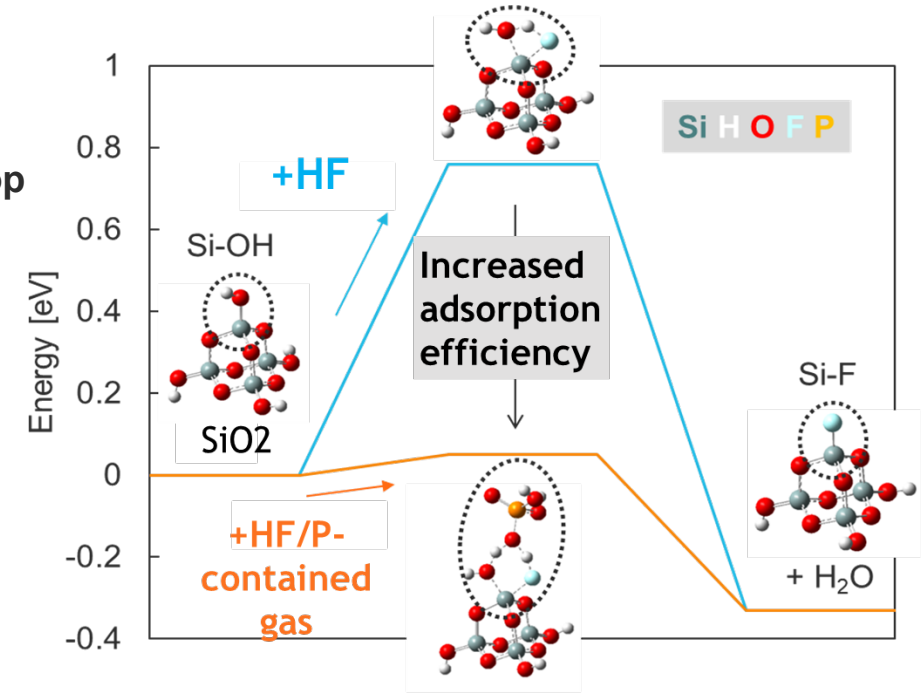
CFx tends to polymerize/adsorb easily
Hinders transportation when accumulated at top

Novel Technology (PHastIE™)



Resolved the issue with novel gas
Achieved high etch rate in combination with low temp.

(PHastIE™: Phosphorus + Hydrogen based "Fast" Ion Etch™)



Novel Cryogenic HARC Etch



Beyond



10μm

2.5x

Faster

Source: TEL

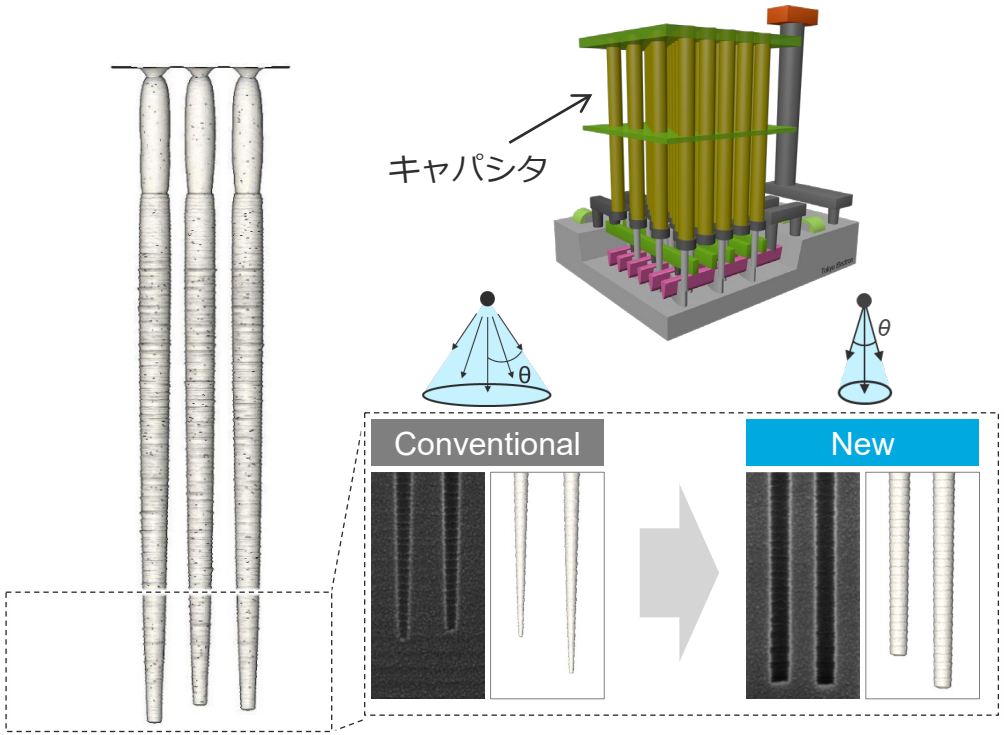
Process	Environment
Cryogenic temp.	**Power Consumption**
More Linear, Deeper & Faster	Less Power **-43%**
Plasma Control	**CO_2e** **-83%**
Deep-learning Optimization	Less Carbon Footprint

Presented world's first new cryogenic process in 2023 (@VLSI 2023), achieving both high process and environmental performance

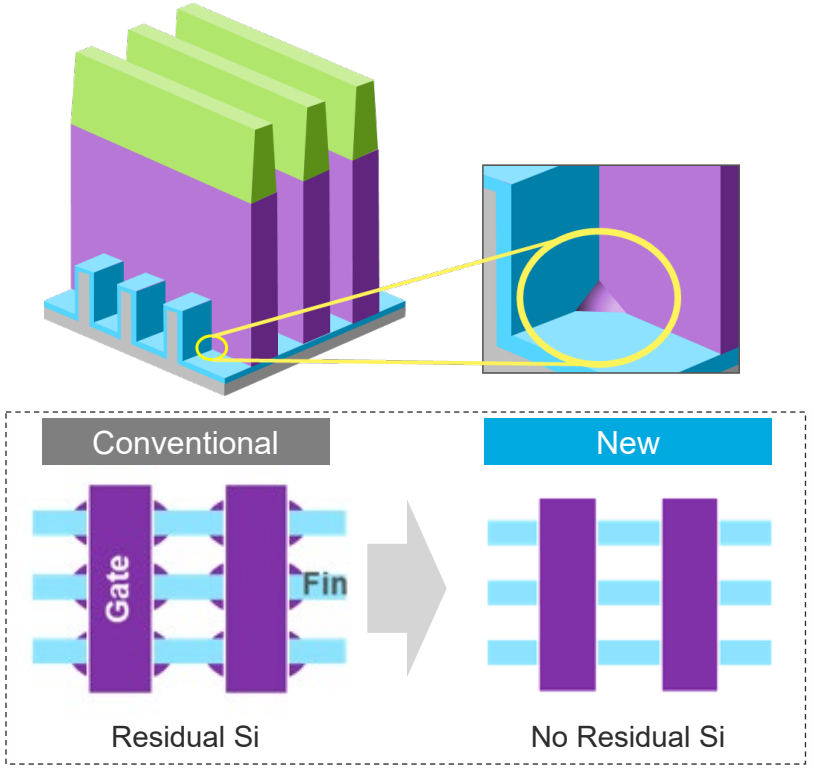
Future of New Etch Technologies

Source of all drawings: TEL

DRAM: Capacitor SiO_2 Etch



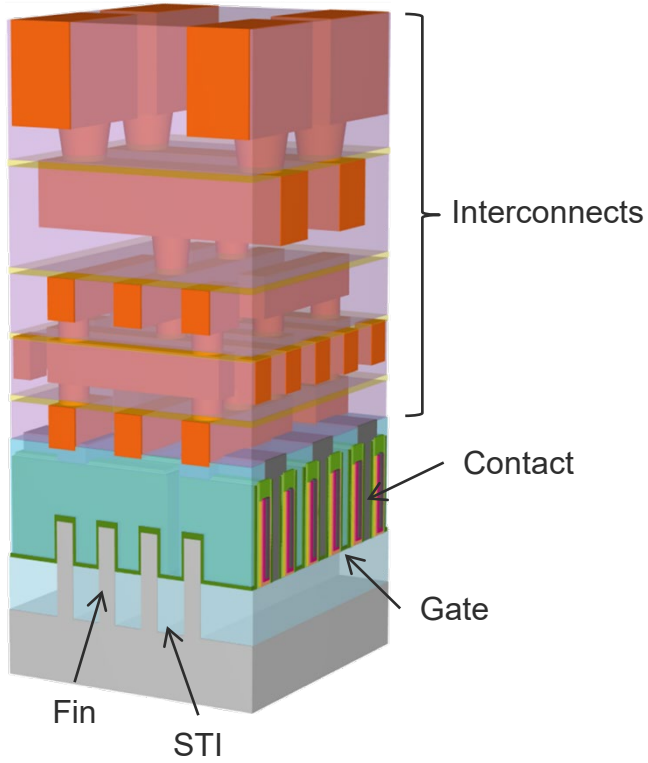
Logic: Gate Silicon Etch

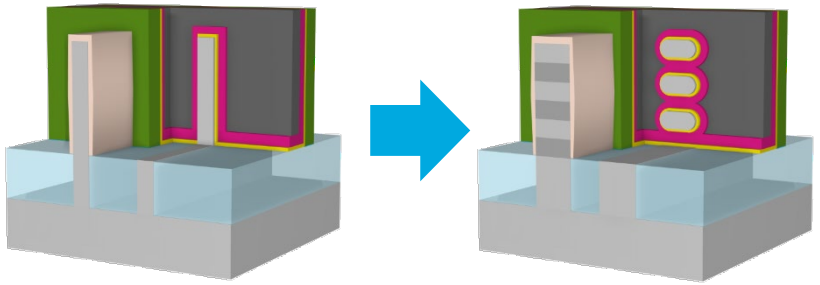


New technologies created through the development of ideal etching process development, will be applied to a variety of critical processes

Business Opportunities in Logic

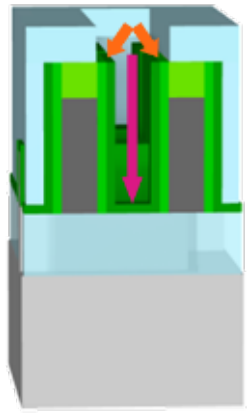
Source of all drawings: TEL



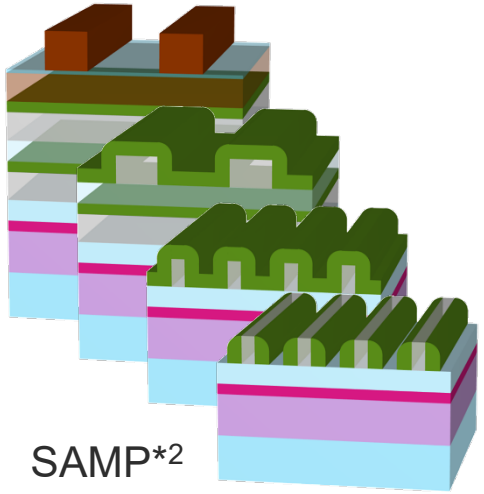


FinFET

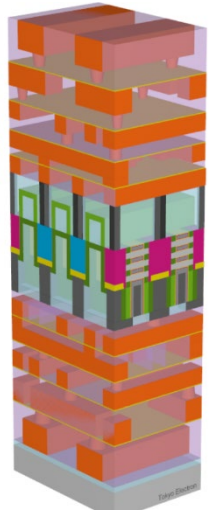
GAA*1 Nanosheet



Self-aligned Contact



SAMP*2



Backside PDN*3

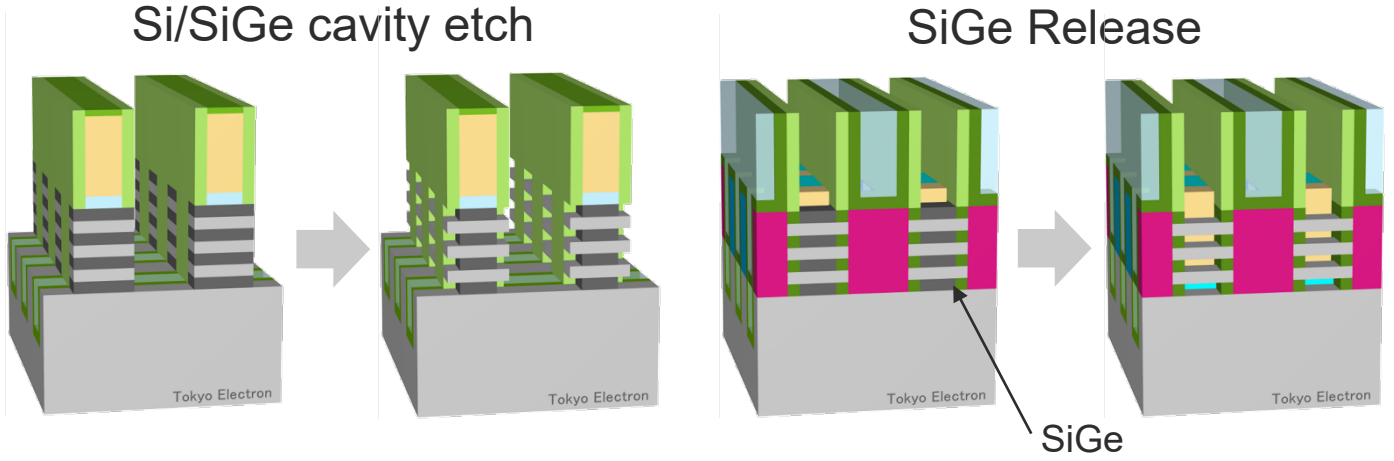
*1 GAA: Gate all around
*2 SAMP: Self-aligned multiple patterning
*3 PDN: Power delivery network

Respond to changes in device manufacturing and EUV lithography for further scaling

Initiative for GAA Nano Sheet Structures

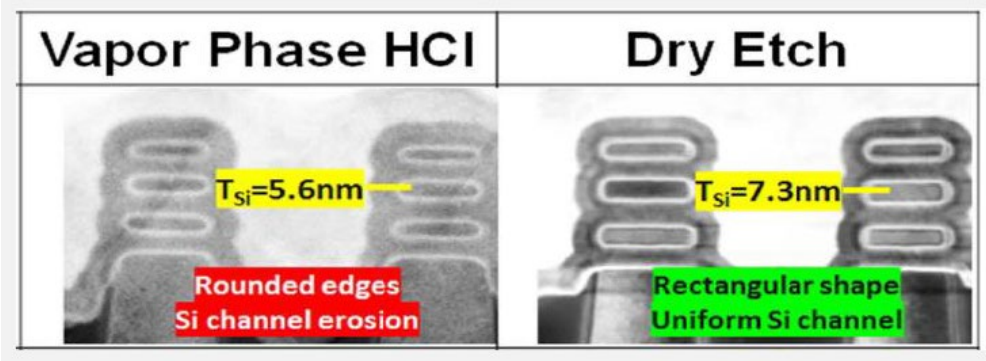
Nano Sheet process challenges:

- Uniformity in rectangle shape
- Mitigation of roughness/residue on patterned surface



TEL's initiative: Gas chemical etch

- High etch selectivity
- High uniformity
- Residue removal/decreased roughness



Source: N. Loubet, et al., IBM, TEL Technology Center, America (IEDM2019)

Leveraging the advantages of gas chemical etch to contribute to leading-edge processes

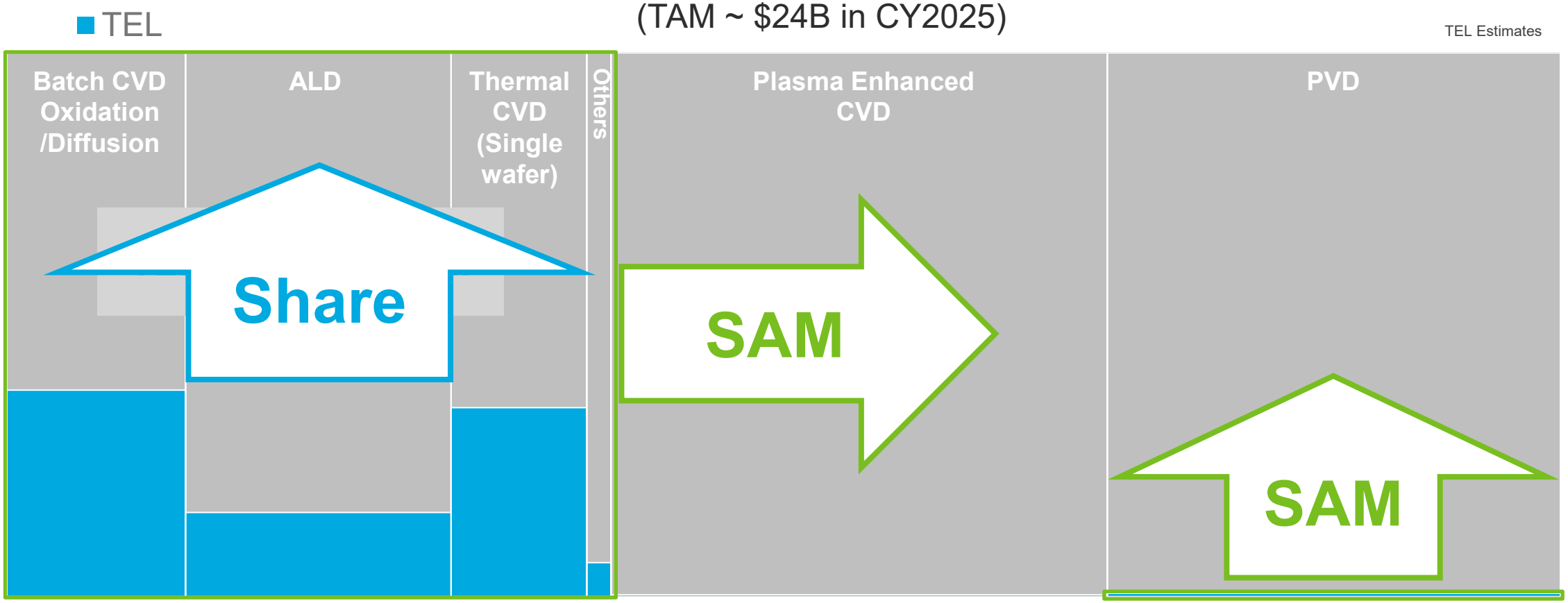
7-1-3. Deposition System

Business Strategy in the Thin Film Deposition Market

Expanding Market Share and SAM*

TEL's Market Share and SAM in Thin Film Deposition

(TAM ~ $24B in CY2025)



* SAM: Served Available Market

Strategies in the Deposition Business 1:
Expand SAM with Single Wafer CVD

Triase+™



Single Reactor
Existing Platform

Episode™ 1



Single Reactor
Equipped with up to eight process modules

Episode™ 2 DMR*



***Duo Matched Reactor**
Achieved high productivity
by processing 2 wfs/PM

Episode™ 2 QMR**



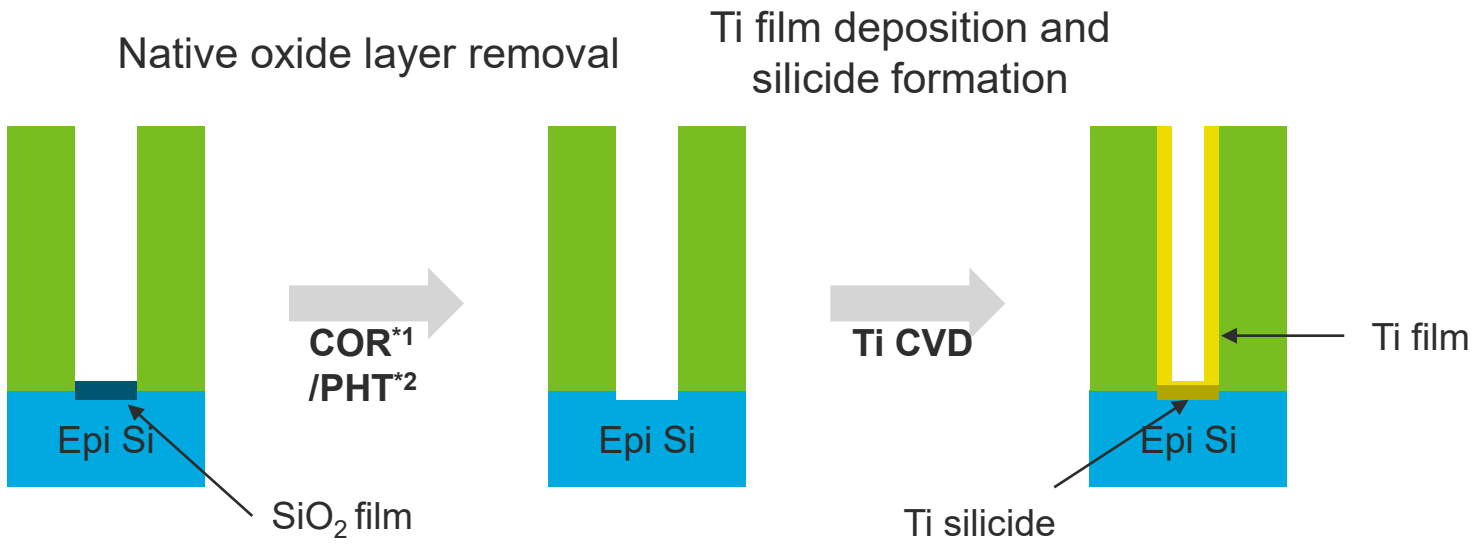
****Quad Matched Reactor**
Equipped with a newly developed
high-density plasma source

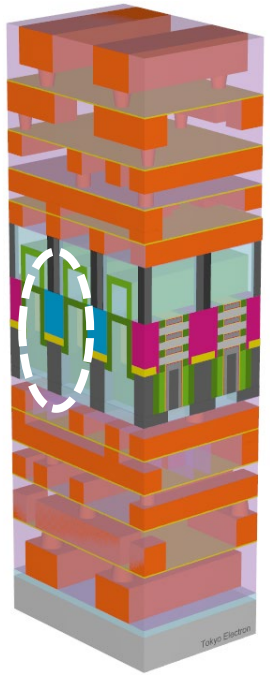
Upcoming Release

Episode™ 1: Contact Formation Process

Source of all drawings: TEL

- Example of process flow





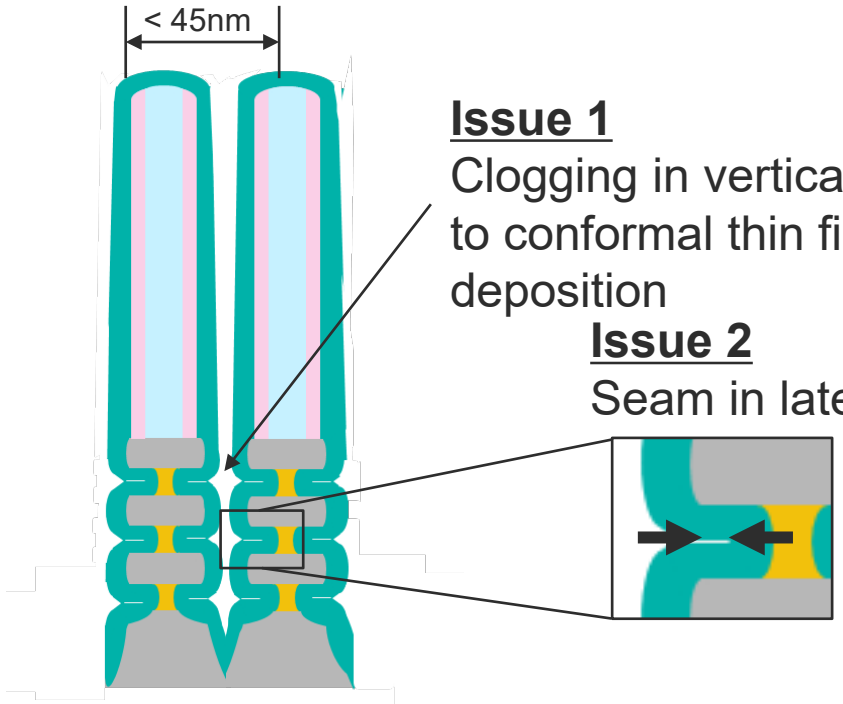
*1 COR: Chemical Oxide Removal
*2 PHT: Post Heat Treatment

Multiple types of process modules are equipped on a high-vacuum transfer module, and low-resistance contacts are achieved by sequentially processing native oxide layer removal and metal film formation

Episode™ 1: Inner Spacer Formation - Lateral Gapfill

Source of all drawings: TEL

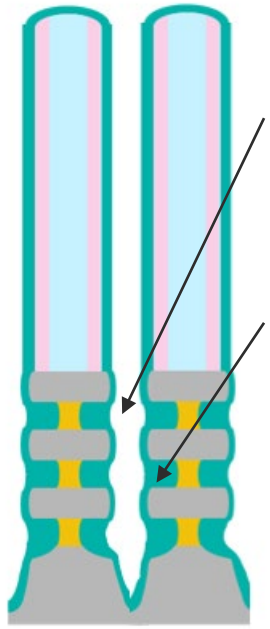
- Issues :
  Leak due to dielectric breakdown due to etching



Issue 1
Clogging in vertical gap due to conformal thin film deposition

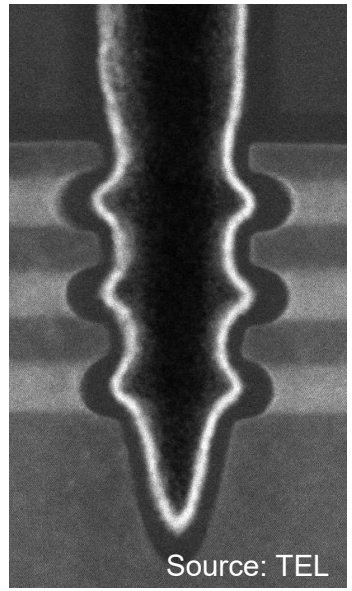
Issue 2
Seam in lateral gap

- Solutions :
  Improve lateral gapfill performance



Solution 1
Thinner film deposition on the side walls

Solution 2
Seamless gapfill in lateral gap



Realized seamless lateral gapfill using a unique thin film deposition technique and laterally uniform film modification using a newly developed high-density plasma

Strategies in the Deposition Business 2:

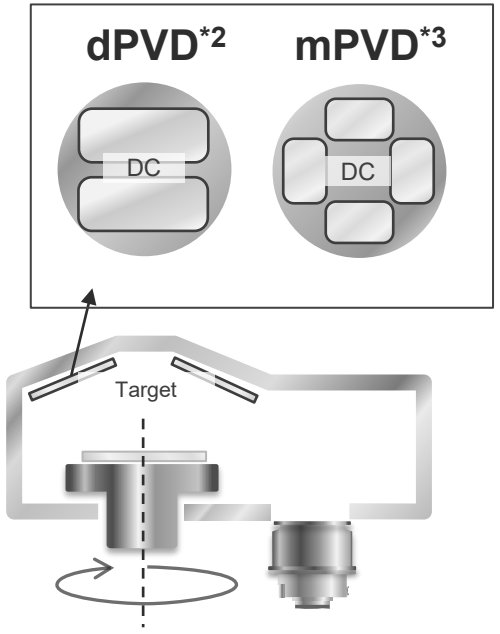
SAM Expansion with PVD

Source of all drawings: TEL

LEXIA™ -EX

- Oblique angle sputter with wafer rotation system
  - Excellent thickness uniformity (1σ 0.5%)
- Unique multi-cathode*1 configuration
  - High deposition rate
  - Capability of tuning film composition ratio with multiple materials
- High throughput (~100WPH)
- Significant footprint reduction vs conventional model





*1 Cathode: An electrode for material deposition
*2 dPVD: Dual cathode PVD
*3 mPVD: Multiple cathode PVD

Strategies in the Deposition Business 3:
Growth in Batch Thermal Process/Deposition



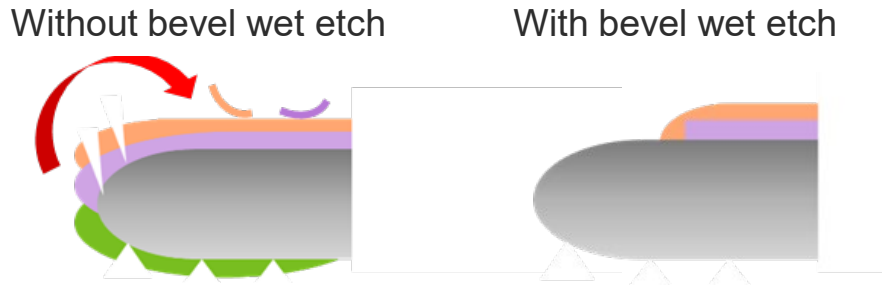
EVAROS™

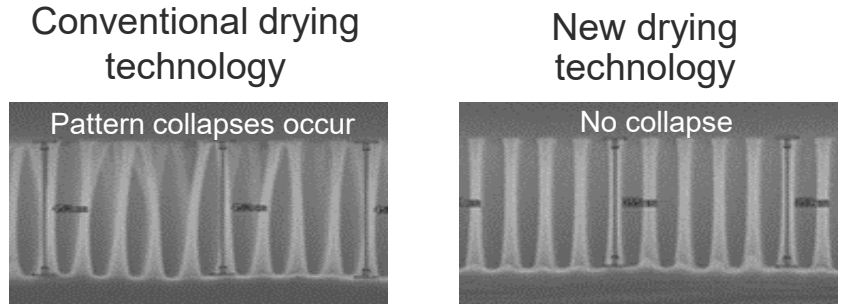
- Major applications: ALD and CVD
  - General silicon processes (contact Si, channel Si, etc.)
  - ALD processes (SiN, SiO2)
  - PE-ALD processes (SiN)
- Features
  - Maximum 200 wafers per batch
  - Larger reactor exhaust diameter to improve exhaust conductance, enabling uniform deposition on large-surface-are patterns
  - 25% less CO_2 emissions per wafer vs TELINDY PLUS™
  - Enhance labor reduction (one-touch start-up, self-maintenance, DX)

7-1-4. Cleaning System

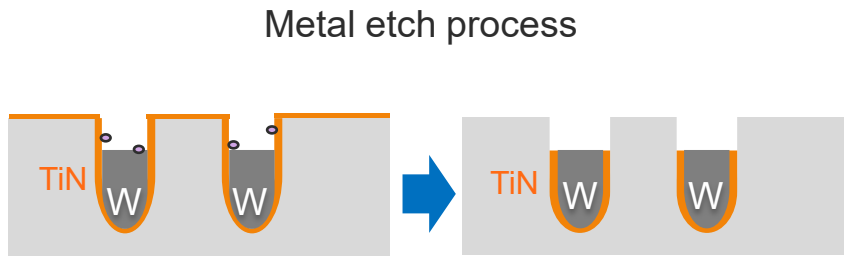
Single Wafer Cleaning Strategy

- Single wafer cleaning
  - Bevel wet etch
    - Expect annual market growth rate of around 10%
    - Contribute to improving customers' yields. Maintain a high market share by differentiating through performance in precisely removing film from the outer part of the wafer
  - Prevent pattern collapse
    Expand market share by TEL original technology to reduce collapse of high aspect ratio pattern
  - Metal etch
    Launched new dedicated SPM chambers for controlling selectivity for metal in order to solve reduced yield issues caused by dry etch damage and residue



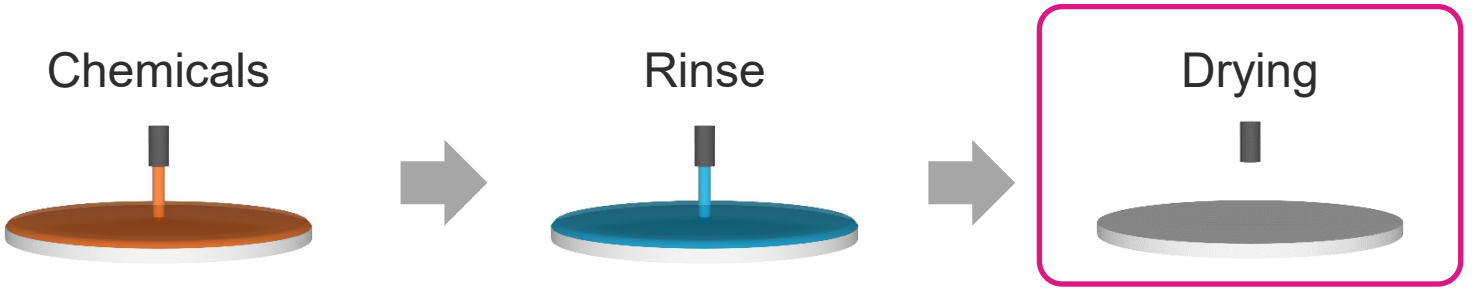


Source: TEL

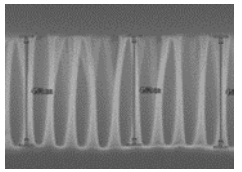


Source of all drawings: TEL

Technology Challenges in Cleaning for State-of-the-Art Devices

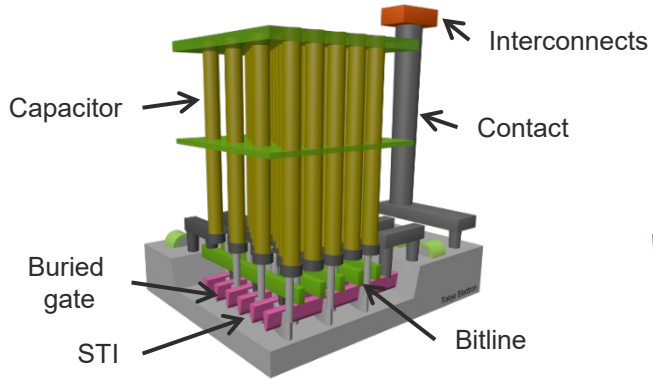


Pattern collapse

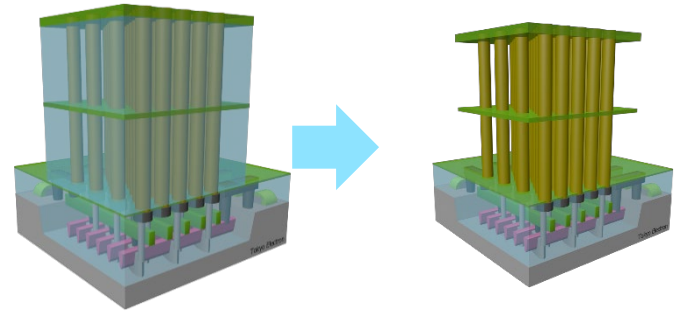


Source: TEL

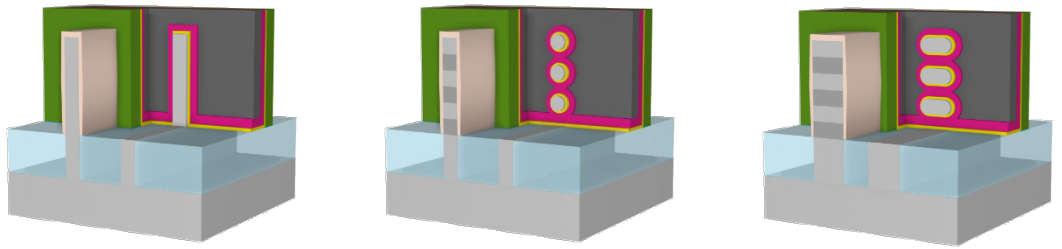
- DRAM
  - Post-STI etch cleaning
  - Mold wet etch after capacitor electrode formation



Wet etch



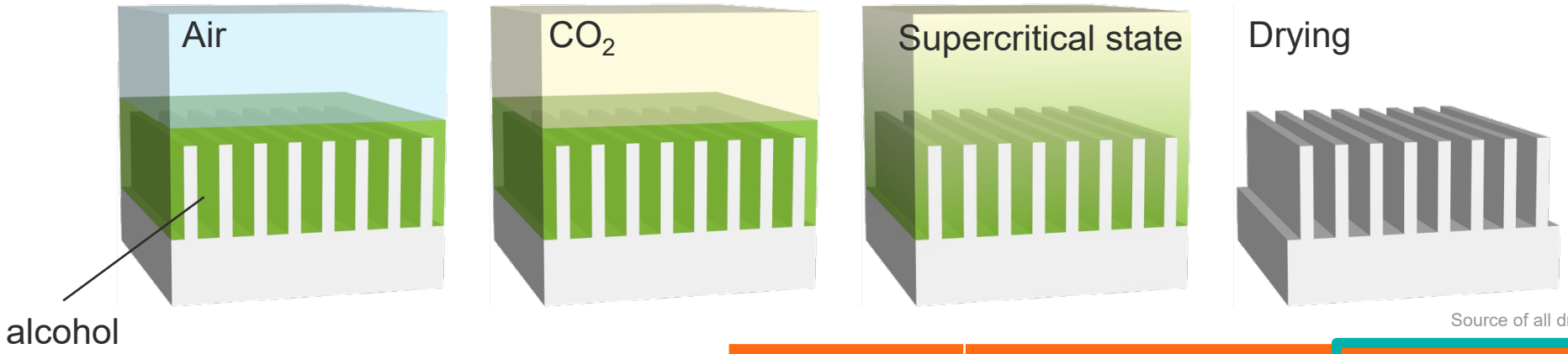
- Logic
  - Post-fin etch cleaning
  - Post-nanowire/nanosheet formation cleaning



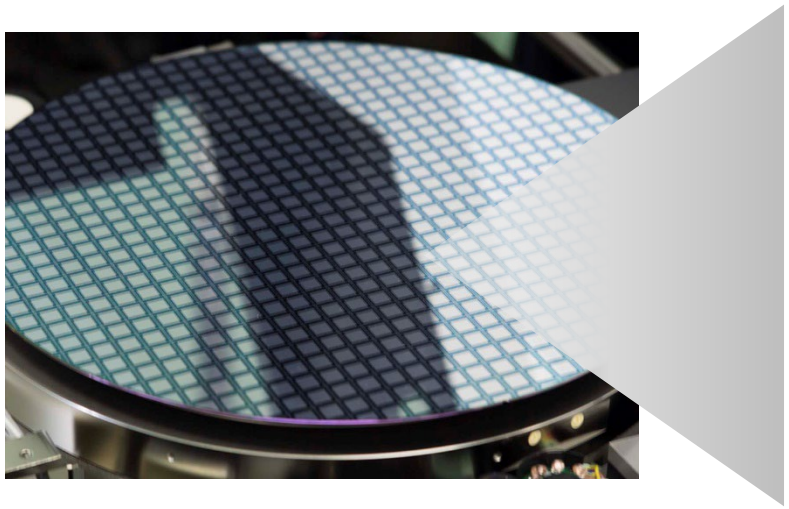
Source of all drawings: TEL

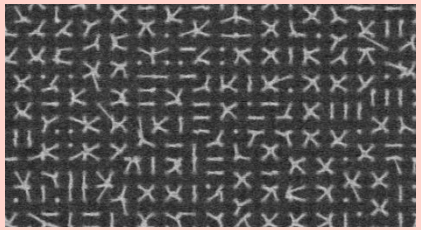
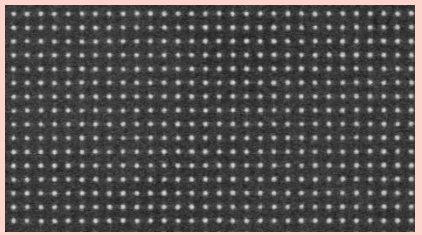
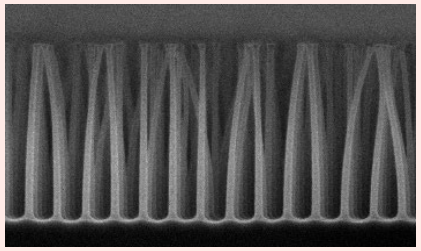
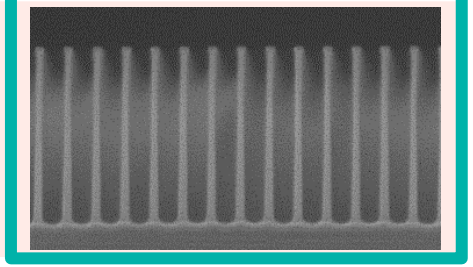
Drying technology more difficult due to further scaling and higher aspect ratios in device manufacturing

Supercritical Drying Technology



Source of all drawings: TEL



	Traditional drying	TEL's supercritical drying
Top View		
Side View		

Source: TEL

Supercritical drying technology prevents pattern collapse

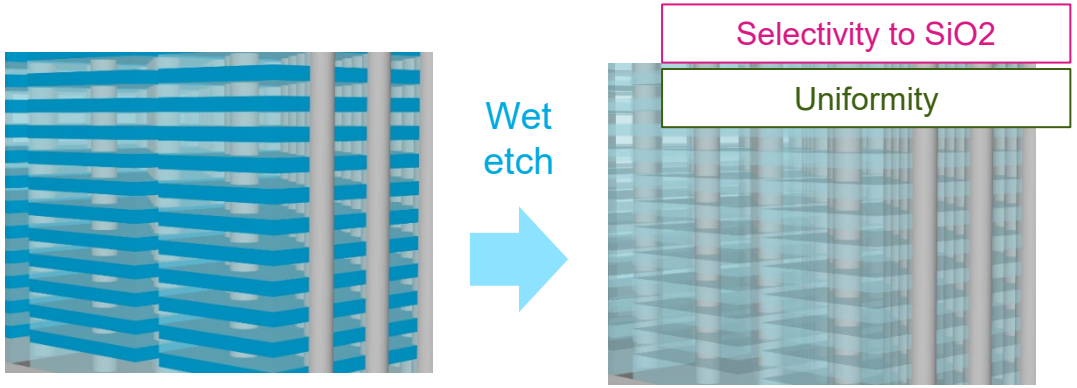
Batch and Scrubber Cleaning Strategy

- Batch cleaning
  - SiN etch and W etch processes for 3D NAND
    Focus on processes that require long durations and advanced process technology. Differentiate by realizing high uniformity, high selectivity and high productivity in wet etch

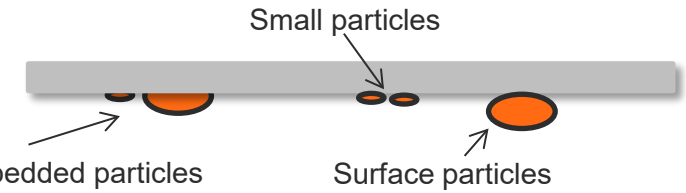
- Scrubber cleaning
  - Pre-lithography process
    Provide high-value solutions such as reducing particles brought in by wafers, contributing to the improvement of exposure tool availability which have grown increasingly important due to the introduction of EUV

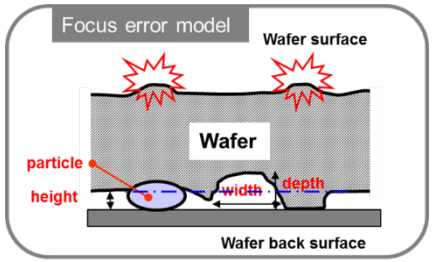
Source of all drawings: TEL

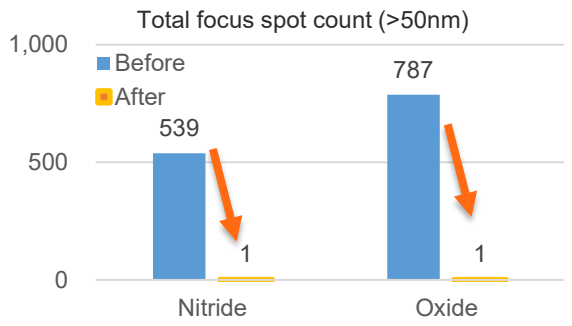
SiN etch process



Wafer back and defocus diagram



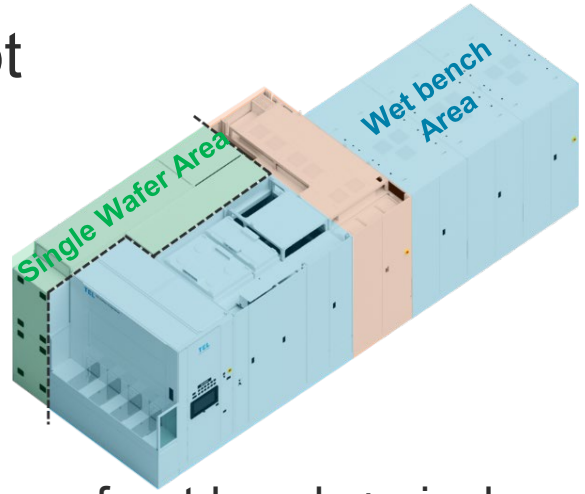




ZEXSTA™

Source of all drawings: TEL

- Concept



A combination of wet bench + single-wafer process

Method	Features
Wet Bench	High-temp/ long-duration process, wet etch
Single Wafer	Advanced drying technology, particle control

- Target Application
  - Advanced wet etch + advanced dry tech



    - Highly selective wet etch process will be required for also 3D DRAM in addition to 3D NAND
  - High throughput + surface cleanliness



    - High surface cleanliness is required for logic and DRAM

TEL will contribute to customer technology development by continuing to create new value, overcoming the constraints of traditional equipment classifications

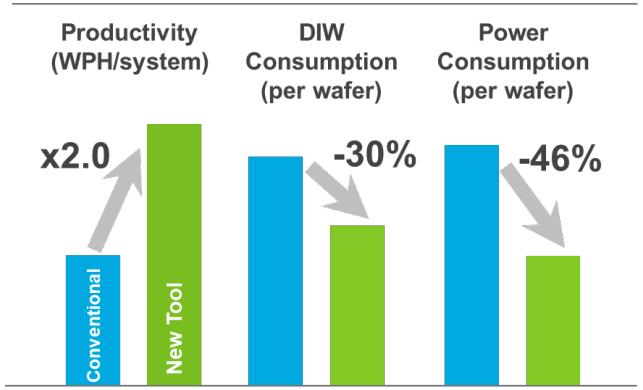
Development of Cleaning Systems

Source of all drawings: TEL

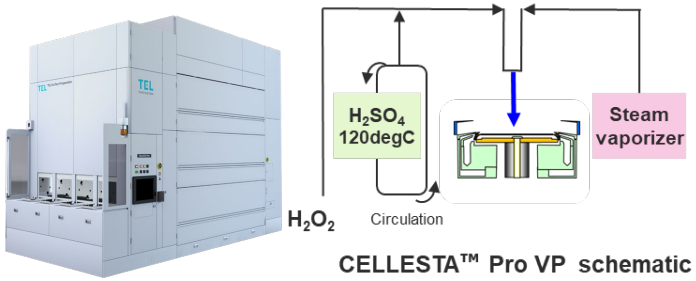
High Productivity Wet Bench (EXPEDIUS™-R)



Industry's first large-batch process (increased wafer counts)



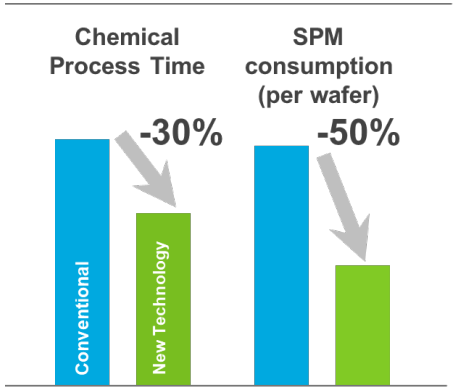
SPM*1 Vapor Technology (CELLESTA™ Pro VP)



CELLESTA™ Pro VP schematic

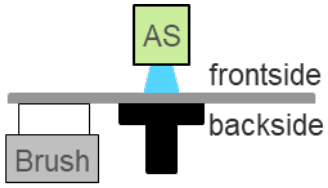
Enabled higher temperature process due to a more effective rection by adding water vapor to chemicals

*1 SPM: Sulfuric Acid and Hydrogen Peroxide Mixture



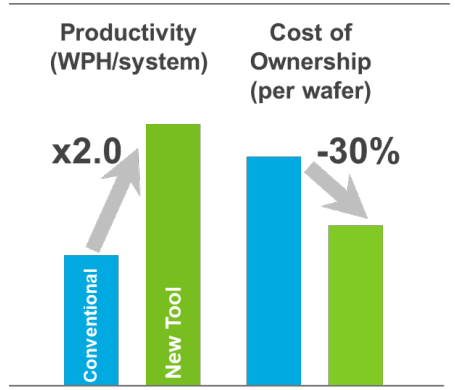
Simultaneous Scrubber (CELLESTA™ MS2)





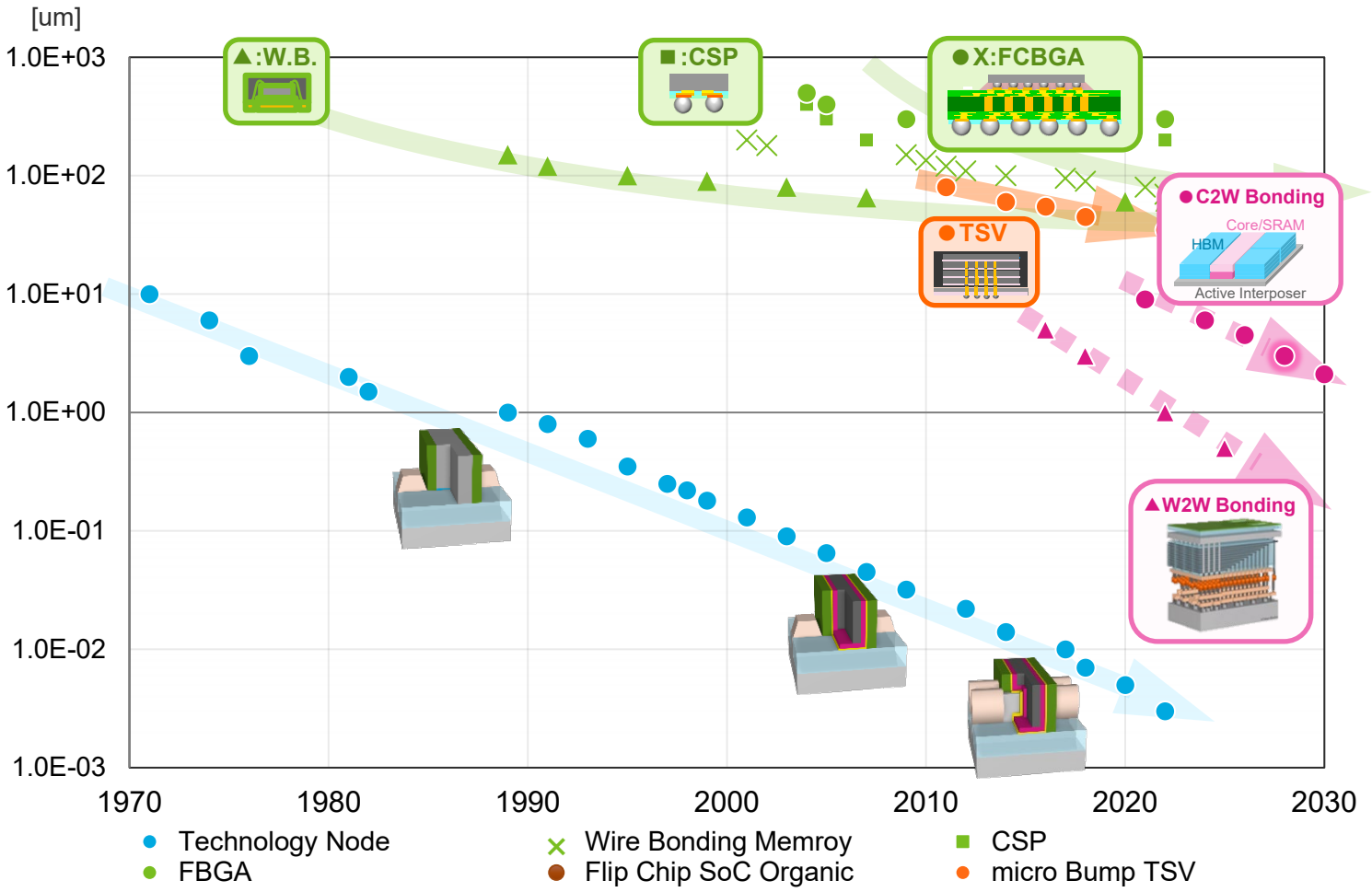
A tool enabling AS*2 process on wafer frontside and physical brushing process on wafer backside simultaneously in a single chamber

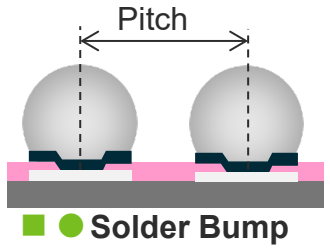
*2 AS: Atomized Spray

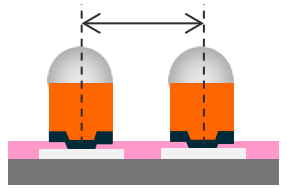


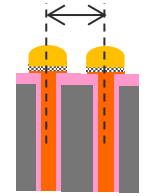
7-2. Backend Business Strategy

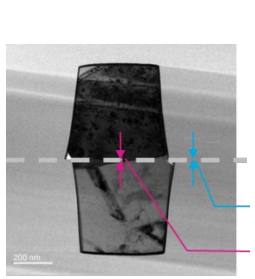
Semiconductor Technology Node and Bump Pitch

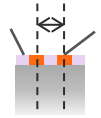












Wafer Bonding

● ▲ Cu Hybrid Bonding

Introduction of wafer bonding technology accelerates further reduction of pitch

History of Product Launches in Assembly and Test*1 Systems

New Category Product　Next Generation/Improvement Product

Synapse™ S
Fusion bonder



Synapse™ V
Temporary bonder



Synapse™ Si
Cu hybrid / Fusion wafer bonder



Prexa™
Wafer Prober



Ulucus™ L
Laser Edge Trimmer



Synapse™ Si (high accuracy)
Cu hybrid / Fusion wafer bonder



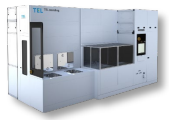
Ulucus™ LX
Extreme Laser Lift Off



Prexa™ SDP*2
Device Prober

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026

Synapse™ Z plus
De-bonder



Synapse™ ZF
Post bond re-worker



Ulucus™ G
Wafer Thinning



3DI
Upcoming system for release

Accelerating product development to prepare for the era of 3D integration

*Test : Prober for Advanced Packaging Test
*2 SDP：Singulated Device Prober

Source of all drawings: TEL

3DI / Test Business Expands Opportunities for HPC/AI Device

Frontend Process

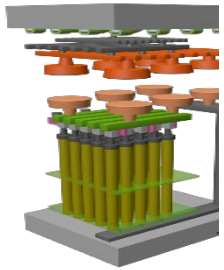
Device Manufacturing



BSPDN*1



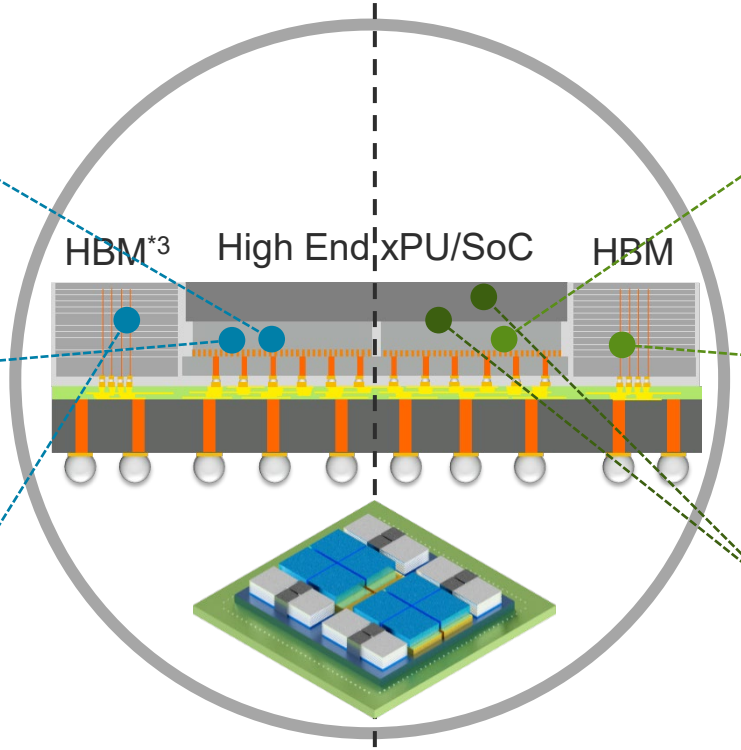
CFET*2



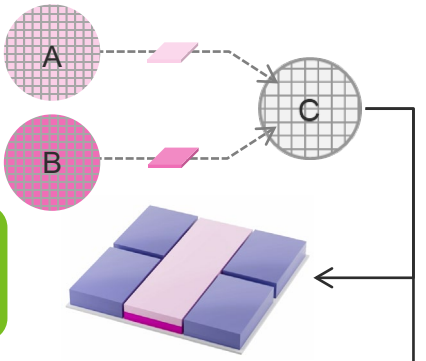
DRAM

Advanced Packaging

Assembly after Dicing/Singulation



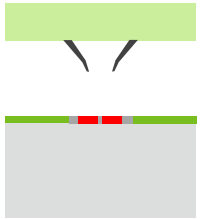
3DIC



Stack Memory



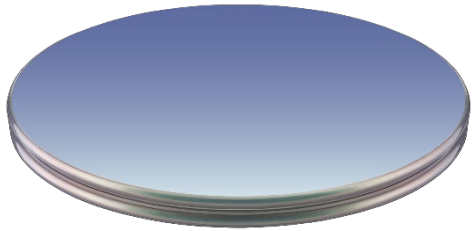
Die Test for KGD*4



*1 BSPDN: Back Side Power Delivery Network
*2 CFET: Complementary Field Effect Transistor
*3 HBM: High Bandwidth Memory
*4 KGD: Known Good Die

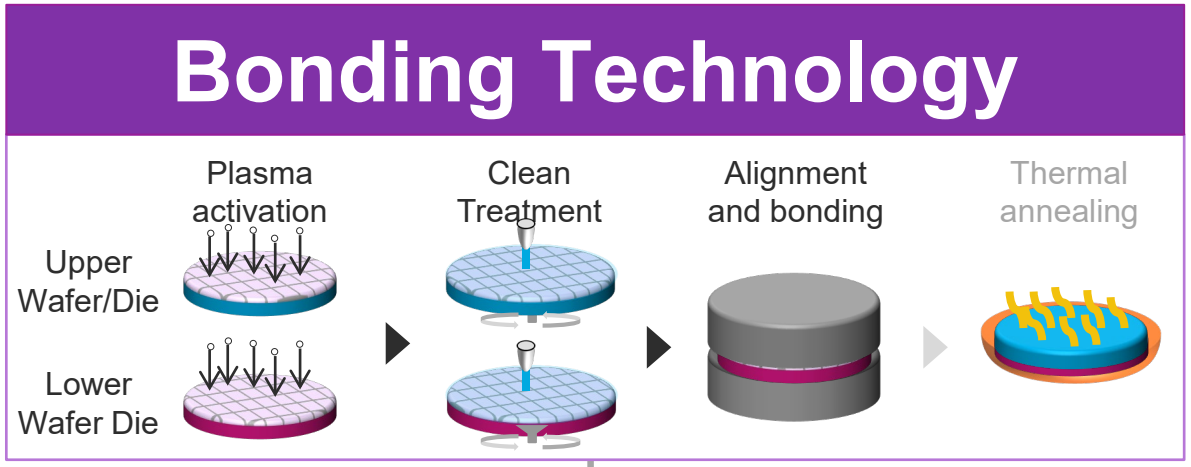
Source of all drawings: TEL

TEL's Opportunities for Bonding Technology

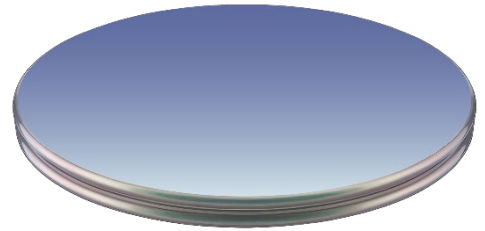


Wafer-to-Wafer Bonding

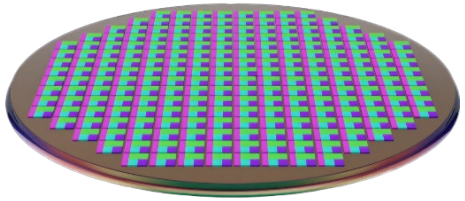
Bonding Technology



Benefits for Pitch scaling & Higher speed / Lower power consumption



Wafer-to-Wafer Bonding



Die-to-Wafer Bonding

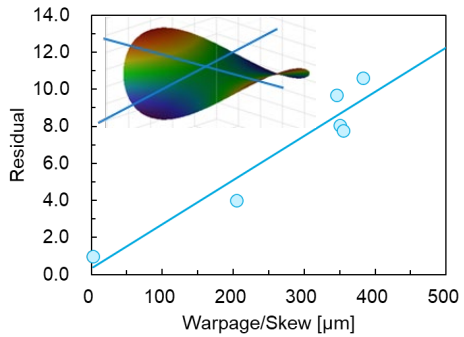
Frontend Process

Advanced Packaging

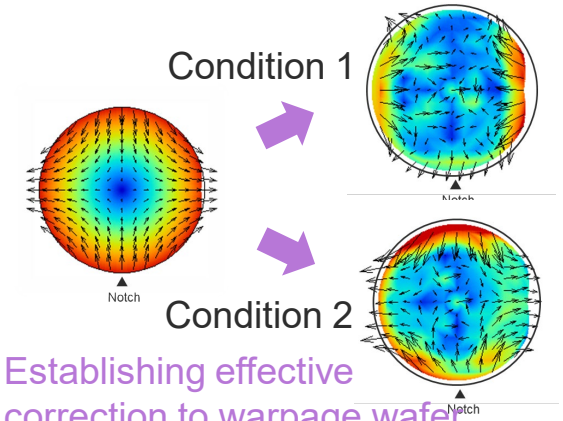
Wafer Bonder Technology Roadmap and Challenges

CY	2025~26	2027	2028	2029	2030~31	2032~33	2034~35	Beyond
Logic	BSPDN (2nm/18A)	(16A)	(14A)	(12A)	(10A)	(7A)	(5A) CFET	(3A)
	Distortion ≤ 4nm			Distortion ≤ 3nm			Distortion ≤ 2nm	
NAND	2-wafer-bonding				3-wafer-bonding		4-wafer-bonging	
	Wafer warpage < 500μm						Wafer warpage > 500μm	
DRAM	6F² DRAM			6F² + Peri Bonding/4F² VCT/3D DRAM				
				Distortion ≤ 3nm / DxDy < 50nm				

Wafer Warpage Challenges and Actions

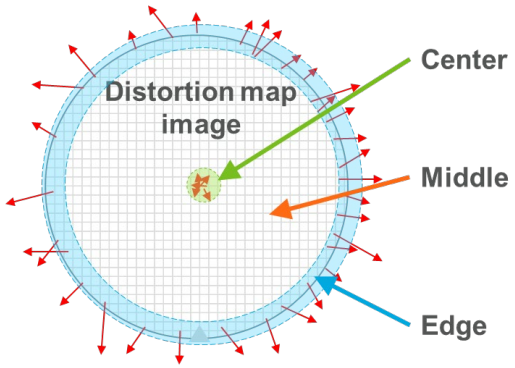


Relation between wafer warpage and residual (distortion)

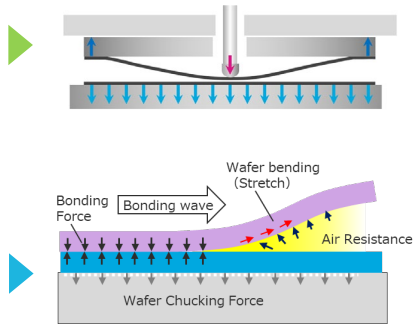


Establishing effective correction to warpage wafer

Distortion Challenges and Actions



Distortion vector

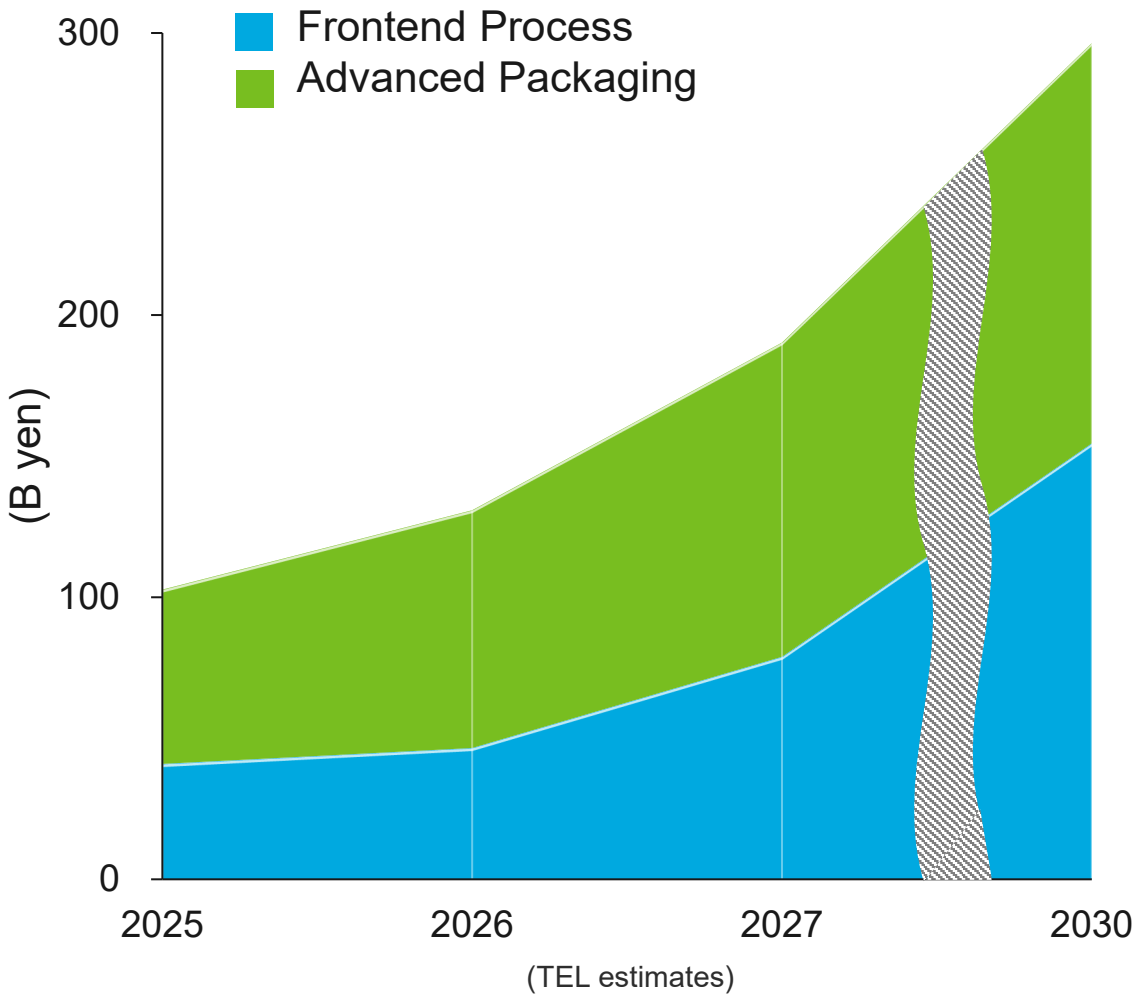


Optimizing hardware and process

Source of all drawings: TEL

TEL is developing various technologies in advance to prepare for next-generation devices

Bonding Process Equipment TAM*



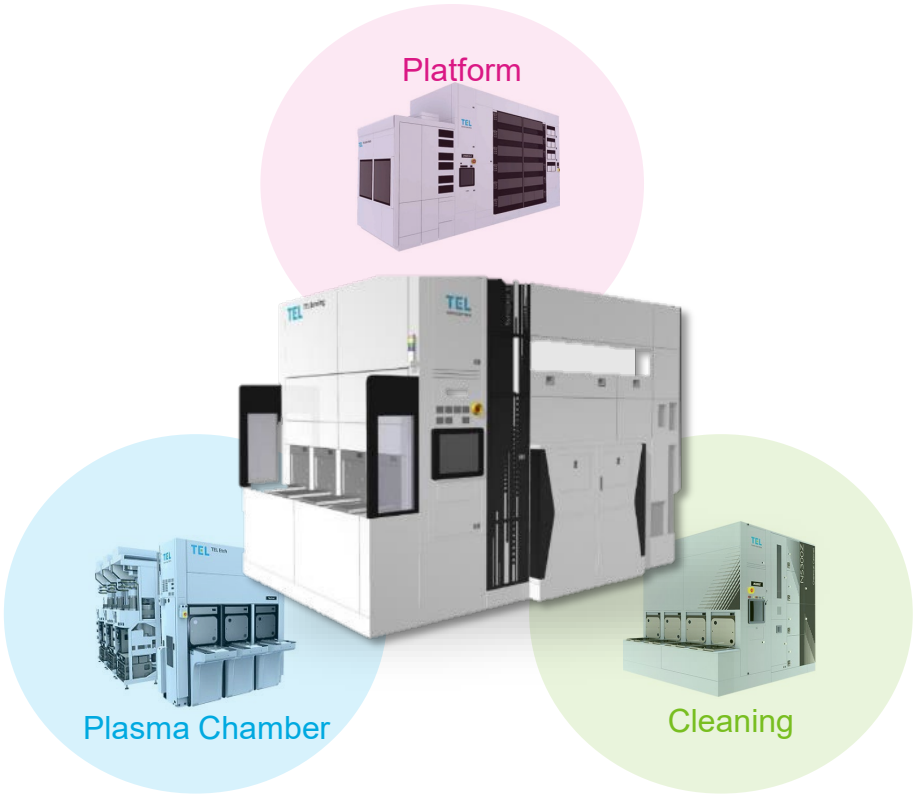
Anticipating a TAM CAGR of 24% from CY2025 to CY2030

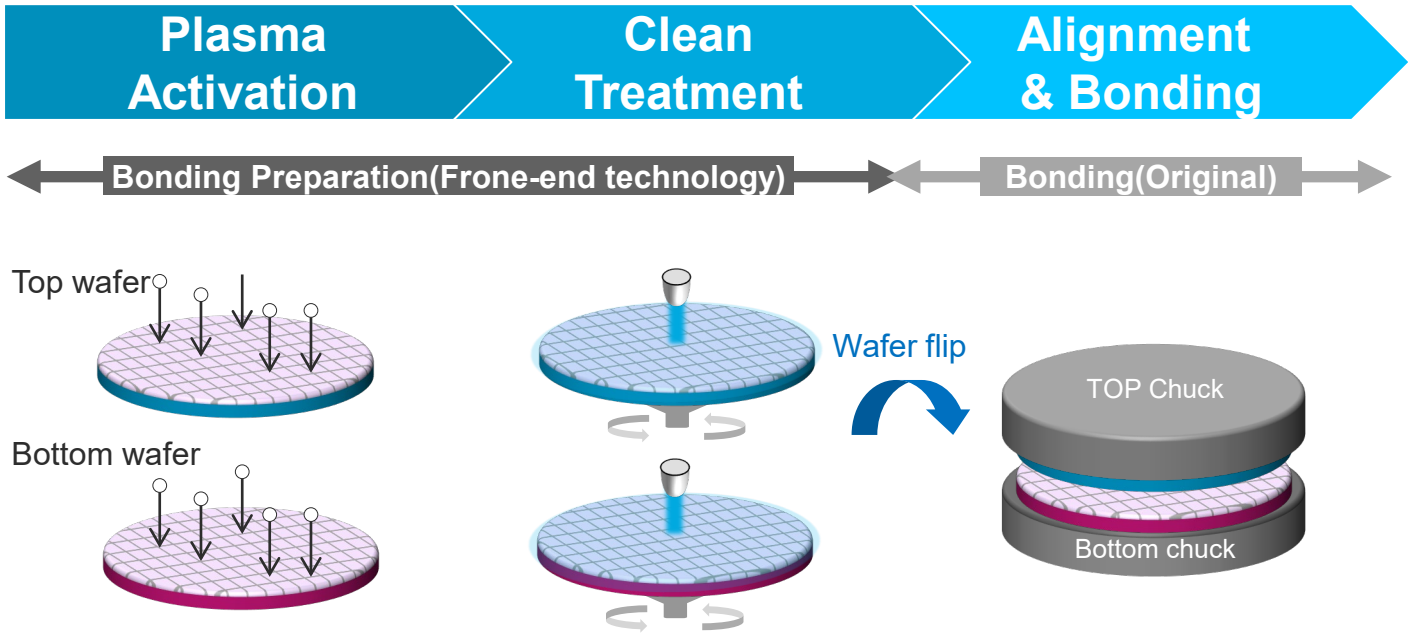
- Projected to achieve 300 billion yen by CY2030
- Encompassing both frontend processes and advanced packaging equipment
- Addressing bonding/debonding, slicing, and thinning process equipment utilizing various technologies

* TAM : Total Available Market

Source of all drawings: TEL

Wafer-to-Wafer Permanent Bonder Synapse™ Si

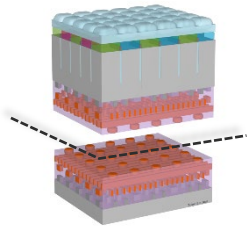
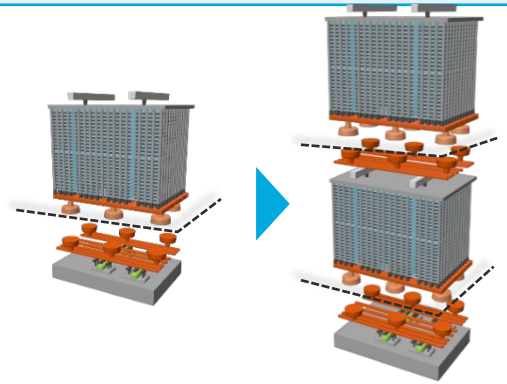
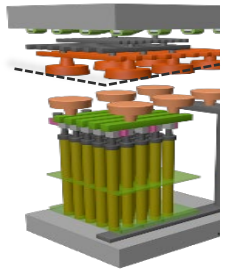
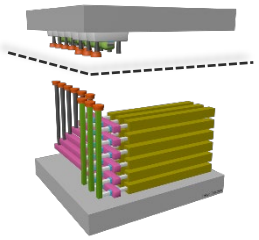
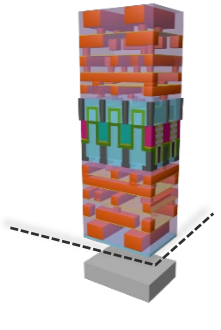
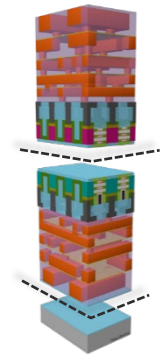




- TEL's existing broad technology and business contributing effective product development/CIPs
- Making good progress with major memory, logic customers towards high volume manufacturing
- Leading W2W Fusion/Cu hybrid bonding technology for next generation device manufacturing

Source of all drawings: TEL

Broad Applications and Expansion of Bonding Technology

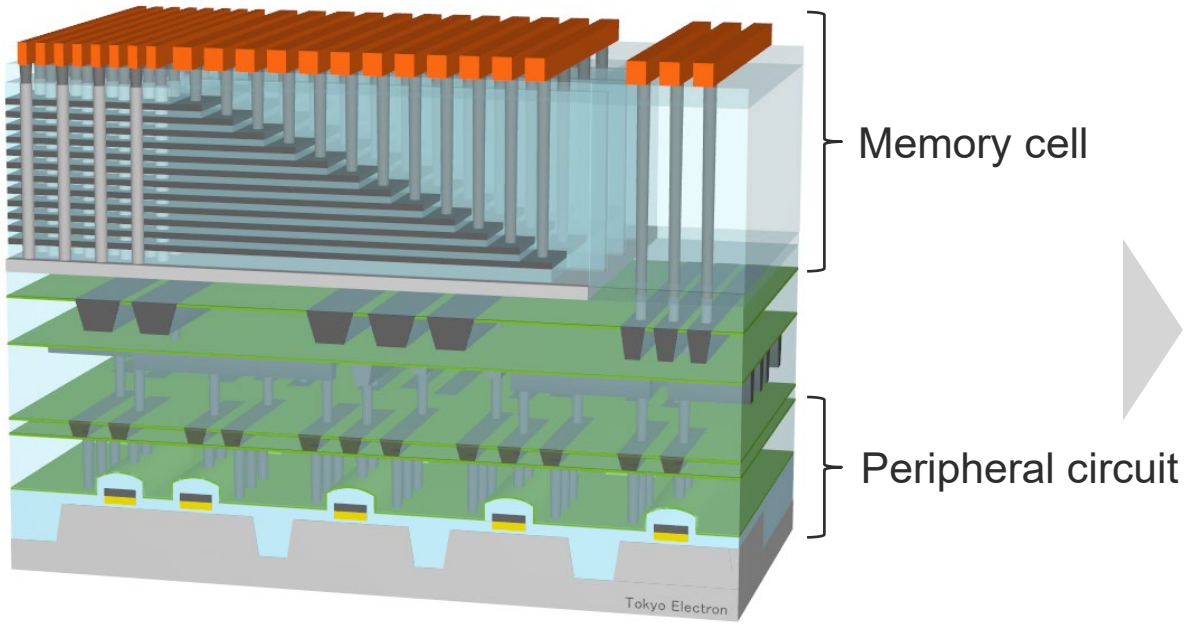
Application	Frontend Process					
	CIS[*1]	NAND		DRAM		Logic	
Stacking Device	BSI[*2] Pixel + (Peripheral) + Logic	3D NAND Cell + Peripheral ⋮ + Cell + Cell + Peripheral		VCT[*5] DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	3D DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	BSPDN Logic + Si Substrate	BSPDN & CFET Logic + Logic + Si Substrate
Bonding	Wafer to Wafer (CHB[*3]/Fusion)	Wafer to Wafer (CHB)		Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (HB[*6]/Fusion)	
Structure							
Status	HVM[*4]	R&D~HVM	R&D	R&D	R&D	R&D~HVM	R&D

The design of future devices is transitioning from single bonding to multi-bonding structures

*1 CIS: CMOS Image Sensor
*2 BSI: Backside Illumination
*3 CHB: Cu Hybrid Bonding
*4 HVM: High Volume Manufacturing
*5 VCT: Vertical Channel Transistor
*6 HB: Hybrid Bonding

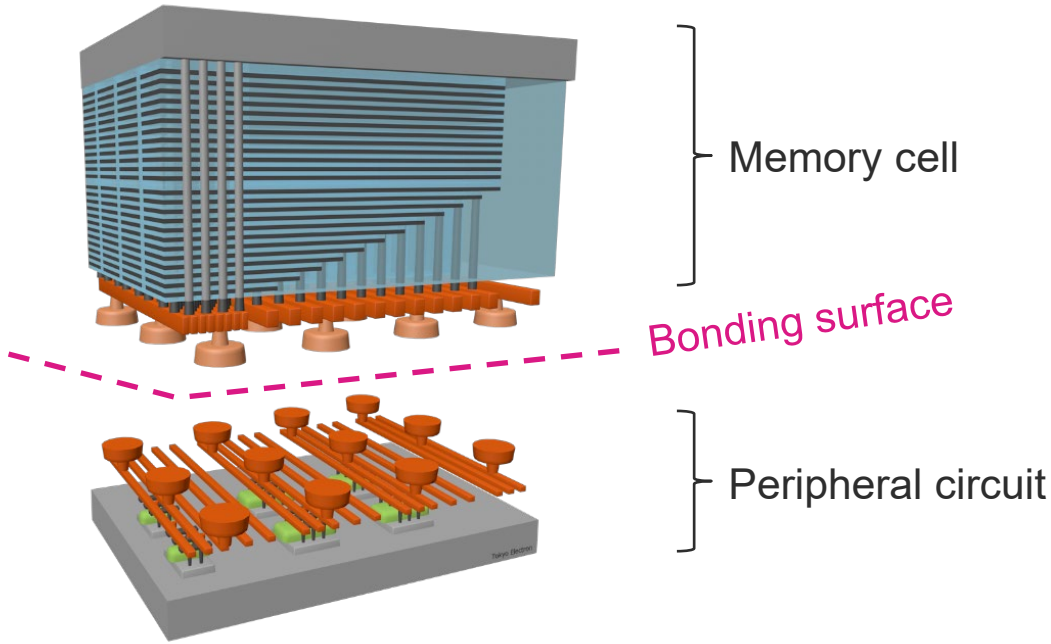
Wafer Bonding Application for 3D NAND

Current structure



- ✓ Peripheral circuit performance deteriorates due to exposure to high temperature during memory cell manufacturing
- ✓ Long interconnects wiring

New structure

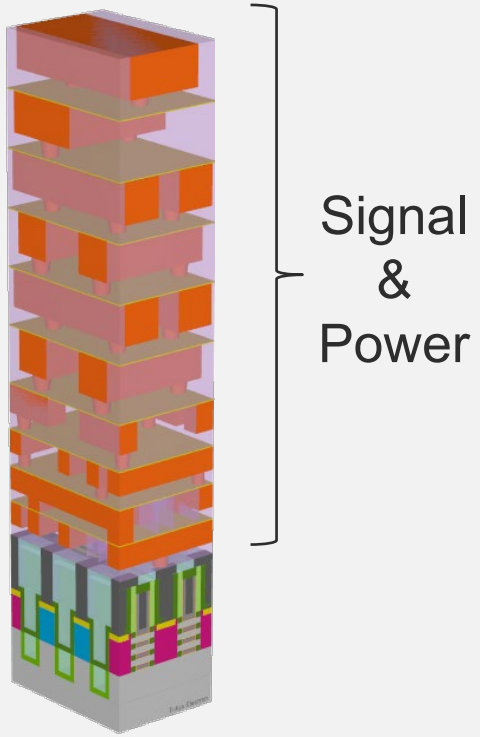


- ✓ Peripheral circuit is manufactured on the separate wafer and bond to the memory cell wafer
  - higher peripheral circuit performance
  - shorter TAT* process
- ✓ Shorter interconnects wiring

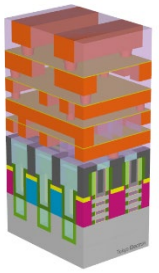
* TAT: Turnaround time

Wafer Bonding Application for Logic Backside PDN

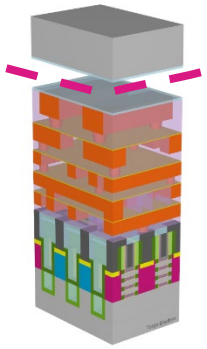
Conventional Structure



1. Signal BEOL (Front side)

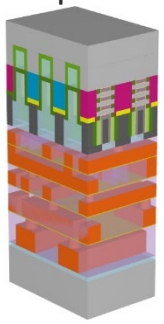


2. Si Wafer Bonding

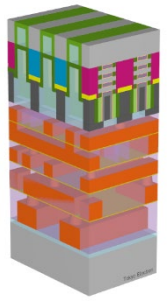


flip

3. Flip Wafer



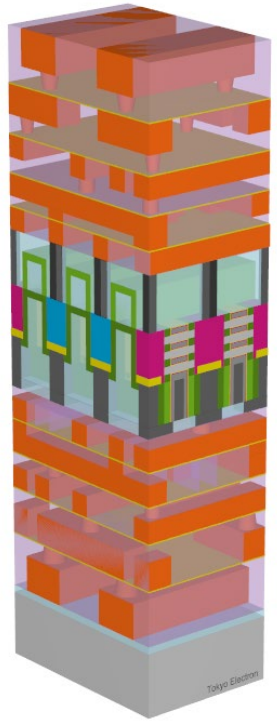
4. Backside Thinning



5. Power BEOL (Backside)

Backside PDN*

*Power Delivery Network



Can pursue further scaling without the bottleneck due to power wiring

Source: TEL

Source of all drawings: TEL

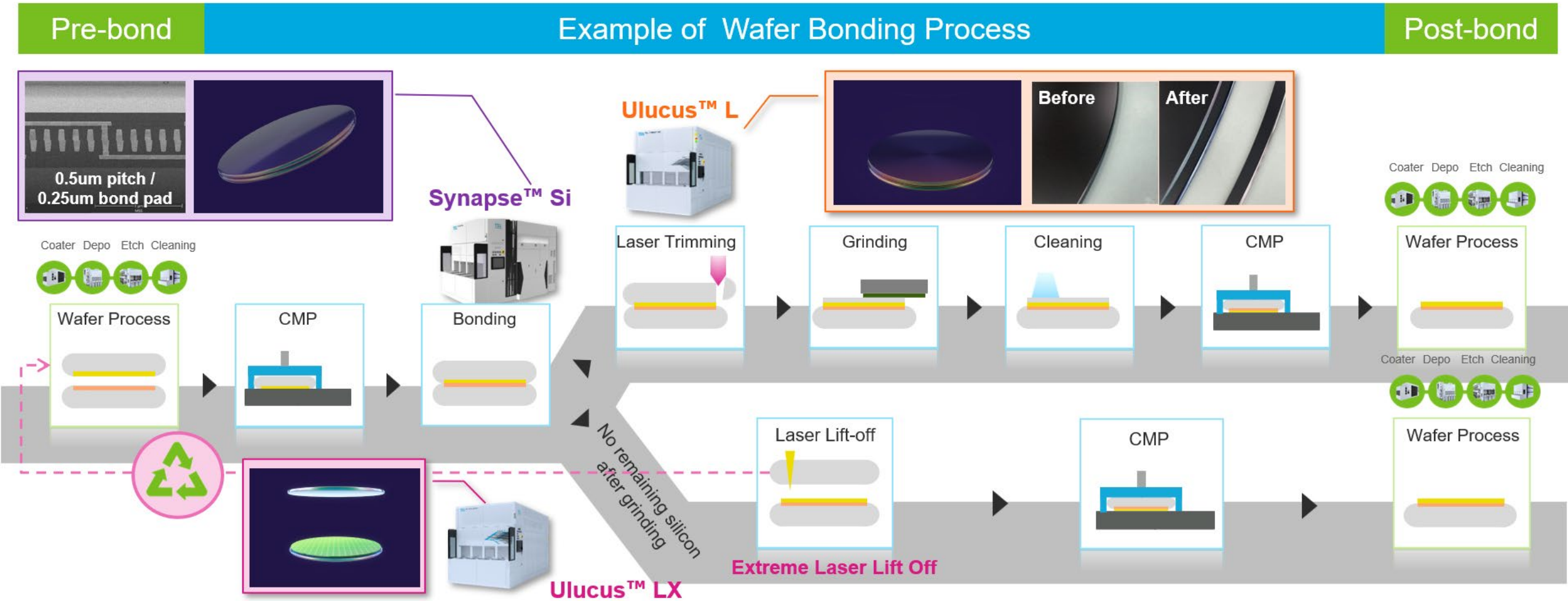
Broad Applications and Expansion of Bonding Technology

Application	Advanced Package		
	Stack Memory / HBM	3DIC	
Stacking Device	DRAM Wafer ⋮ DRAM Wafer + DRAM Wafer + Logic Wafer OR DRAM ( ) Die ⋮ DRAM ( ) Die + DRAM ( ) Die + Logic Wafer	SoC Disaggregation Device A Wafer + Device AorB Wafer OR A, B, C Die, Wafer	Heat Spreader Heat Spreader + Device
Bonding	Wafer to Wafer / Die to Wafer (CHB/Fusion)	Wafer to Wafer / Die to Wafer (CHB)	Wafer to Wafer (Fusion)
Structure	**Micro Bump** → ***Cu hybrid*** (More stacks) Change • Thinner die / more stacks • High density connection • Better thermal conductance Cu	**Monolithic SoC** → ***3D Stack IC*** SRAM, CPU/GPU, I/O & Peripheral Change • Small formfactor (3D stack vs. 2D) • Higher speed (shorter wiring, no bump) • Lower power (shorter wiring, no bump) • Lower cost (higher yields, easy to mix processes) • Shorter time to market (matured IP block reuse)	Heat Spreader • Better thermal conductance
Status	R&D	R&D ~ HVM	HVM

The opportunity for CHB/fusion bonding is growing to encompass advanced packaging

Source of all drawings: TEL

Frontend Wafer Bonding Process and TEL Products



Integrating various TEL equipment enables next generation wafer bonding processes that deliver high performance and process efficiency

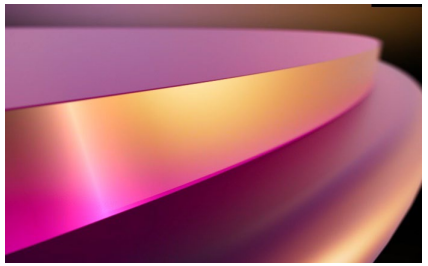
Laser Trimming System: Ulucus™ L

Source of all drawings: TEL

- Concept
  - Edge trimming of bonded wafer with laser
  - Latest platform utilizing super clean technology from frontend process, with the integration of laser control technology



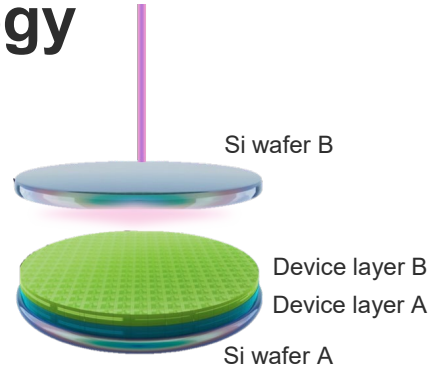
- Features
  - High accuracy: enabling narrower trimming width and smooth sidewall with less damage and good yield
  - High-productivity, high-reliability process
  - Environmentally-friendly process by reducing DIW usage by 70% or more



High-accuracy and high-quality laser trimming process - environmentally-friendly and innovative approach for wafer-level bonding

Introducing Ulucus™ LX for Post-Wafer Bonding Process

- **Extreme laser lift-off (XLO) technology**
  - Advanced thinning and critical technology for post-wafer bonding process
  - Unique laser technology enables separation of the Si-substrate from the device layer



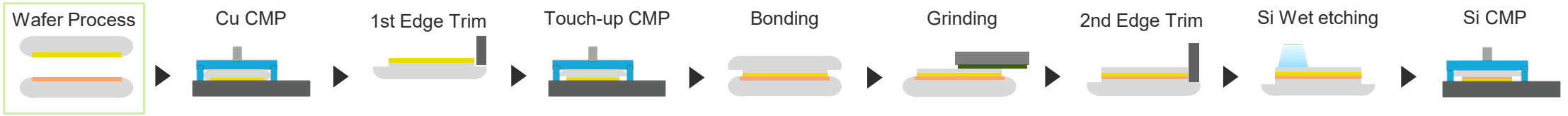
- **Advantages for process and environment**
  - Enhanced efficiency in silicon active areas
  - Fewer process steps required
  - Reduced need for DI water usage and CO_2 emission
  - Opportunity for wafer reuse



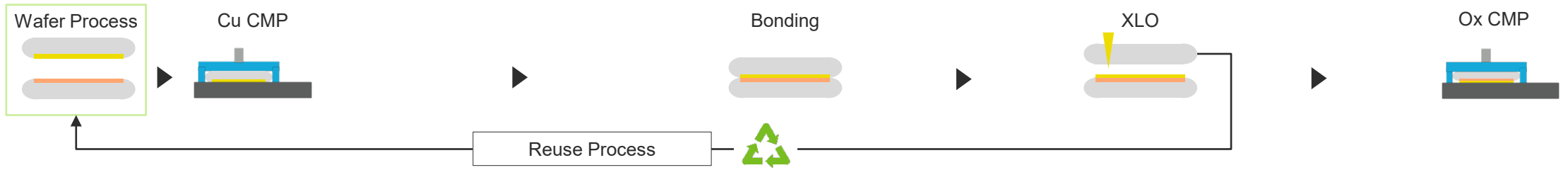
Source of all drawings: TEL

Ulucus™ LX Advantages

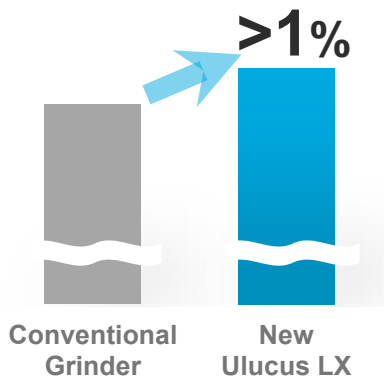
Permanent Bonding Process with Grinding & Blade Edge Trimming (Conventional)



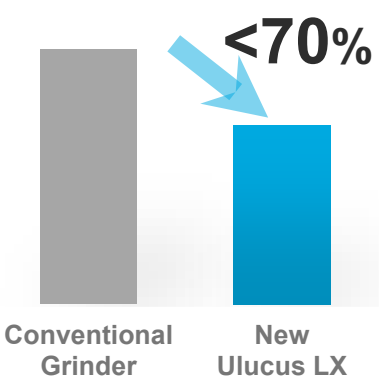
Permanent Bonding Process with XLO (Extreme Laser Lift Off)



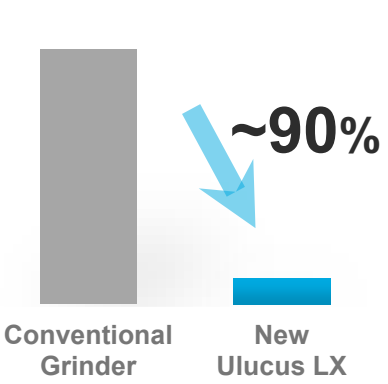
Active Silicon Area



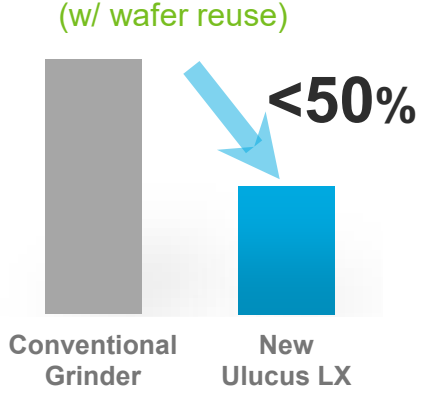
of Process Steps



DIW* Usage



CO_2 Emission
(w/ wafer reuse)



No Silicon Sludge
→ Advantage Over Grinder



Source: TEL

* DIW : De-ionized Water

8. MAGIC Market and Field Solutions Business Initiatives

MAGIC market

- Expected market growth of 2x
  (approximately $25B in 2023, projected $50B in 2030)
- Developing and supplying equipment for MAGIC
- Demo line ready for 200mm MAGIC
  - Yamanashi, Kumamoto, Miyagi
  - Massachusetts, Minnesota, Florida

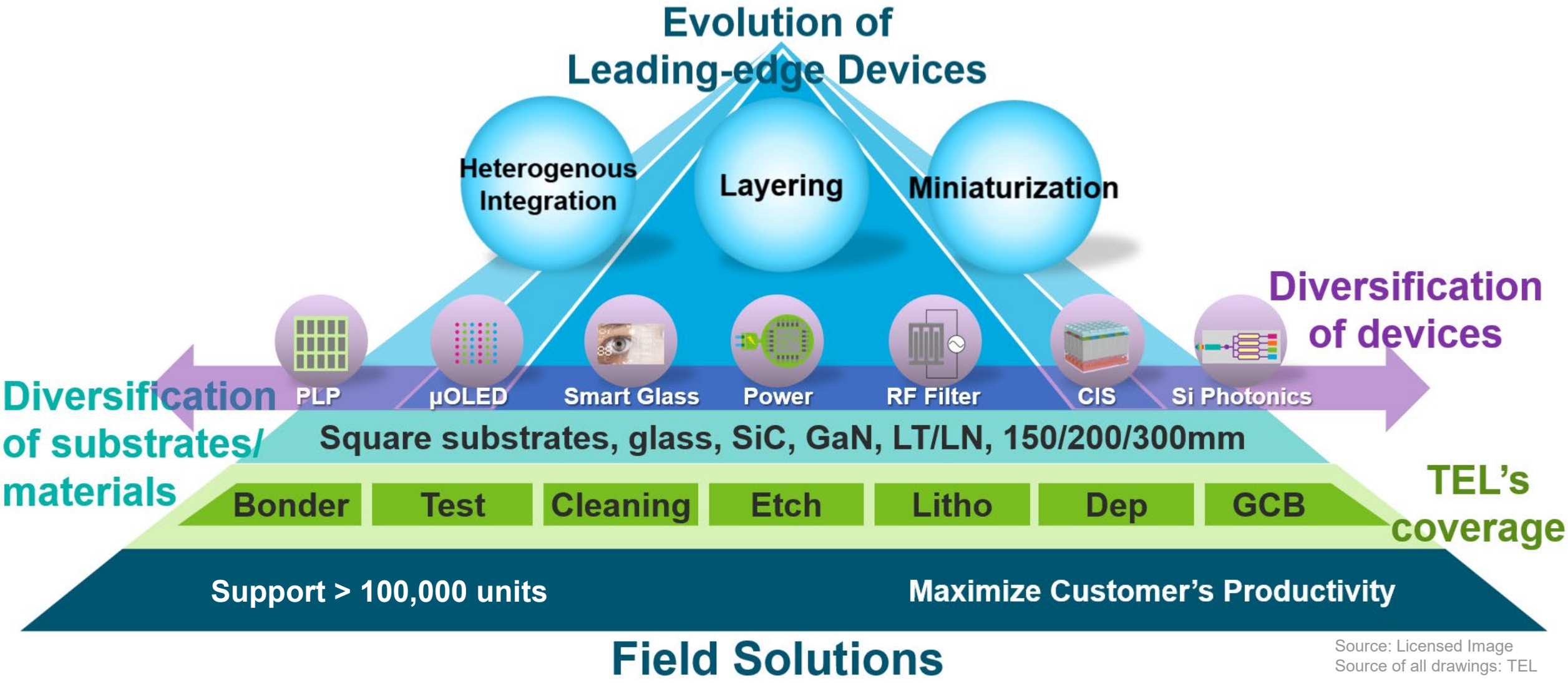






Source: TEL, Licensed Image

Providing Diverse Systems and Solutions for Diverse Needs



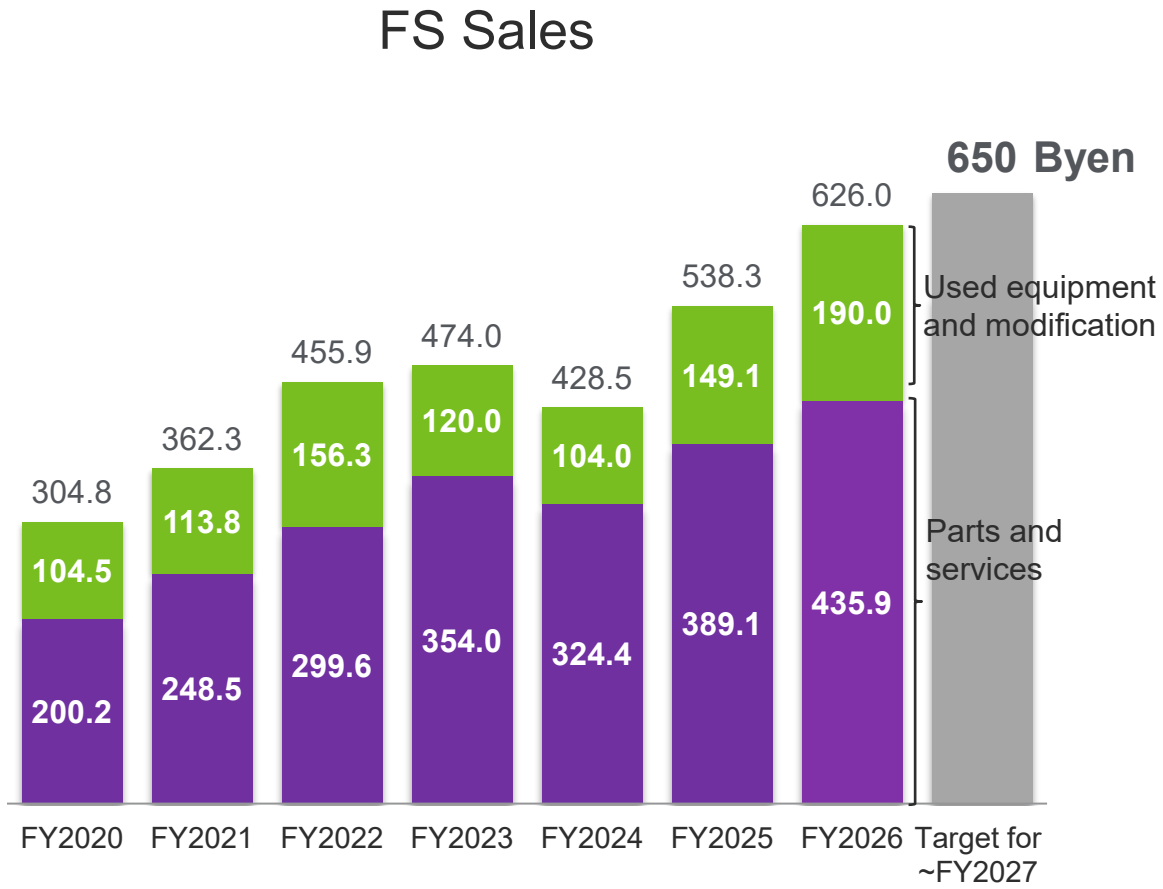
Source: Licensed Image
Source of all drawings: TEL

Basic Strategy for Field Solutions (FS)

- Deploying solution business based on installed base
- Development and promotion of advanced Field Solutions
  - Providing leading-edge and sustainable support that utilizes the latest technology, such as DX
  - Development of remote maintenance support and training tools
- Enhancing the front-lines engineers and capabilities
  - Continuous skill improvement for field engineers

Support customers to maximize their business operations through services with high added value

Field Solutions (FS) Sales Results and Business Contents



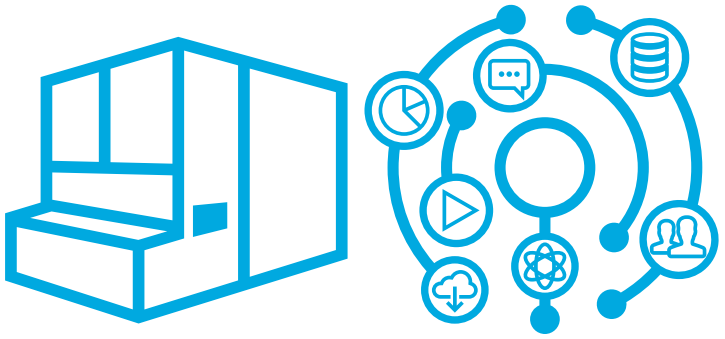
- Parts and repair
  - Predictive maintenance for parts deterioration
  - Appropriate parts inventory management and prompt delivery
- Services
  - Providing “comprehensive contract type” services that encompass everything from equipment delivery to after-care maintenance
  - Proposing solutions that address customer demands and maximizing equipment utilization rates
- Modification
  - Productivity improvement
  - Yield improvement

SAM is expanding with over 100,000* installed base currently and increasing by approx. 4,000 to 6,000 units each year

* As of March 2026

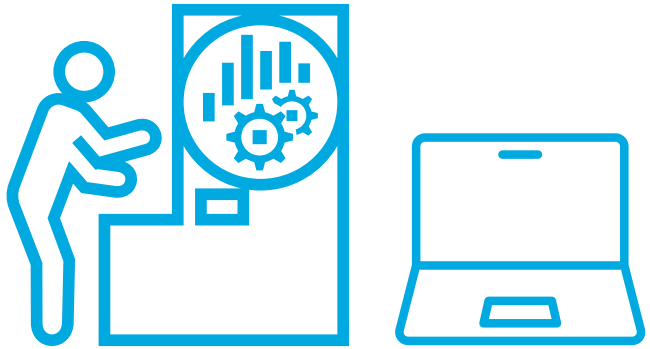
Advanced Field Solutions

TELeMetrics™



- Monitoring data on individual equipment
- Knowledge management and accumulation of problem case studies

Remote Support



- Minimization of downtime through predictive maintenance of equipment
- Remote support that enables prompt response even under travel restrictions

Proposing solutions with high added value
centered around “TELeMetrics™” that utilize DX

9. Digital Transformation (DX) Initiatives

Leveraging DX in each step of Product Lifecycle

Best Product Dev. | Start up / Process Ramp up | Production | Best Service Delivery



Source: TEL

MI* (Materials Informatics) | Self-diagnostics (Sensors) | Robotics

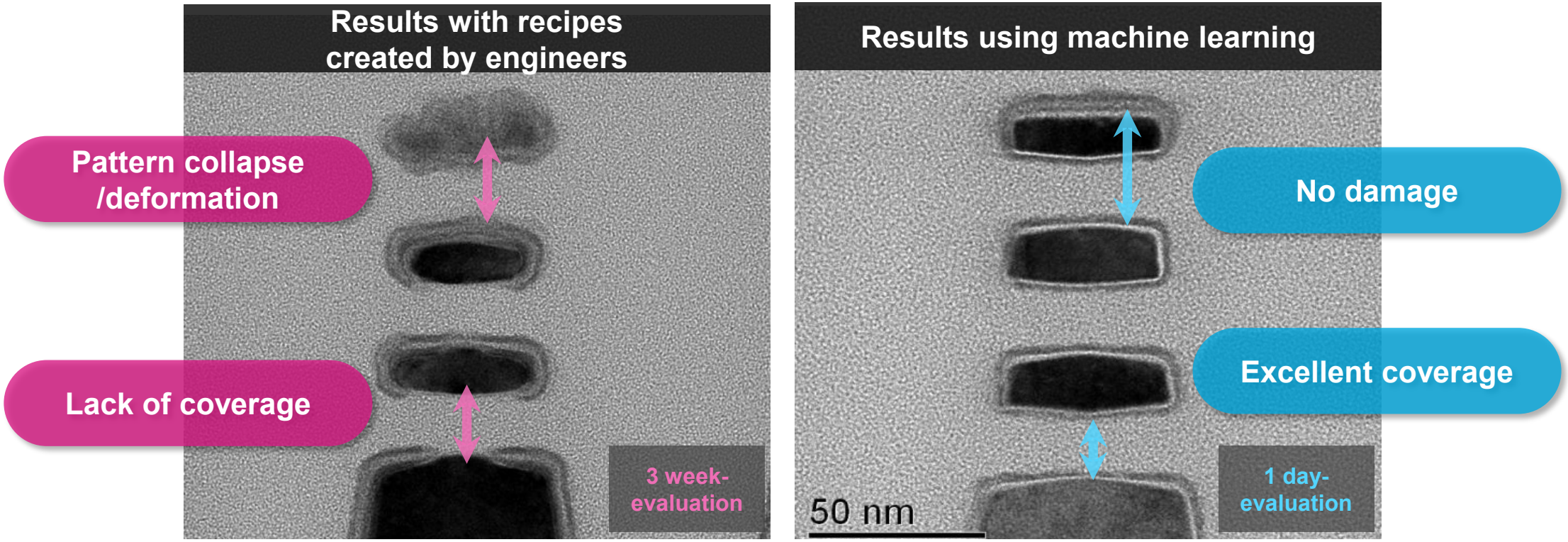
PI* (Process Informatics) | High Throughput Platform | AR/VR

Developing digital enablers for use throughout Product Lifecycle (PLC) to leverage productivity and profitability

*MI: a method that leverages material databases and AI to develop new material and to predict material properties effectively.
*PI: a method that uses data and machine learning from manufacturing and chemical processes to optimize operations, detect anomalies, and improve quality.

Example Activity 1: Increasing Productivity of R&D

Process Informatics



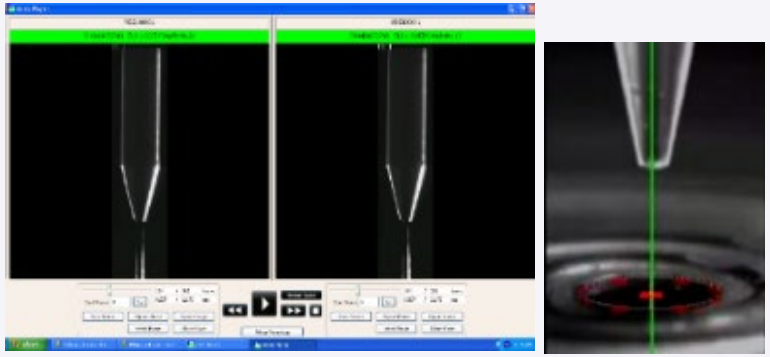
Source: Tokyo Electron Technology Solutions Limited / Tokyo Electron Limited

Achieved good step coverage with no pattern deformation in the ALD process by machine learning

Example Activity 2: Increasing Operation Cost of Equipment

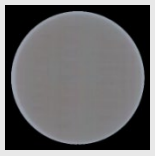
Reducing Chemicals of Coater/Developer

Monitoring of chemical discharge status
using image processing technology



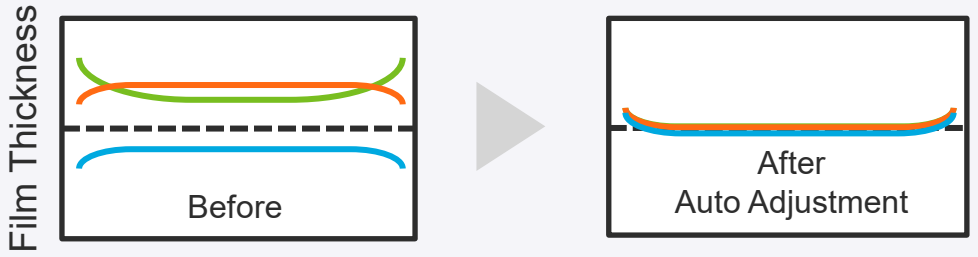
Source: TEL

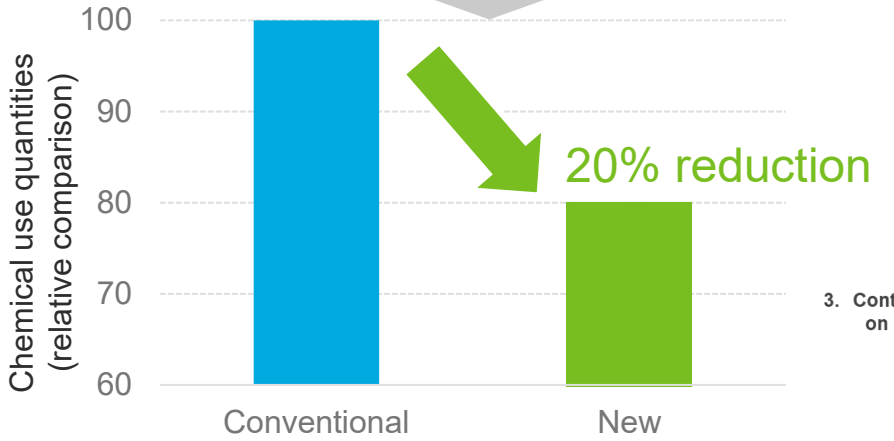
Monitoring of chemical coverage of interior of surfaces
using image processing technology

Dispense Volume	X ml	Y ml	Z ml	A ml
Judgement	Passed	Passed	Failed	Failed
Wafer image				

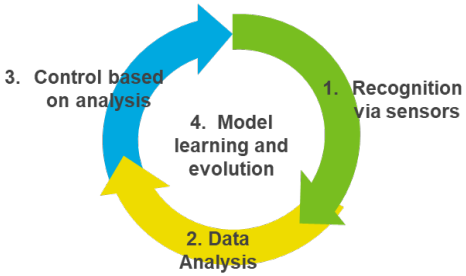
Source: TEL

Automatic film thickness adjustment function



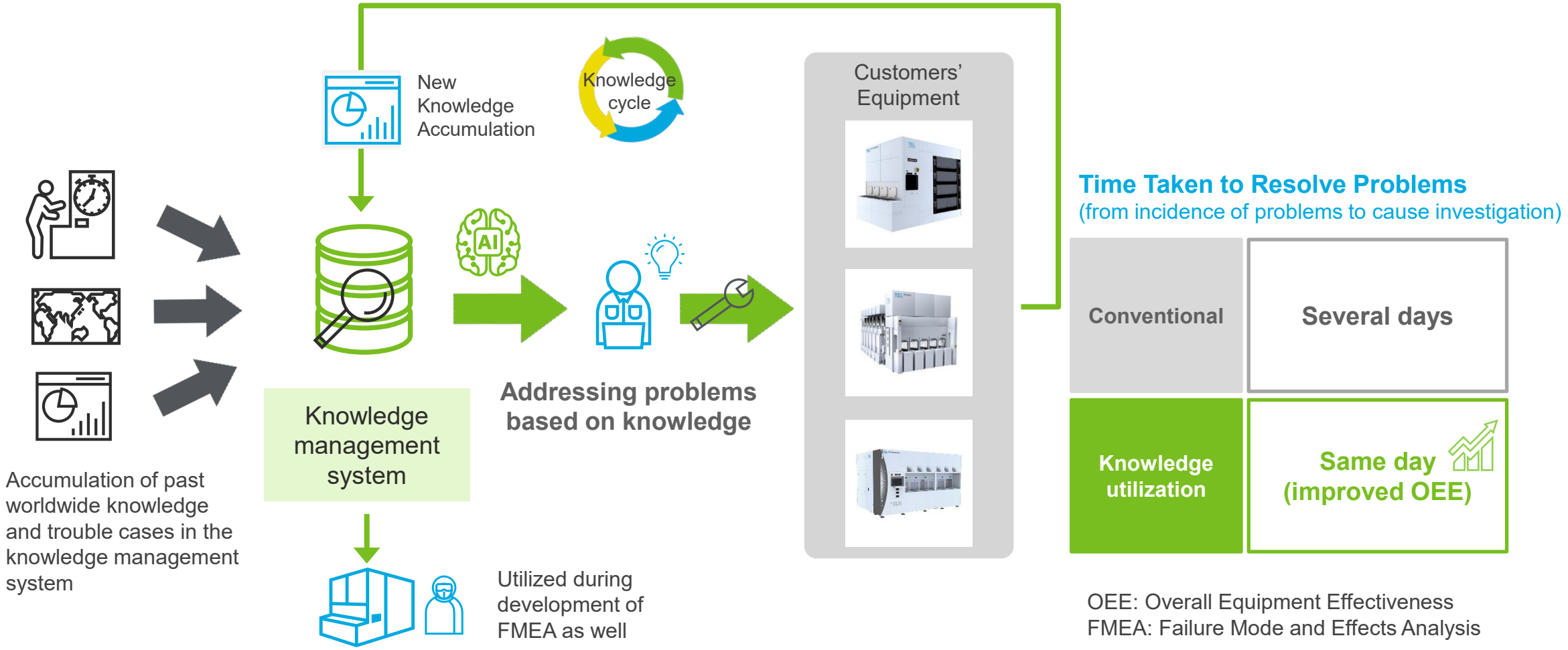






Contributed to customer operation costs
and the environment by using machine learning

Example Activity 3: Improving Overall Equipment Effectiveness



Time Taken to Resolve Problems
(from incidence of problems to cause investigation)

Conventional	Several days
Knowledge utilization	Same day (improved OEE)

OEE: Overall Equipment Effectiveness
FMEA: Failure Mode and Effects Analysis

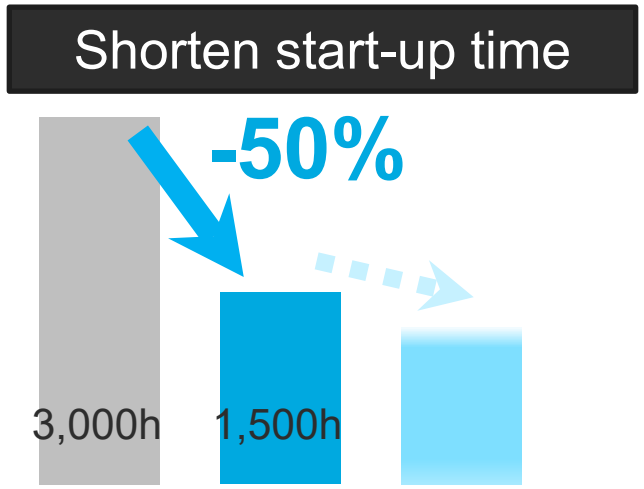
Using the Knowledge Management System to reduce the time taken to resolve problems and improve equipment operation rates

10. Procurement and Manufacturing Strategy

Continuous Production Innovation in Pursuit of Safety, High Quality and High Reliability

- Build a production system able to quickly respond to market changes
- Shorten time from new product development to mass production
- Shorten production lead times: Achieve 100% module shipment
- Utilize DX and automation in manufacturing, and expand automated warehouse
- **Significantly reduce equipment start-up time (One-touch start-up)**
  - Reduce start-up time up to 75% (primary target), One-touch (final target)





Conventional ➔ after production innovation

Expected outcome from shorten start-up time

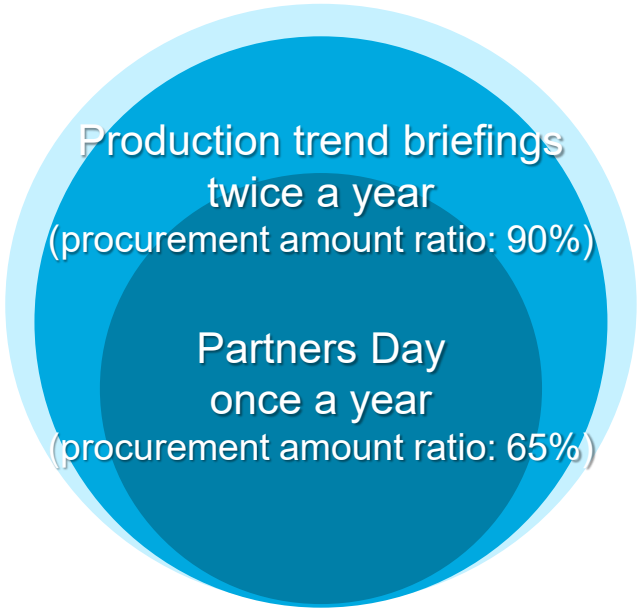
- Enhance productivity and start-up quality
- Reduce accident risks
- Optimize resources and the work-life balance

Build a Sustainable Supply Chain



Source: United Nations Information Centre（https://www.unic.or.jp/）

- Fair and transparent relationships and reliable trust relationship with our business partners
  - – Implement CSR/BCP assessments based on industry codes of conduct
  - – Share knowledge in such areas as safety, quality, the environment and compliance



E-COMPASS

Applaud environmental impact reduction activities, adding environmentally related items to assessment studies

- ✓ Reduce CO_2 emissions and the amount of energy usage
- ✓ Introduce renewable energy
- ✓ Promote resource conservation
- ✓ Promote waste reduction and recycling
- ✓ Promote activities for reducing the environmental impact of logistics



Procurement BCP and Proactive Procurement Activities

Mid- and long-term forecast
Promote “Shift Left” procurement strategy
Build BCP system resilient to procurement difficulty

Safety stock
Inventory liquidity

Oversee whole supply chain from upstream to downstream
Visualize and grasp risks

Visualize supply chain

Supply chain responsive to any kind of risks (Raw materials, parts, processing and assembly)
Strong and reliable supply chain

Risk management on business partners
Strengthen partnership

Measures for procurement BCP

Early procurement of parts

- Early procurement for long term
- Ensure inventory exchange flexibility among factories
- Inventory reductions in total

Secure semiconductor devices

- Secure semiconductor devices for our equipment
- Visualize and streamline distribution channel
- Collaborate with semiconductor makers

= TEL can be a customer of our customers

Parts and Suppliers

- Identify and analyze risk parts
- Multi sourcing of producing countries
- Standardization, centralization and decentralization of parts
- Measures to secure capacity for us

Smart Manufacturing to Achieve High Quality and Productivity

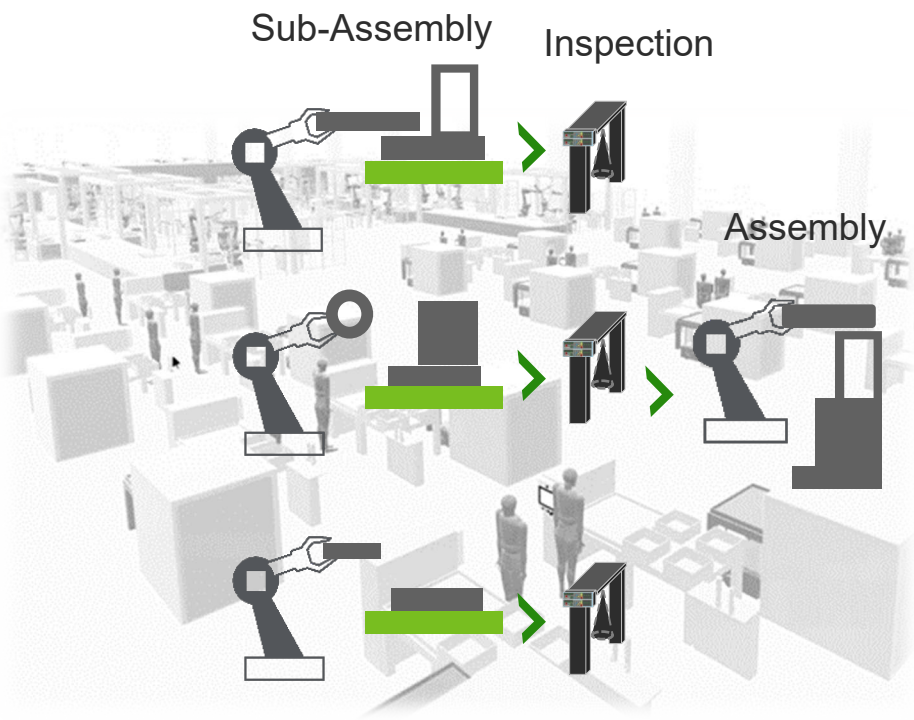
Development & Design



Feed Forward

Feedback

Smart Manufacturing



By centralizing development and production in TEL Miyagi,
we ensure continuous concurrent engineering and advanced manufacturing capabilities

Source: TEL

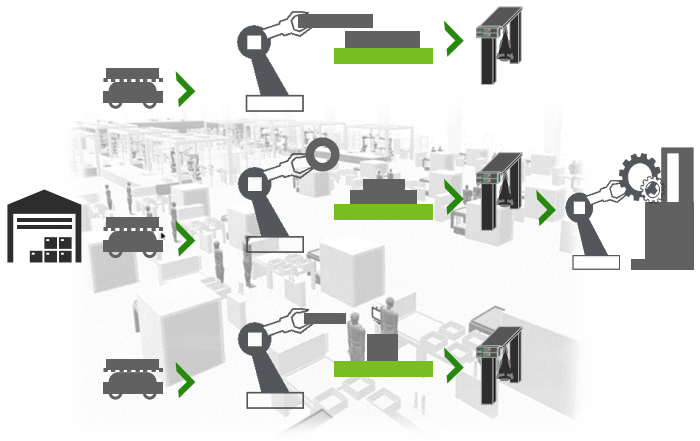
Vision for Smart Production

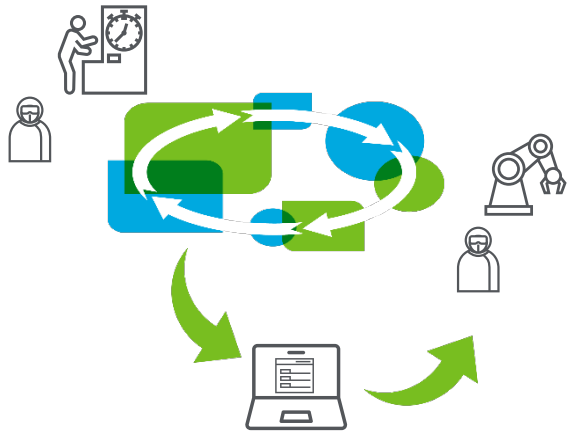
- Achieve sustainable manufacturing for the future

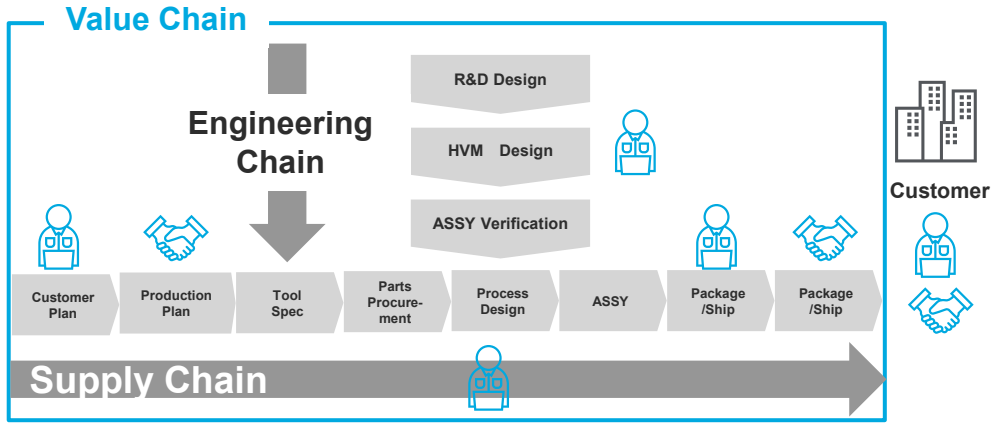
Overwhelming Efficiency
through automation and standardization

Enhancing Adaptability
to internal and external environmental changes

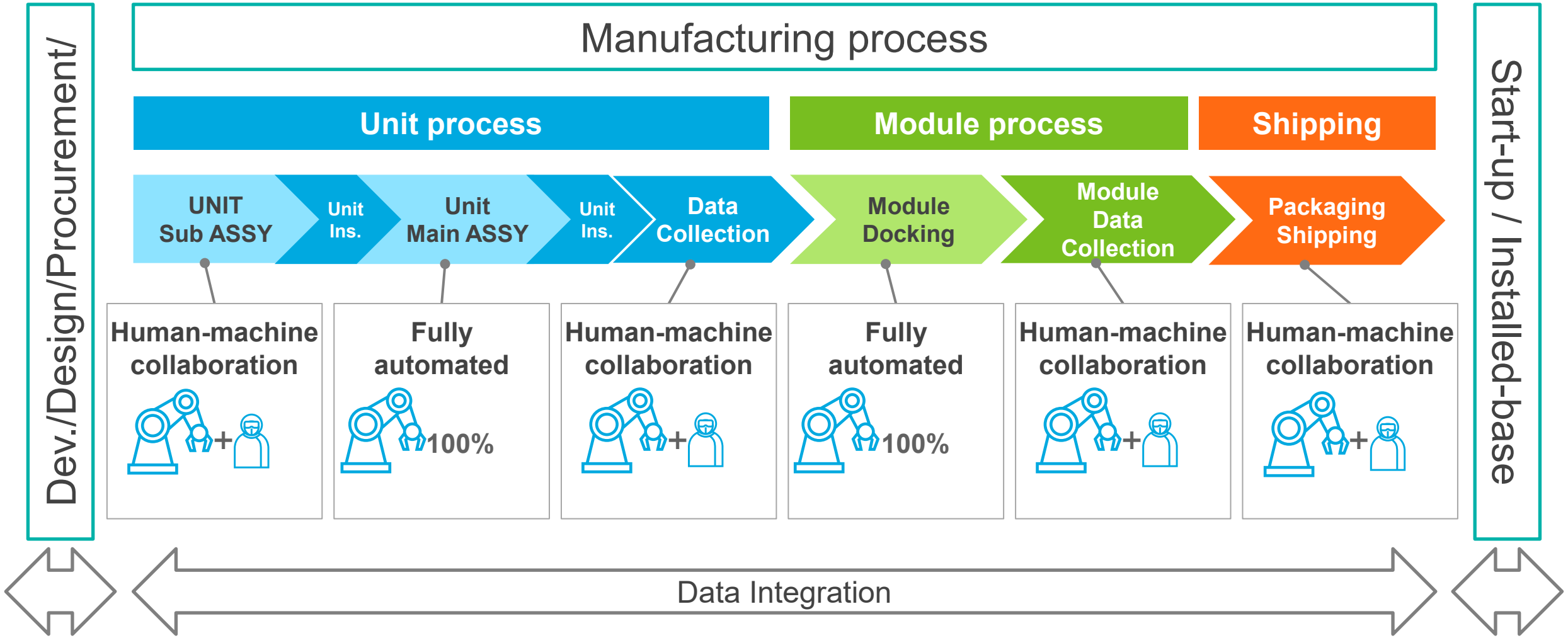
Product & Service Quality Improvement
through enhanced value chain







Concept of Smart Production



Appendix: Data Section

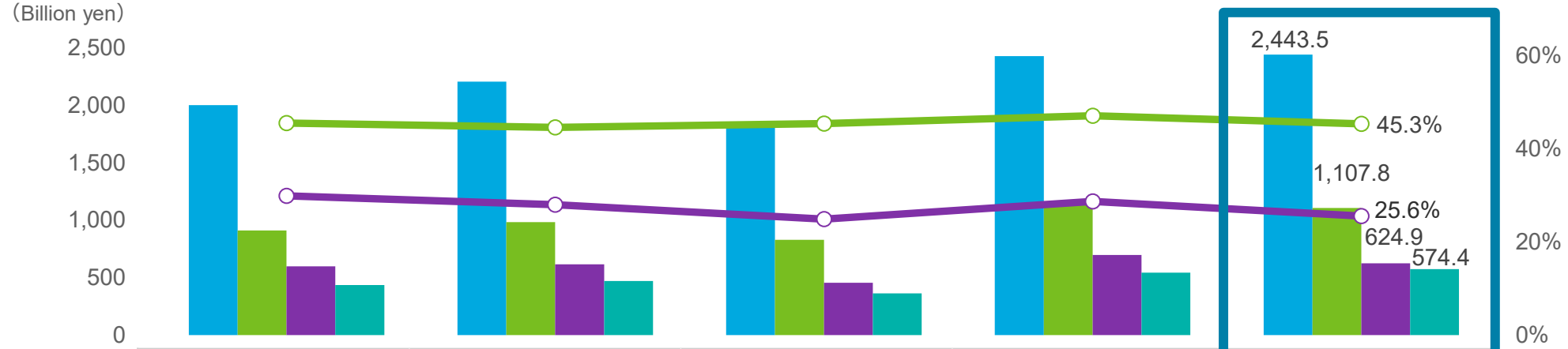
Financial Summary

(Billion yen)

	FY2025	FY2026	FY2026 vs FY2025	Reference: FY2026 estimates announced on February 6, 2026
Net sales	2,431.5	2,443.5	+0.5%	2,410.0
Gross profit	1,146.2	1,107.8	-3.4%	1,092.0
Gross profit margin	47.1%	45.3%	-1.8pts	45.3%
SG&A expenses	448.9	482.9	+7.6%	499.0
Operating income	697.3	624.9	-10.4%	593.0
Operating margin	28.7%	25.6%	-3.1pts	24.6%
Income before income taxes	706.1	748.1	+6.0%	714.0
Net income attributable to owners of parent	544.1	574.4	+5.6%	550.0
EPS (Yen)	1,182.40	1,254.57	+6.1%	1,200.05
R&D expenses	250.0	277.8	+11.1%	290.0
Capital expenditures	162.1	216.0	+33.2%	240.0
Depreciation and amortization	62.1	80.9	+30.3%	86.0

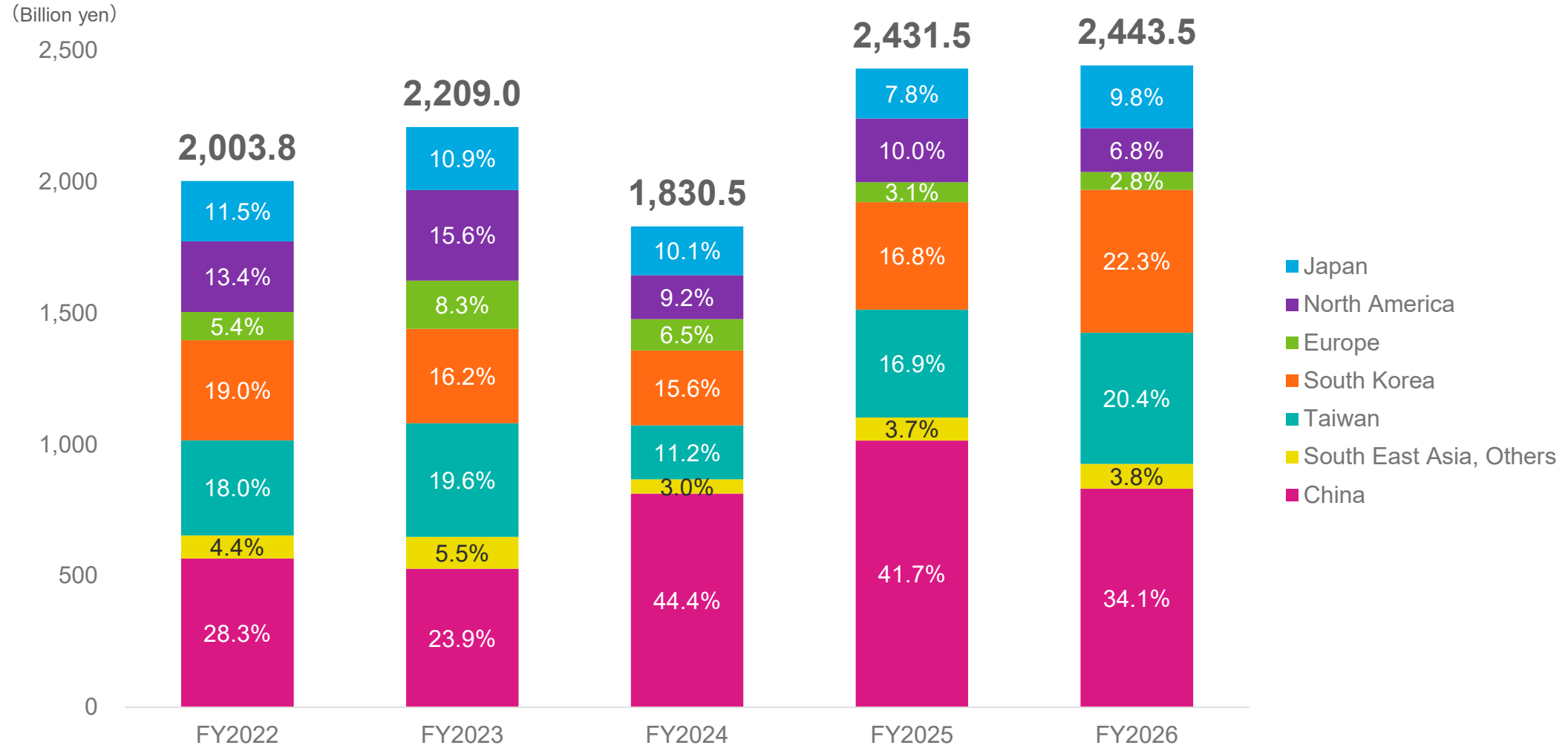
1. In principle, export sales of Tokyo Electron's products are denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of foreign exchange rate fluctuations on profits is negligible, unless extreme fluctuations occur.
2. Profit ratios are calculated using full amounts, before rounding.

Financial Trend



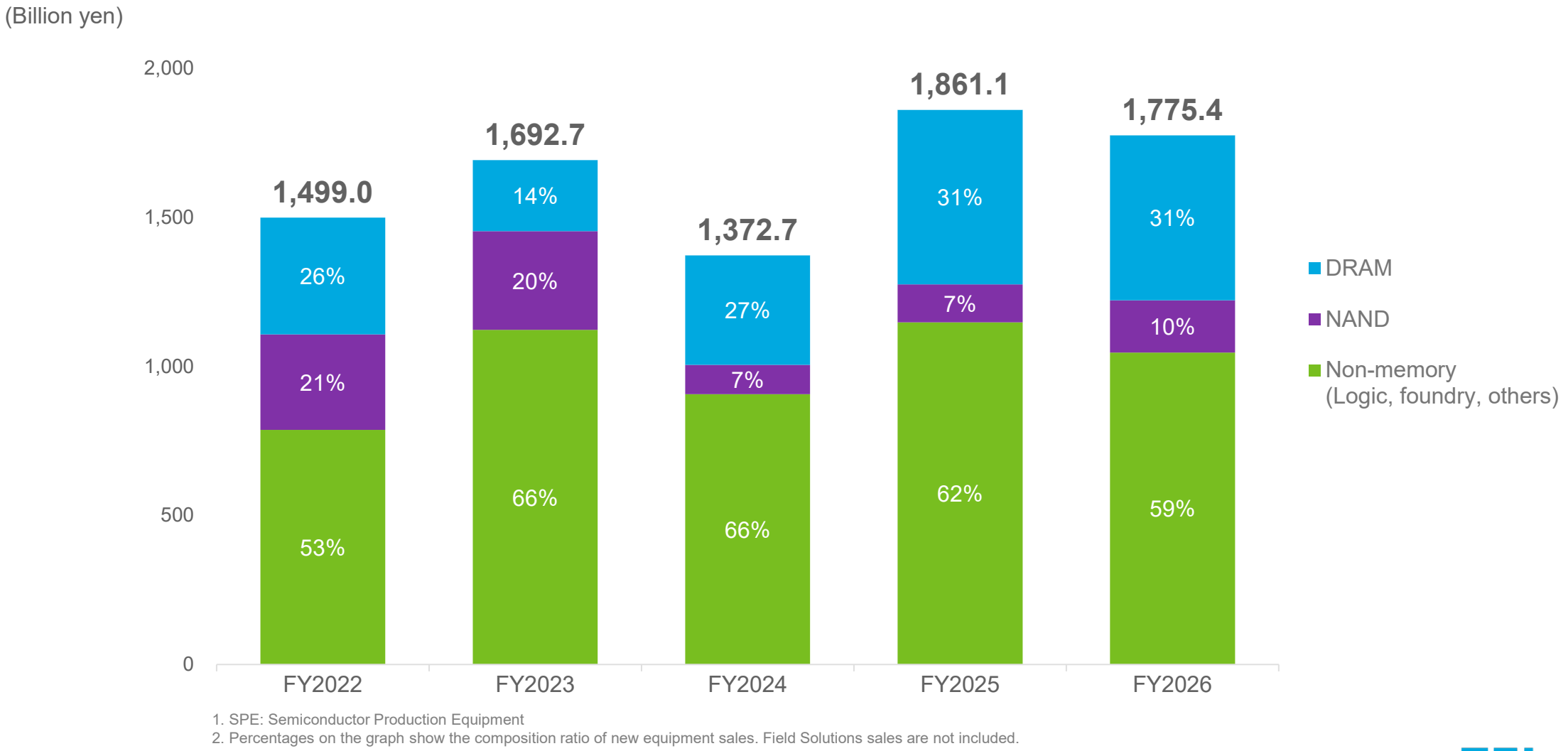
	FY2022	FY2023	FY2024	FY2025	FY2026
Net sales	2,003.8	2,209.0	1,830.5	2,431.5	**2,443.5**
Gross profit	911.8	984.4	830.2	1,146.2	**1,107.8**
Operating profit	599.2	617.7	456.2	697.3	**624.9**
Net income attributable to owners of parent	437.0	471.5	363.9	544.1	**574.4**
Gross profit margin	45.5%	44.6%	45.4%	47.1%	**45.3%**
Operating margin	29.9%	28.0%	24.9%	28.7%	**25.6%**
ROE	37.2%	32.3%	21.8%	30.3%	**29.6%**

Sales by Region



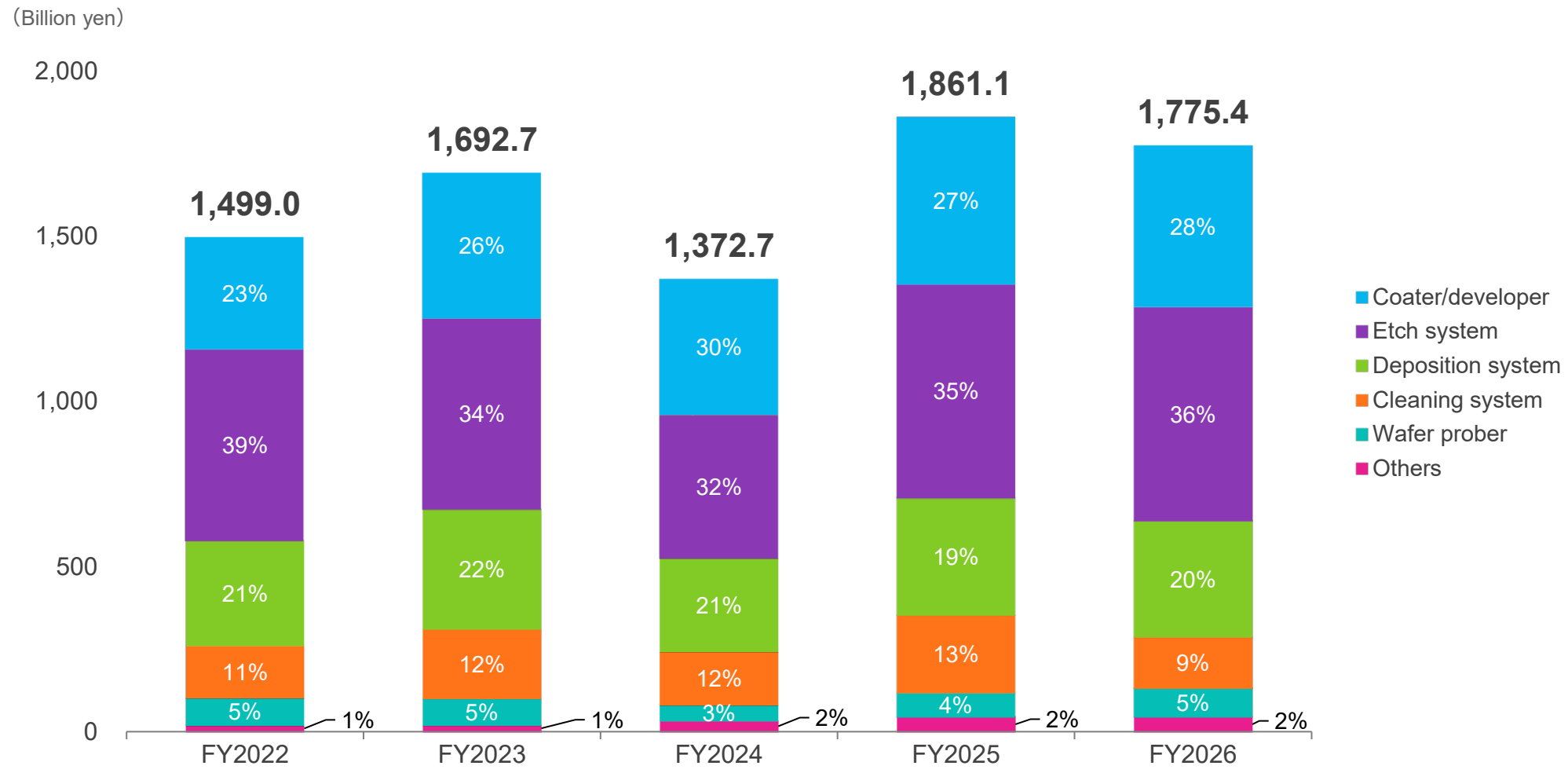
1. SPE: Semiconductor Production Equipment
2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

SPE New Equipment Sales by Application



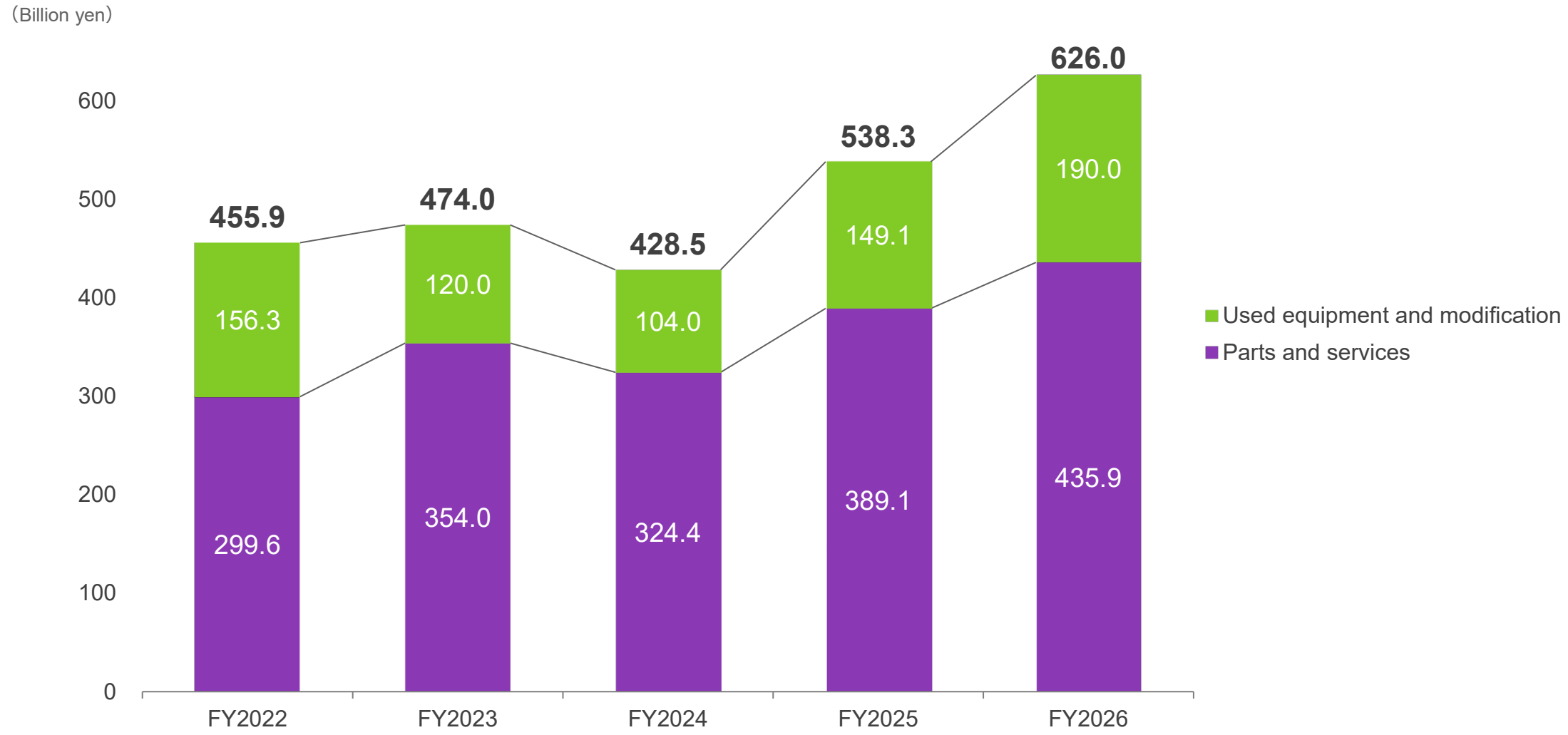
1. SPE: Semiconductor Production Equipment
2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

SPE New Equipment Sales by Product



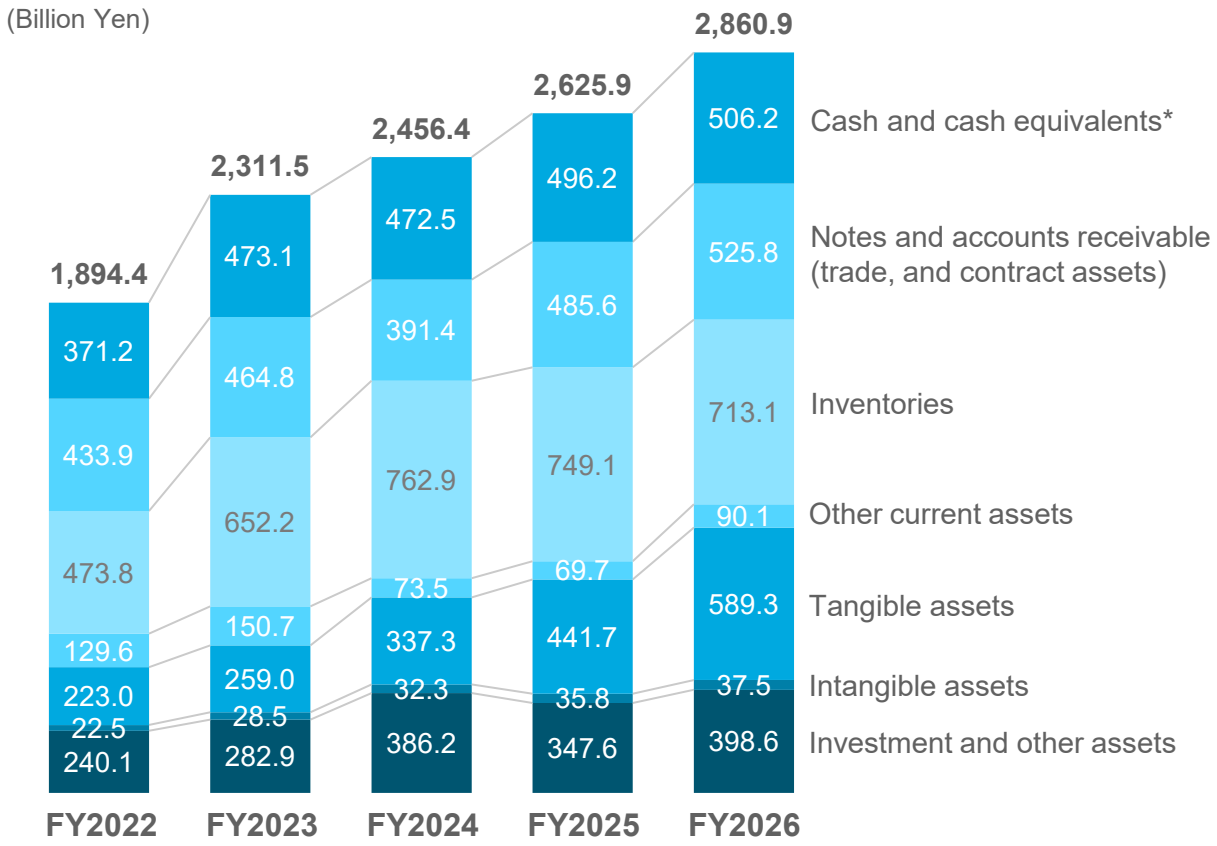
1. SPE: Semiconductor Production Equipment
2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

Field Solutions Sales

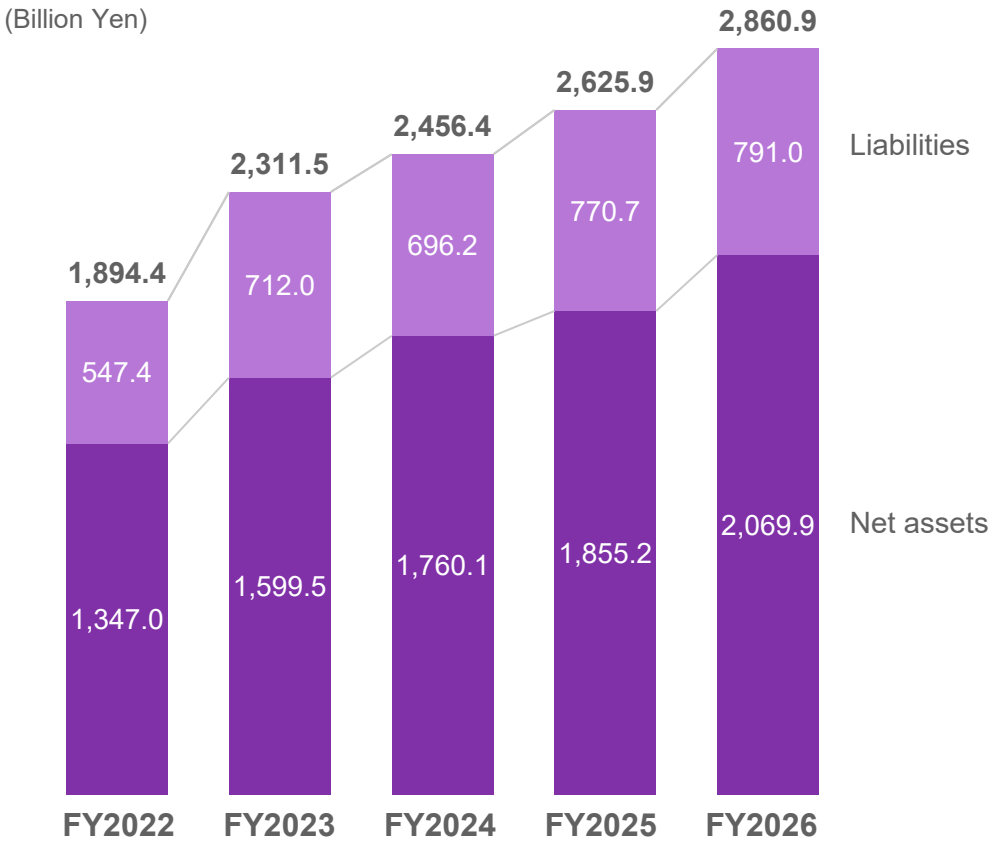


Balance Sheet

Assets

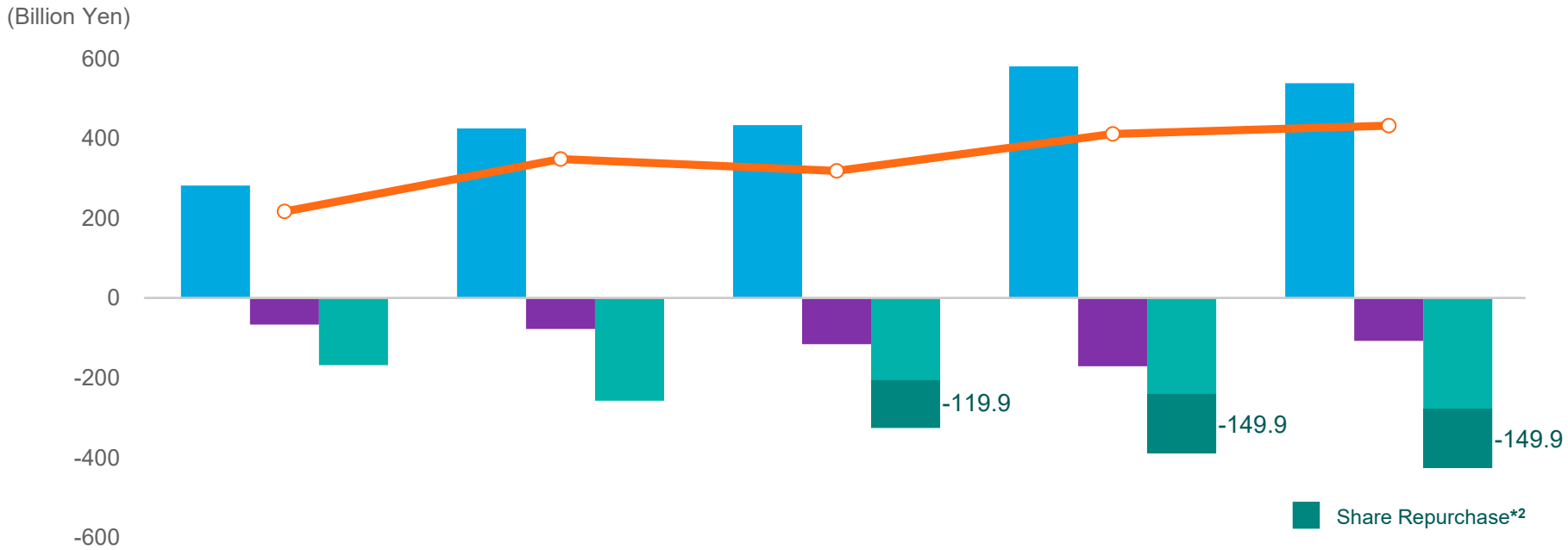


Liabilities and Net Assets



*Cash and cash equivalents: “Cash and deposits” + “Short-term investments”, etc. (“Securities” in Balance Sheet).

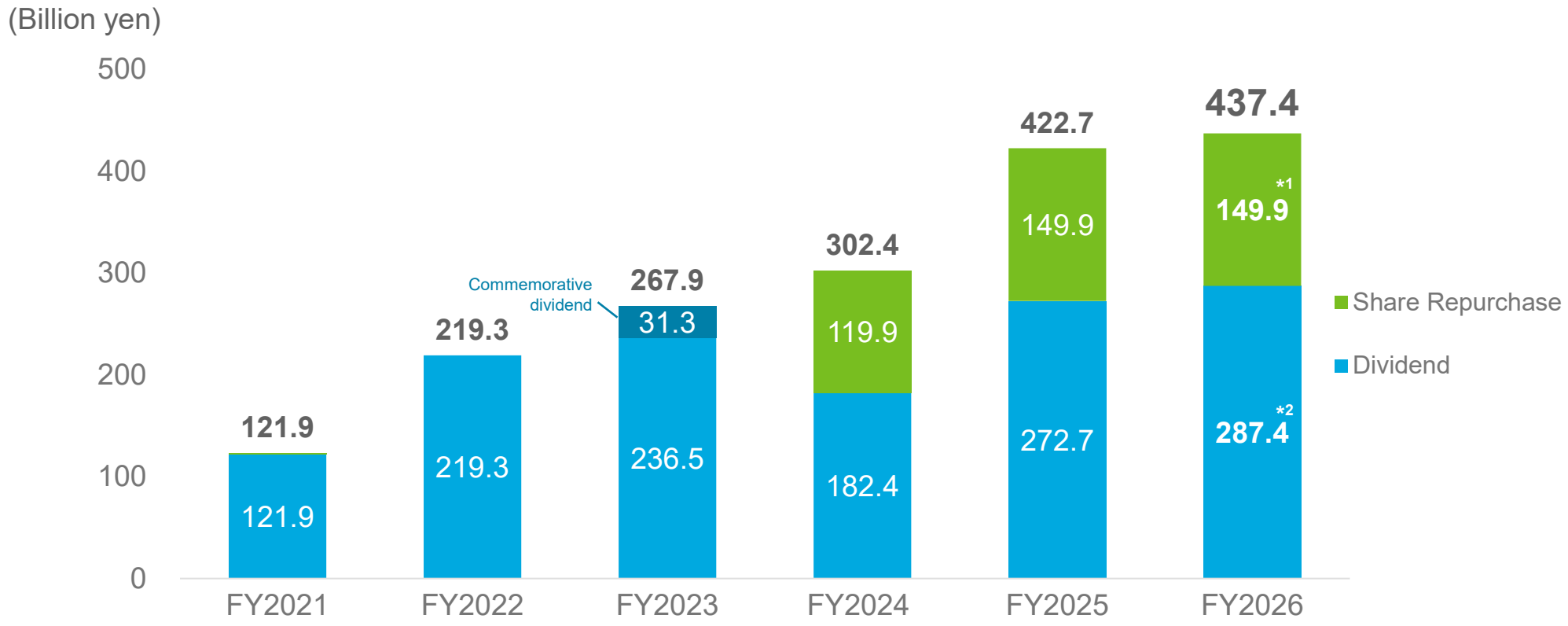
Cash Flow



	FY2022	FY2023	FY2024	FY2025	FY2026
Cash flow from operating activities	283.3	426.2	434.7	582.1	539.7
Cash flow from investing activities*1	-65.6	-76.7	-115.0	-169.7	-106.4
Cash flow from financing activities	-167.2	-256.5	-325.0	-388.8	-425.3
Free cash flow*3	217.7	349.4	319.6	412.4	433.2
Cash on hand*4	371.2	473.1	472.5	496.2	506.2

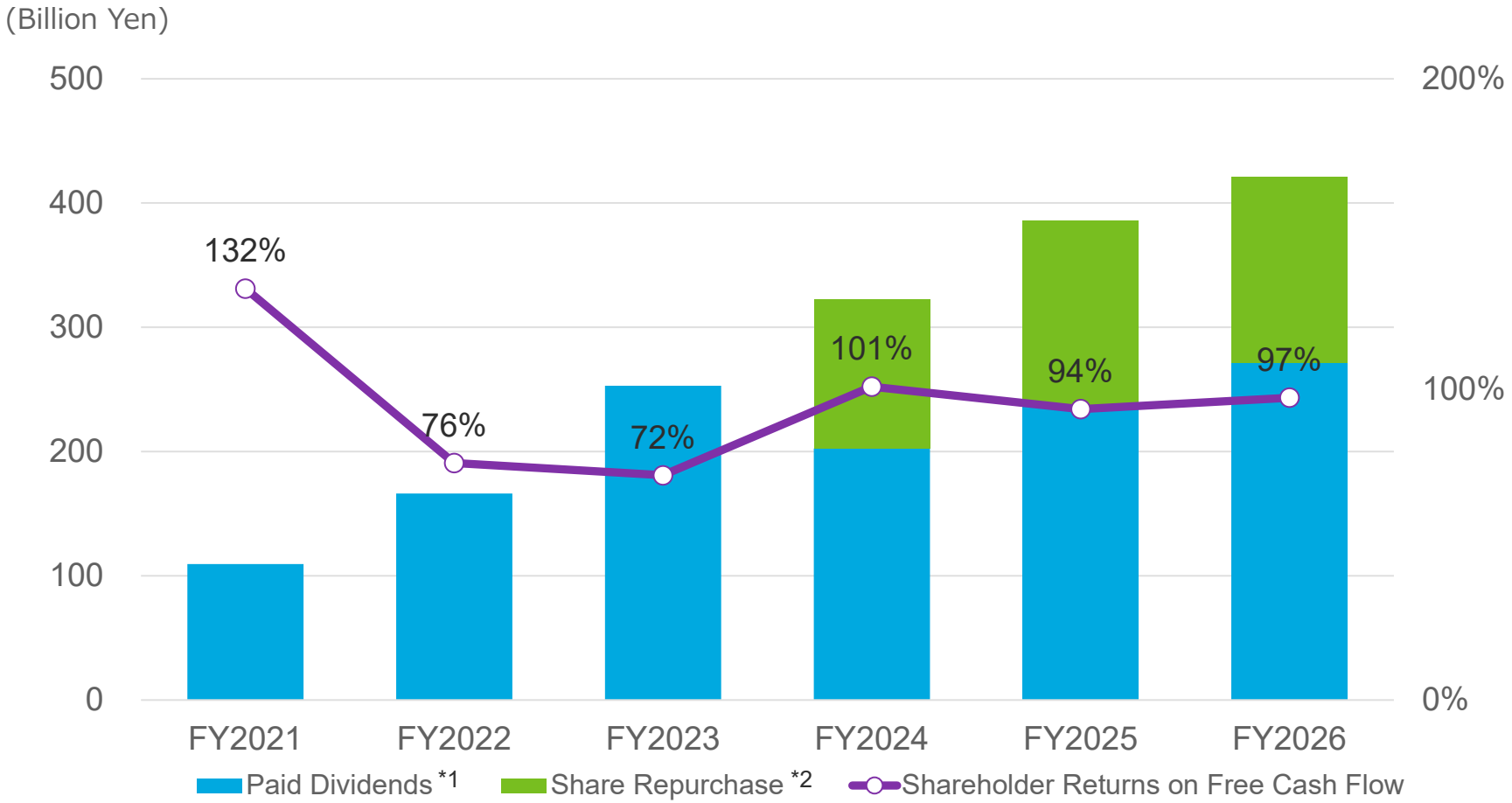
*1 Cash flow from investing activities excludes changes in time deposits and short-term investments.
*2 The amount for share repurchase excludes the cost incurred to purchase odd-lot shares.
*3 Free cash flow = “Cash flow from operating activities” + “Cash flow from investing activities” (excluding changes in “Time deposits” and “Short-term investments”).
*4 Cash on hand includes “Cash and cash equivalents” + “Time deposits and short-term investments” with original maturities of more than three months.

Total Return Amount



*1 https://www.tel.com/news/ir/2026/kn008f00000000ho-att/20260327_002_e.pdf
*2 The year-end dividend for FY2026 is provisional and pending approval by the Board of Directors.

Shareholder Returns Trend



*1 Paid dividends are shown based on their payment date.

*2 The amount for share repurchase excludes the cost incurred to purchase odd-lot shares.

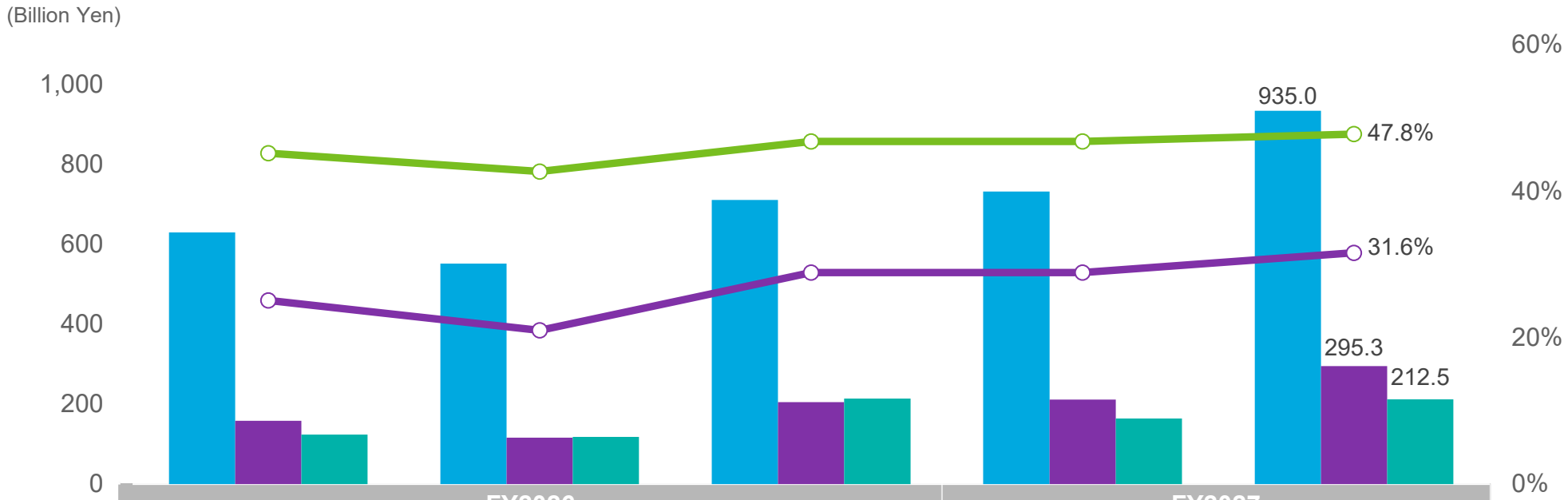
Financial Summary (Quarterly)

(Billion yen)

	FY2026			FY2027		vs. Q1 FY2027	vs. Q2 FY2026
	Q2	Q3	Q4	Q1	Q2		
Net sales	630.0	552.0	711.8	732.3	**935.0**	+27.7%	+48.4%
Gross profit	284.8	235.8	333.1	342.7	**447.3**	+30.5%	+57.0%
Gross profit margin	45.2%	42.7%	46.8%	46.8%	**47.8%**	+1.0pts	+2.6pts
SG&A expenses	126.4	119.6	127.5	131.3	**152.0**	+15.8%	+20.2%
Operating income	158.4	116.1	205.6	211.4	**295.3**	+39.7%	+86.4%
Operating margin	25.1%	21.0%	28.9%	28.9%	**31.6%**	+2.7pts	+6.5pts
Income before income taxes	161.0	153.3	281.8	215.4	**292.2**	+35.6%	+81.5%
Net income attributable to owners of parent	123.8	118.5	214.2	164.3	**212.5**	+29.4%	+71.7%
R&D expenses	72.6	66.2	76.7	72.0	**85.2**	+18.4%	+17.3%
Capital expenditures	91.2	30.3	41.6	39.9	**32.3**	-18.9%	-64.5%
Depreciation and amortization	19.1	21.1	23.5	22.5	**24.3**	+8.3%	+27.5%

1. Profit ratios are calculated using full amounts, before rounding.
2. FY202x refers to the financial year ending in March 202x.

Financial Performance (Quarterly)



	FY2026			FY2027	
	Q2	Q3	Q4	Q1	Q2
Net sales	630.0	552.0	711.8	732.3	935.0
Operating income	158.4	116.1	205.6	211.4	295.3
Net income attributable to owners of parent	123.8	118.5	214.2	164.3	212.5
Gross profit margin	45.2%	42.7%	46.8%	46.8%	47.8%
Operating profit margin	25.1%	21.0%	28.9%	28.9%	31.6%

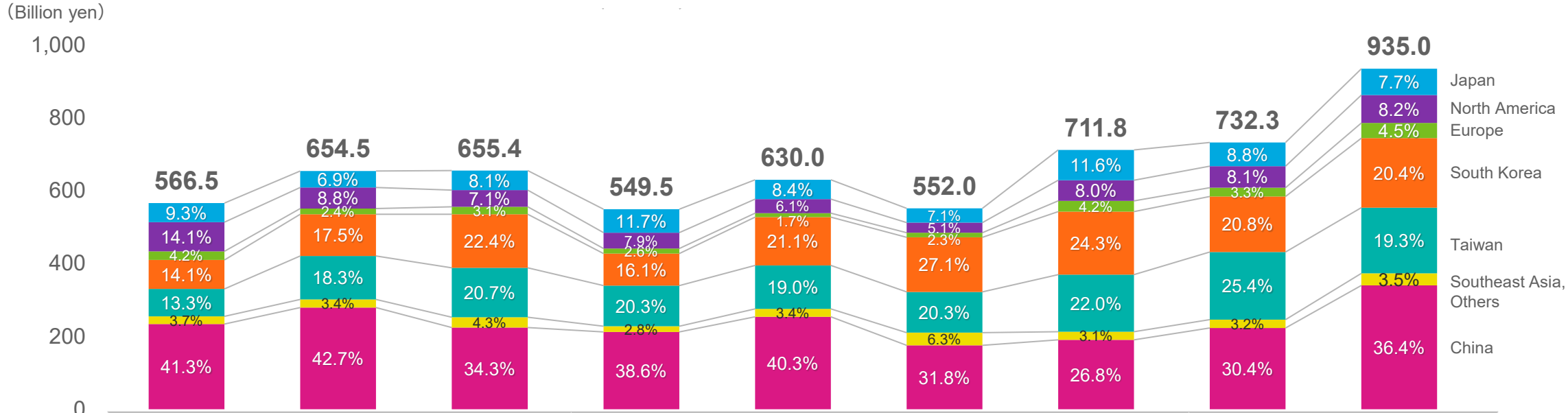
Financial Summary (Semiannual)

(Billion yen)

	FY2026		FY2027	vs. H2 FY2026	vs. H1 FY2026	H1 FY2027 Estimate (As of July 30)
	H1	H2	H1			
Net sales	1,179.6	1,263.8	**1,667.4**	+31.9%	+41.3%	1,620.0
Gross profit	538.8	569.0	**790.1**	+38.9%	+46.6%	748.0
Gross profit margin	45.7%	45.0%	**47.4%**	+2.4pts	+1.7pts	46.2%
SG&A expenses	235.7	247.2	**283.3**	+14.6%	+20.2%	290.0
Operating income	303.1	321.7	**506.7**	+57.5%	+67.2%	458.0
Operating margin	25.7%	25.5%	**30.4%**	+4.9pts	+4.7pts	28.3%
Income before income taxes	312.9	435.1	**507.7**	+16.7%	+62.2%	464.0
Net income attributable to owners of parent	241.6	332.8	**376.9**	+13.3%	+56.0%	349.0
R&D expenses	134.8	143.0	**157.3**	+10.0%	+16.7%	160.0
Capital expenditures	144.0	71.9	**72.3**	+0.5%	-49.8%	-
Depreciation and amortization	36.2	44.7	**46.8**	+4.9%	+29.2%	-

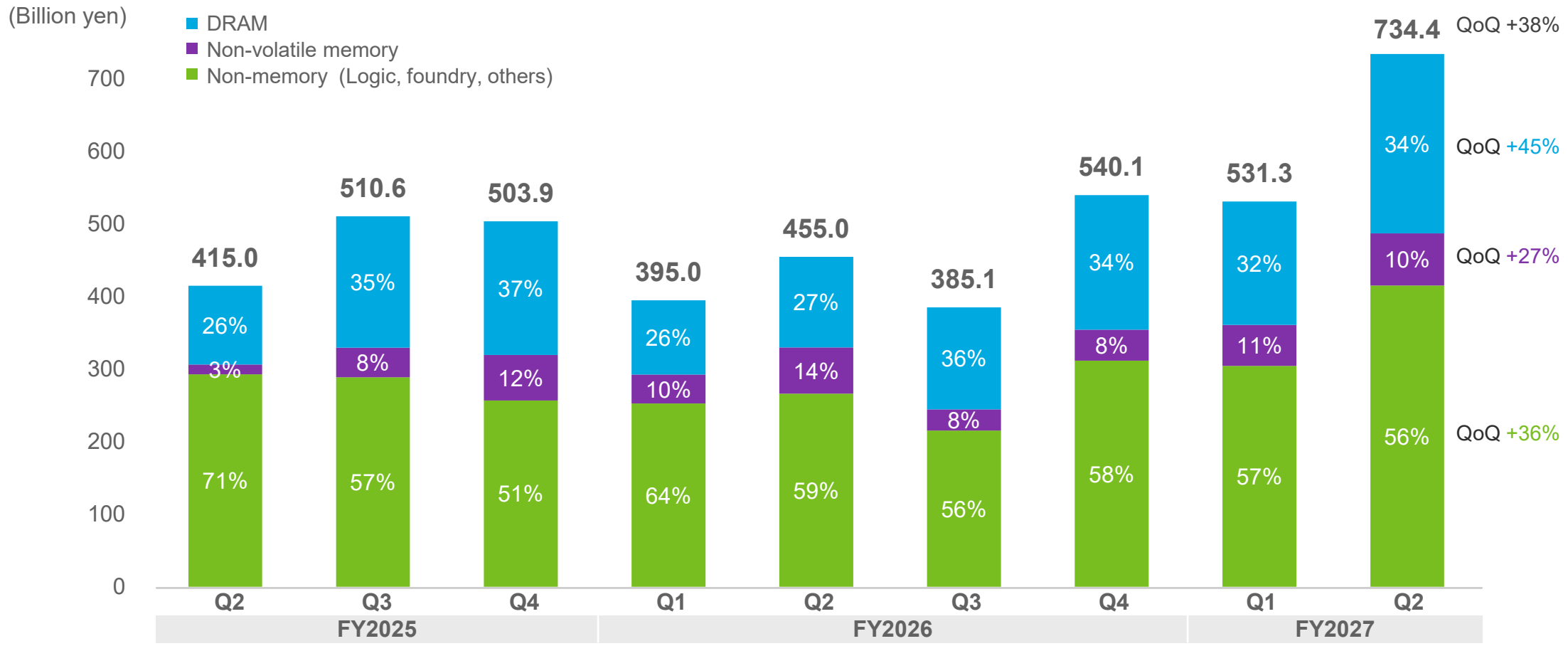
1. Profit ratios are calculated using full amounts, before rounding.

Composition of Net Sales by Region (Quarterly)



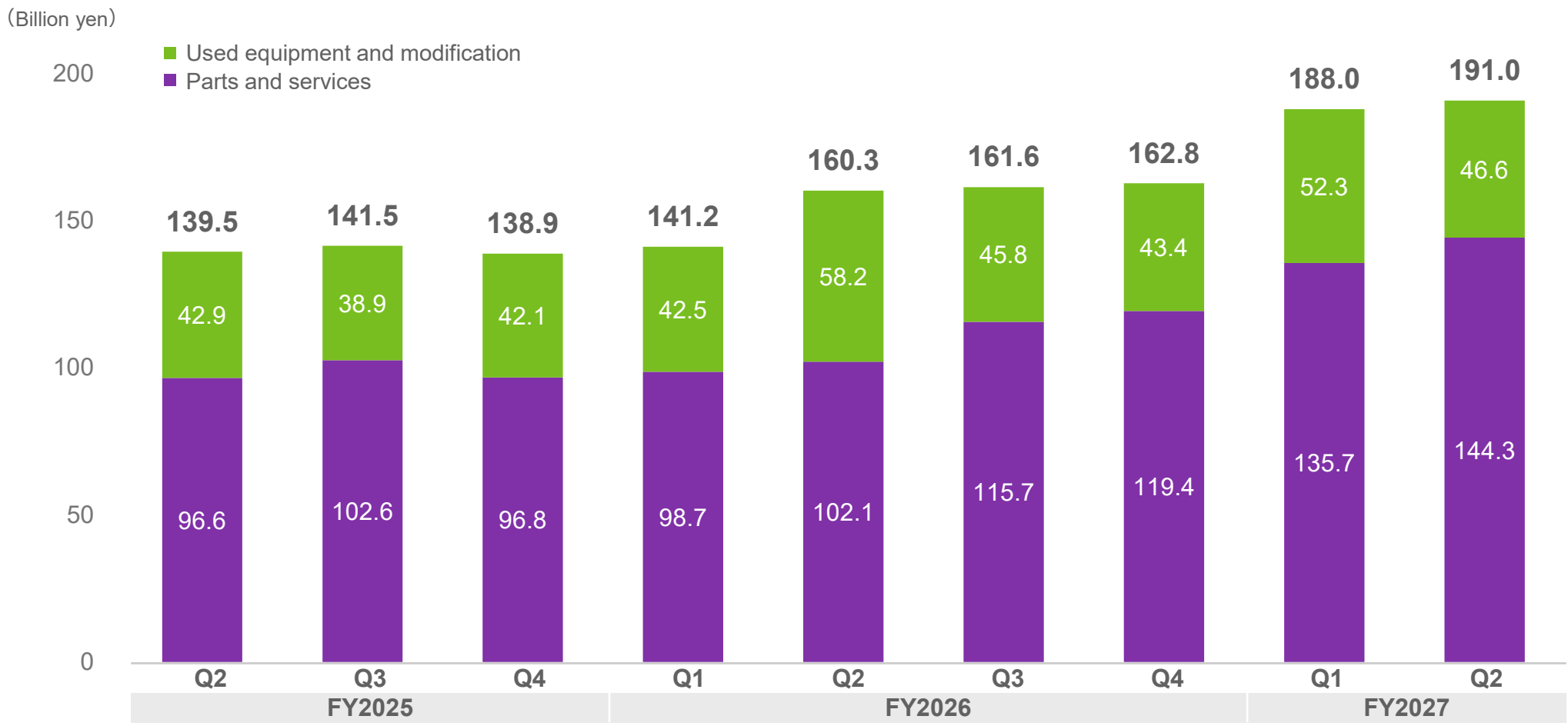
	FY2025			FY2026				FY2027	
	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
Japan	52.6	45.3	53.4	64.3	52.9	39.3	82.8	64.6	**72.2**
North America	79.9	57.7	46.2	43.4	38.4	27.8	56.7	59.0	**76.6**
Europe	23.8	15.7	20.3	14.0	10.8	12.7	29.7	24.2	**41.7**
South Korea	79.5	114.5	147.0	88.3	132.5	149.7	173.1	152.4	**190.7**
Taiwan	75.3	119.3	135.8	111.5	119.7	111.9	156.5	186.1	**180.4**
Southeast Asia, Others	21.2	22.3	27.8	15.6	21.3	34.8	22.1	22.9	**33.2**
China	233.9	279.4	224.6	212.1	254.1	175.5	190.7	222.9	**339.9**

SPE New Equipment Sales by Application (Quarterly)



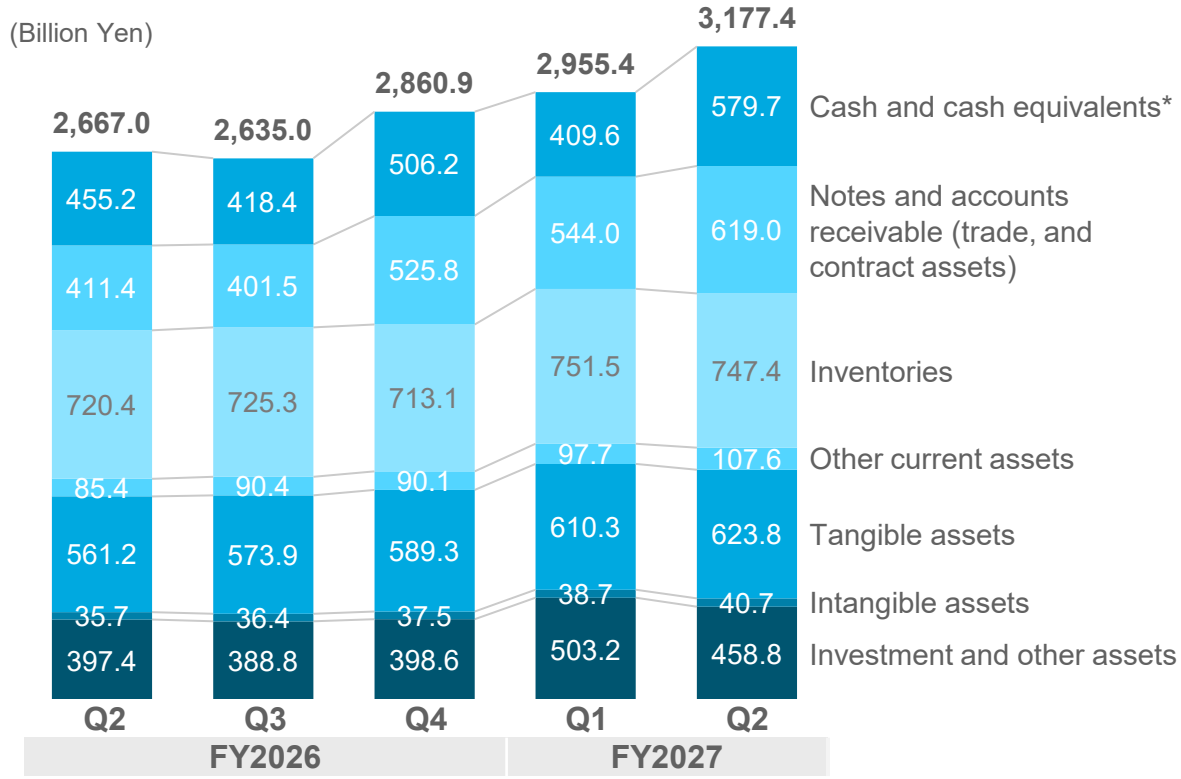
1. SPE: Semiconductor Production Equipment
2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

Field Solutions Sales (Quarterly)

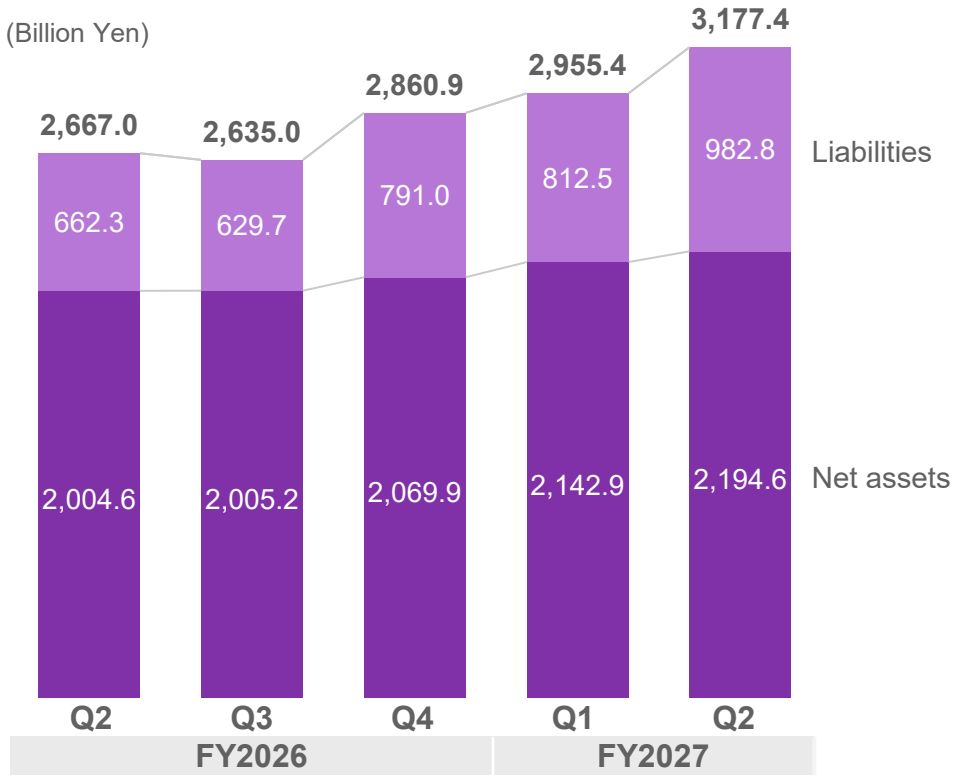


Balance Sheet (Quarterly)

Assets



Liabilities and Net Assets



*Cash and cash equivalents: “Cash and deposits” + “Short-term investments”, etc. (“Securities” in Balance Sheet).

Cash Flow (Quarterly)



	FY2025			FY2026				FY2027	
	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
Cash flow from operating activities	148.6	-15.0	264.8	74.9	175.8	83.1	205.7	118.7	**351.1**
Cash flow from investing activities*1	-54.4	-49.0	-38.9	-54.1	-86.7	1.2	33.2	-38.1	**-40.6**
Cash flow from financing activities	-0.6	-170.1	-23.5	-151.1	-1.0	-122.3	-150.8	-178.4	**-139.6**
Free cash flow*3	94.1	-64.1	225.8	20.7	89.1	84.3	239.0	80.5	**310.4**
Cash on hand*4	525.5	295.5	496.2	367.5	455.2	418.4	506.2	409.6	**579.7**

*1 Cash flow from investing activities excludes changes in time deposits and short-term investments.

*2 The amount for share repurchase excludes the cost incurred to purchase odd-lot shares.

*3 Free cash flow = “Cash flow from operating activities” + “Cash flow from investing activities” (excluding changes in “Time deposits” and “Short-term investments”).

*4 Cash on hand includes “Cash and cash equivalents” + “Time deposits and short-term investments” with original maturities of more than three months.

Consolidated 10-year Financial Summary

(Millions of yen)

	FY2017	FY2018	FY2019	FY2020	FY2021	FY2022	FY2023	FY2024	FY2025	FY2026
Net sales	799,719	1,130,728	1,278,240	1,127,286	1,399,102	2,003,805	2,209,025	1,830,527	2,431,568	2,443,533
Gross profit	322,291	475,032	526,183	451,941	564,945	911,822	984,408	830,269	1,146,287	1,107,880
Gross profit margin	40.3%	42.0%	41.2%	40.1%	40.4%	45.5%	44.6%	45.4%	47.1%	45.3%
SG&A expenses	166,594	193,860	215,612	214,649	244,259	312,551	366,684	374,006	448,967	482,944
Operating income	155,697	281,172	310,571	237,292	320,685	599,271	617,723	456,263	697,319	624,936
Operating margin	19.5%	24.9%	24.3%	21.0%	22.9%	29.9%	28.0%	24.9%	28.7%	25.6%
Ordinary income	157,549	280,737	321,662	244,979	322,103	601,724	625,185	463,185	707,727	630,338
Income before income taxes	149,116	275,242	321,508	244,626	317,038	596,698	624,856	473,439	706,114	748,180
Net income attributable to oweners of parent	115,208	204,371	248,228	185,206	242,941	437,076	471,584	363,963	544,133	574,454
R&D expenses	83,800	97,103	113,980	120,268	136,648	158,256	191,196	202,873	250,017	277,866
Capital expenditures	20,697	45,603	49,754	54,666	53,868	57,288	74,432	121,841	162,171	216,063
Depreciation and amortization	17,872	20,619	24,323	29,107	33,843	36,727	42,927	52,339	62,148	80,982
Interest-bearing debt	-	-	-	-	-	-	-	-	-	-
Equity	643,094	767,146	880,748	819,301	1,012,977	1,335,152	1,587,595	1,746,835	1,839,929	2,046,298
Total assets	957,447	1,202,796	1,257,627	1,278,495	1,425,364	1,894,457	2,311,594	2,456,462	2,625,981	2,860,997
Debt-to-equity ratio	-	-	-	-	-	-	-	-	-	-
Equity ratio	67.2%	63.8%	70.0%	64.1%	71.1%	70.5%	68.7%	71.1%	70.1%	71.5%
ROE	19.1%	29.0%	30.1%	21.8%	26.5%	37.2%	32.3%	21.8%	30.3%	29.6%
Cash flow from operating activities	136,948	186,582	189,572	253,117	145,888	283,387	426,270	434,720	582,174	539,732
Cash flow from investing activities	-28,893	-11,833	-84,033	15,951	-18,274	-55,632	-41,756	-125,148	-169,609	-96,492
Cash flow from financing activities	-39,380	-82,549	-129,761	-250,374	-114,525	-167,256	-256,534	-325,012	-388,836	-425,359
Net income per share (Yen)	234.09	415.16	504.53	390.19	520.73	935.95	1,007.82	783.75	1,182.40	1,254.57
Cash dividends per share (Yen)	117.00	208.00	253.00	196.00	260.00	468.00	570.00	393.00	592.00	628.00
Number of employees	11,241	11,946	12,742	13,837	14,479	15,634	17,204	17,702	19,573	20,236

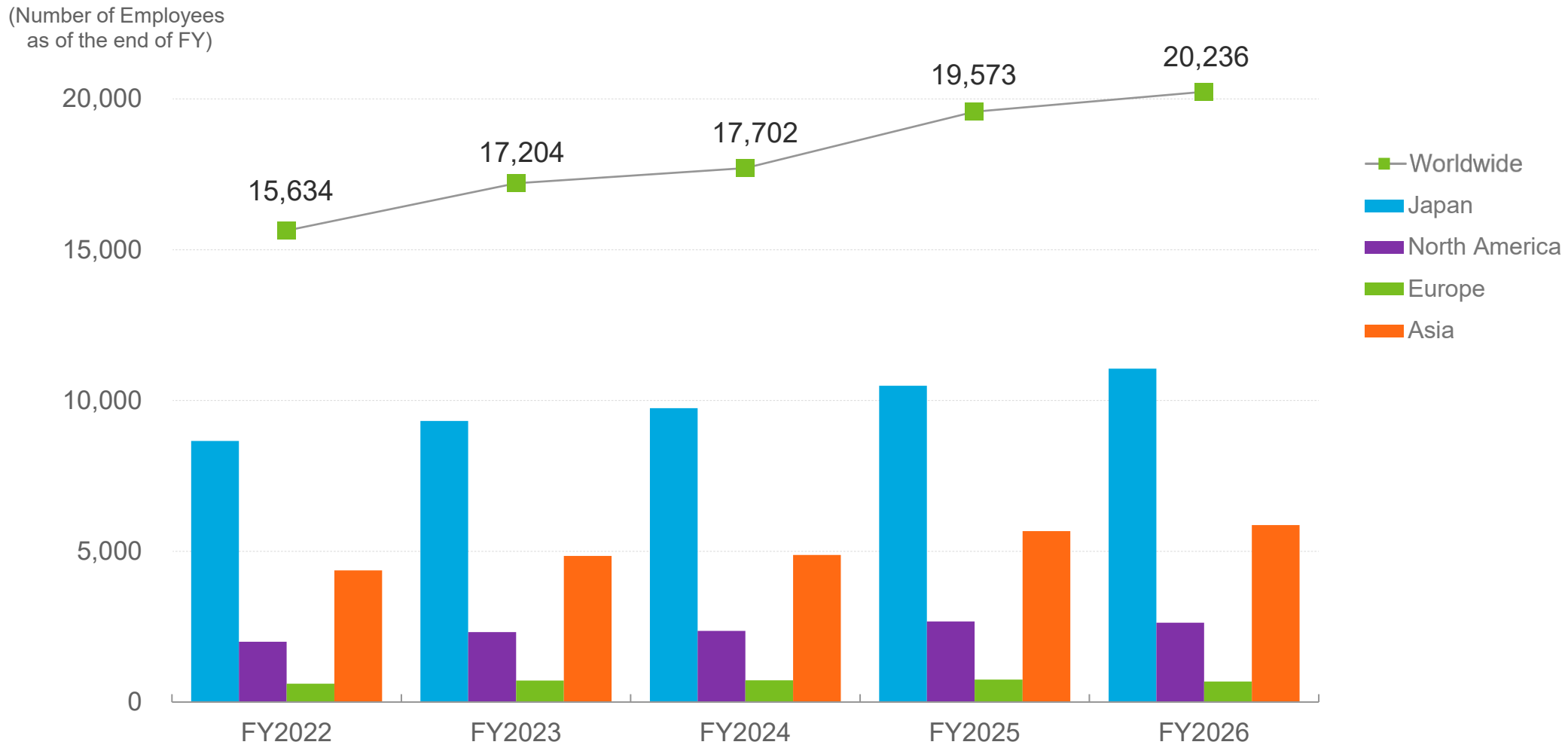
1. From FY2019, the Company adopts “Partial Amendments to Accounting Standard for Tax Effect Accounting” (ASBJ Statement No. 28, revision on February 16, 2018). “Total assets” and "equity ratio" for FY2018 have been restated in the table in accordance with the revised accounting standard.

2. From the beginning of FY2022, the Company applies “Accounting Standard for Revenue Recognition” (ASBJ Statement No. 29).

3. The Company implemented a 3-for-1 common stock split on April 1, 2023. Net income per share and dividend per share (yen) are the figures after the stock split.

4. Some of the data featured in this Investors’ Guide is available for download in Excel format from the "Data Book" section on our website.
https://www.tel.com/ir/library/fb/

Worldwide Employees



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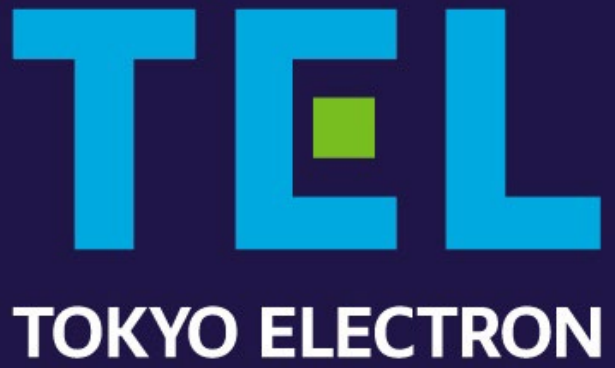
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