

Investors' Guide

August 6, 2026

Tokyo Electron Limited



Contents

1.	<u>TEL Overview</u>	4
2.	<u>Semiconductor and SPE Market Outlook</u>	18
3.	<u>Corporate Principles and New Medium-term Management Plan</u>	27
4.	<u>Business Environment and Financial Estimates</u>	35
5.	<u>Sustainability</u>	48
6.	<u>Diversity of Semiconductor Technology ~Technology Roadmap~</u>	60
7.	<u>SPE New Equipment Initiatives</u>	66
7-1	<u>Frontend, Patterning Technologies</u>	70
7-2	<u>Frontend, Unit Process</u>	78
7-2-1	<u>Etch System</u>	79
7-2-2	<u>Deposition System</u>	88
7-2-3	<u>Cleaning System</u>	95
7-3	<u>Backend Business Strategy</u>	102
8.	<u>MAGIC Market and Field Solutions Business Initiatives</u>	118
9.	<u>Digital Transformation (DX) Initiatives</u>	125
10.	<u>Procurement and Manufacturing Strategy</u>	130
	Appendix : <u>Data Section</u>	137

Updates

Slide Title	Updates
TEL's Strengths	Updated with the latest data
Worldwide Operations R&D Map	Updated as of July 1, 2026
The Market TEL Participates in Outlook for the Semiconductor Market	Reflected latest third-party market data
Business Environment and Financial Estimates	Updated with Q1 FY2027 earnings briefing presentation
Corporate Governance Framework (Audit & Supervisory Board System)	Updated with the latest data
Logic Technology Roadmap (Generic) DRAM Technology Roadmap (Generic) NAND Technology Roadmap (Generic) EUV Lithography Technology Roadmap in Logic	Updated with the latest data
Deposition System Backend Business Strategy	Updated with the latest data
Appendix: Data Section	Updated with Q1 FY2027 results

1. TEL Overview

Company Profile

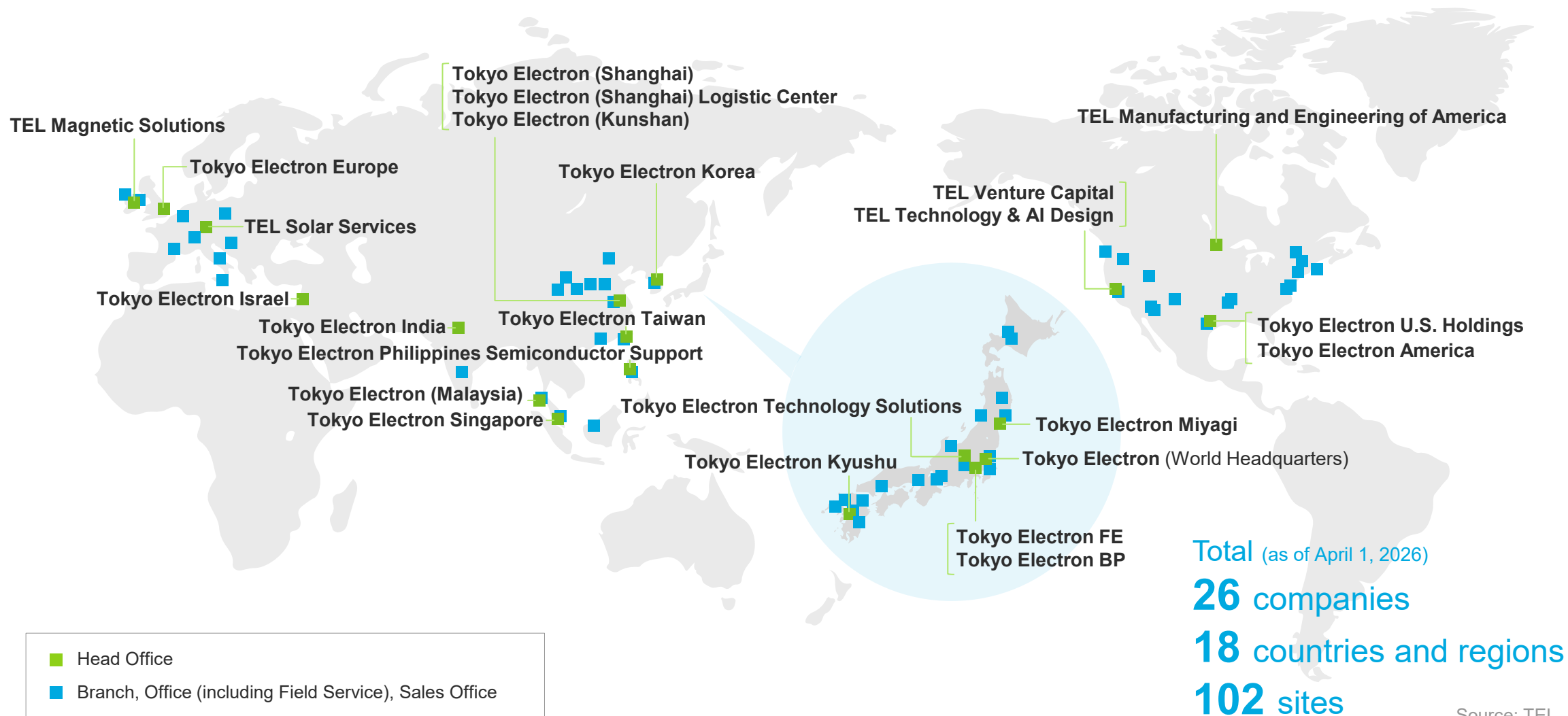
Established	November 11, 1963
Major Products and Services	Semiconductor Production Equipment
Capital	54.9 Billion Yen
Sales/Profit	Net sales 2,443.5 Billion Yen / Operating income 624.9 Billion Yen / Operating margin 25.6% (Fiscal 2026)
Number of Employees	2,436 (non-consolidated) 20,812 (consolidated) (as of April 1, 2026)
Global Network	Japan: 6 companies / 30 sites Overseas: 20 companies / 17 countries and regions / 72 sites Total: 26 companies / 18 countries and regions / 102 sites (consolidated) (as of April 1, 2026)



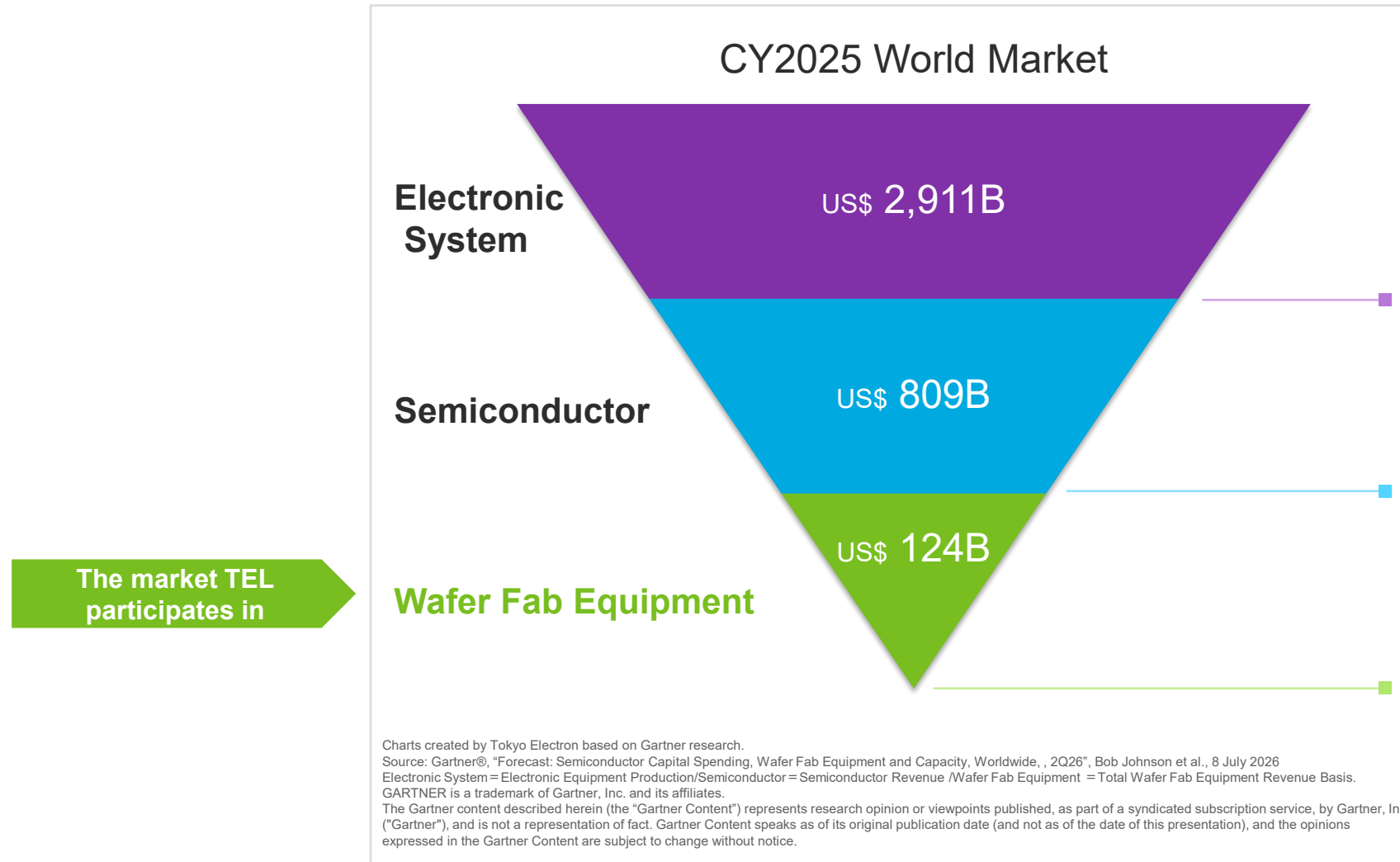
Source: TEL

Worldwide Operations

(As of Jul 1, 2026)

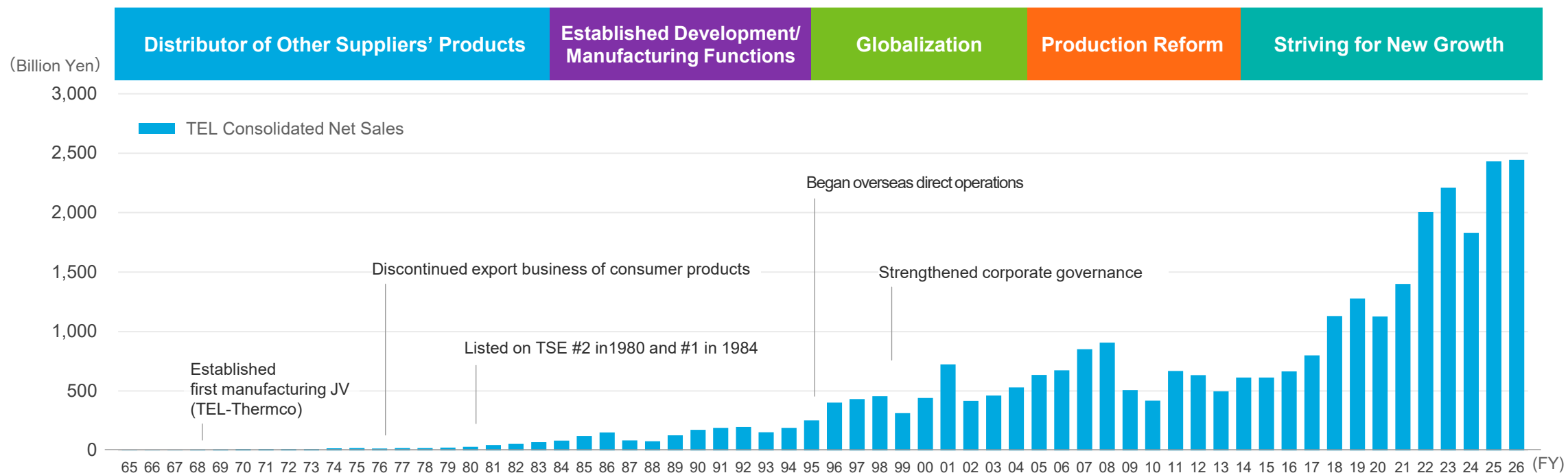


The Market TEL Participates in



Source: Licensed Image

TEL's Growth

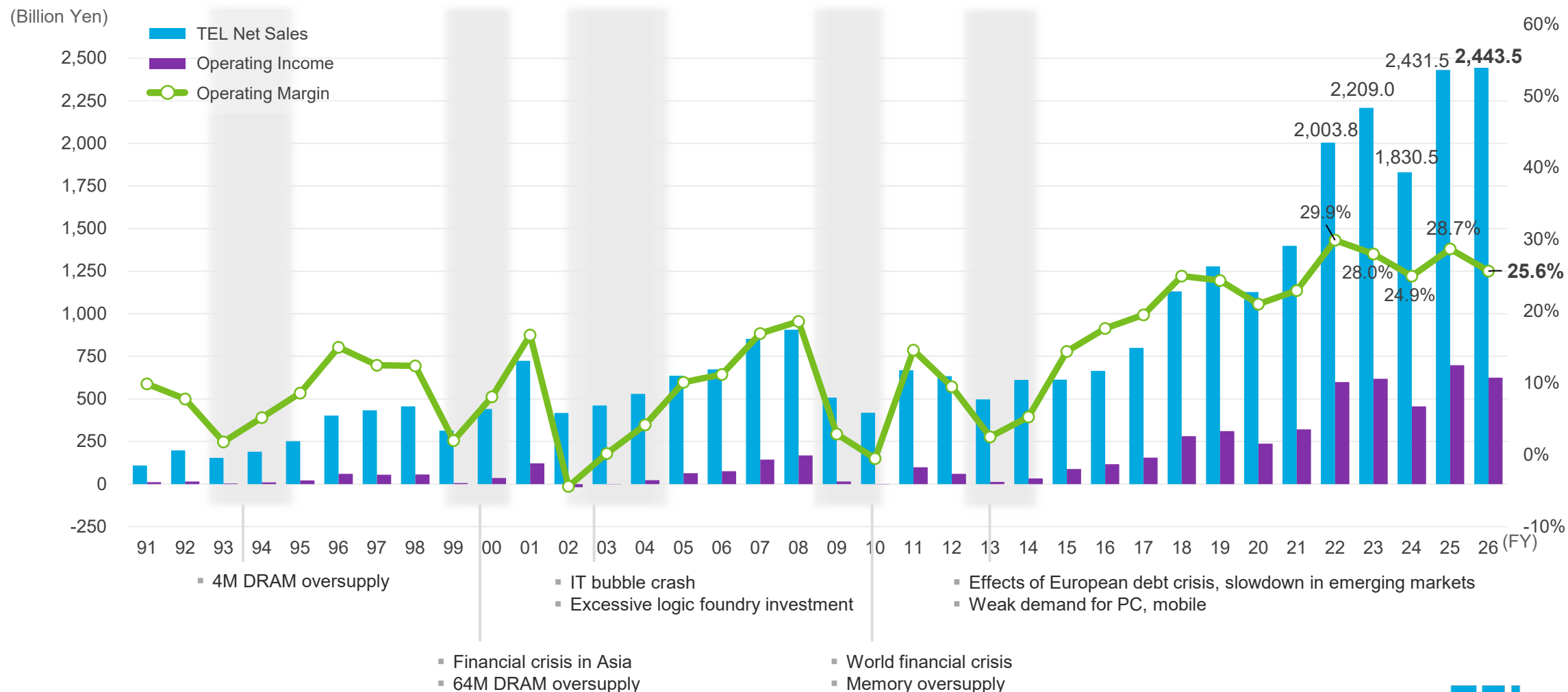


Expansion of Semiconductor Applications*



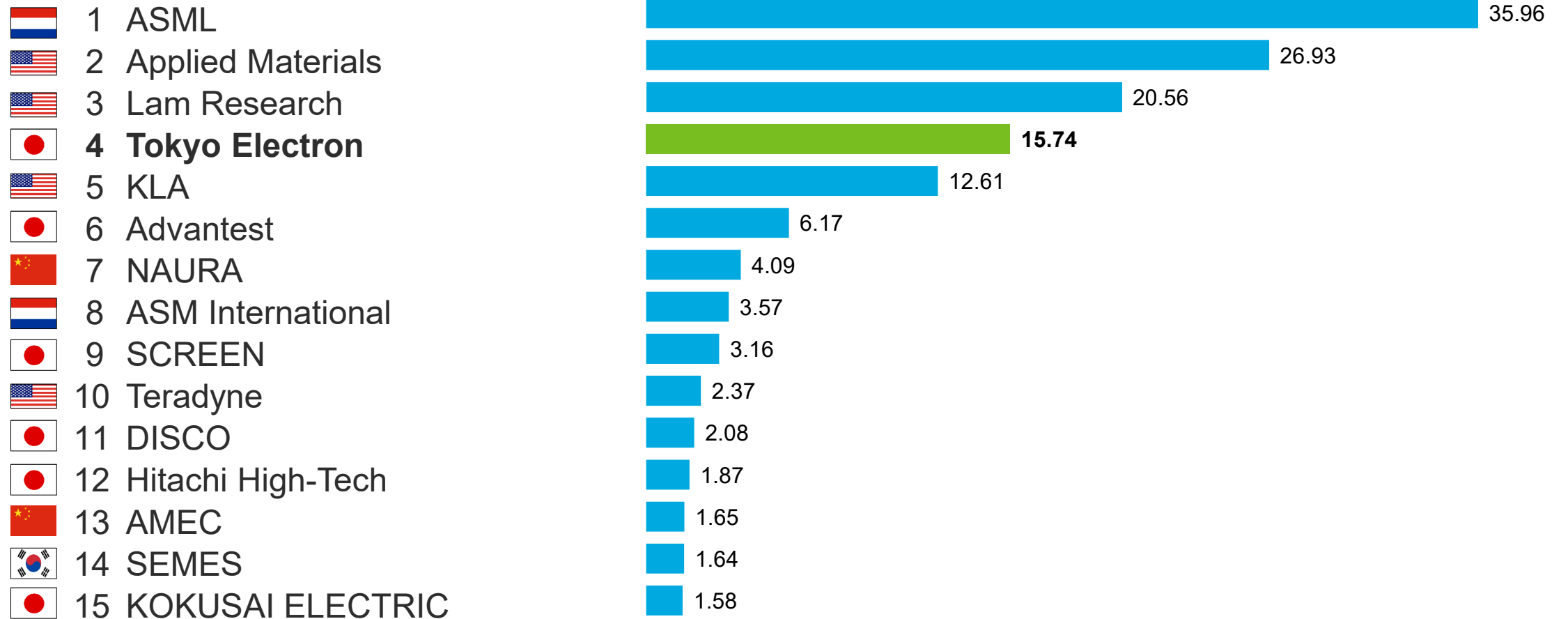
Source: Licensed Image

Financial Performance: Sales and Operating Margin



CY2025 SPE Makers Top 15

CY2025 Sales (Billions of US\$)



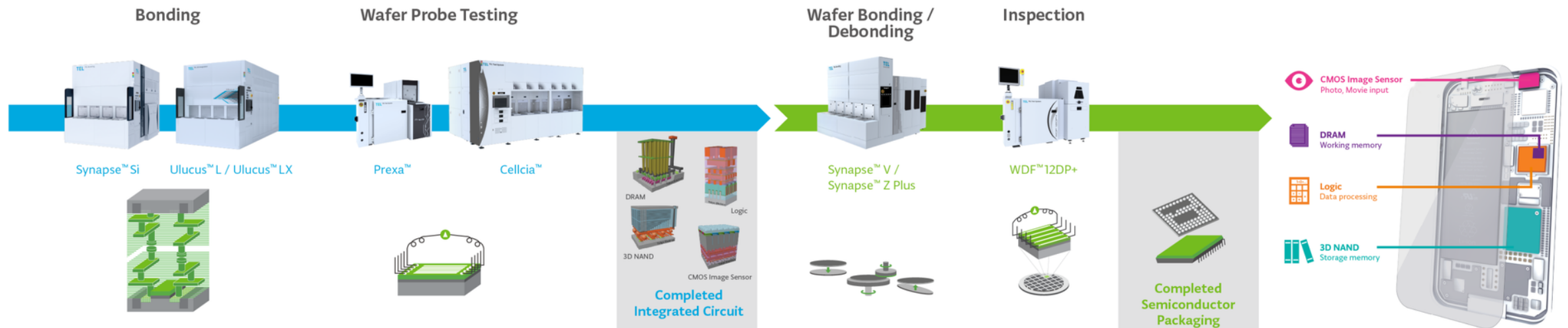
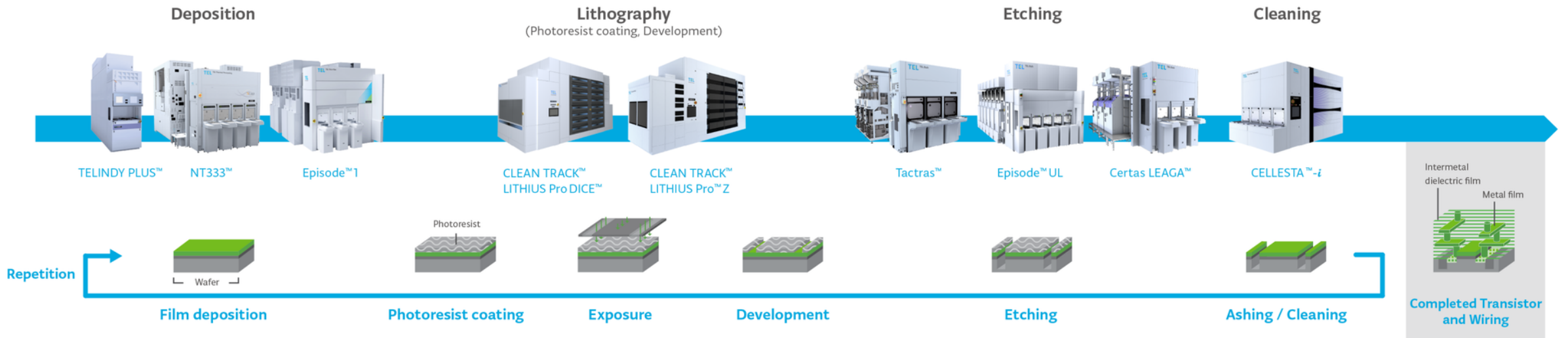
Source: Licensed Image

Source : TechInsights Inc., May 2026

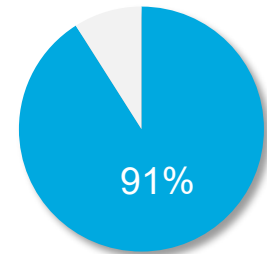
Semiconductor Manufacturing Process

Source: TEL TELCBC-SMP-001

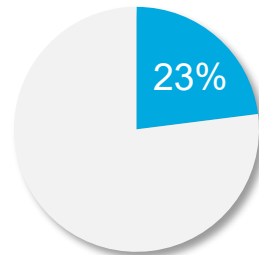
- Wafer Process (Front-end)
- Assembly and Test Process (Back-end)



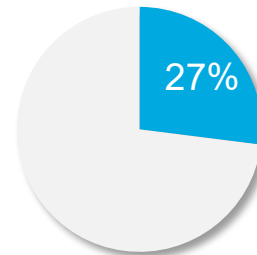
World Market Share of Major Products (CY2025)



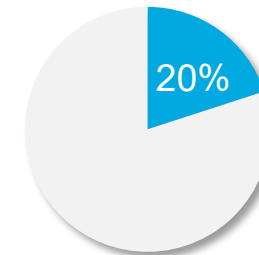
Coater/Developer



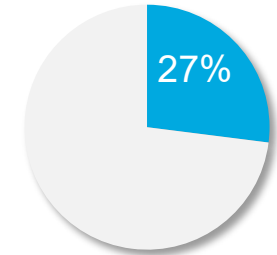
Dry Etch System



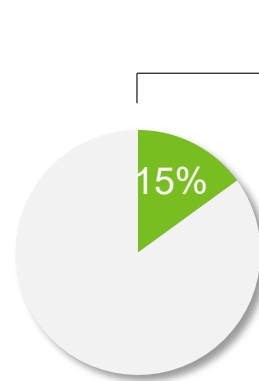
Deposition System



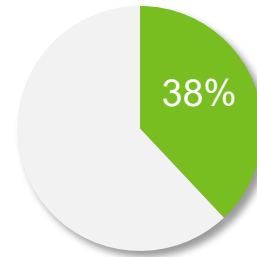
Cleaning System



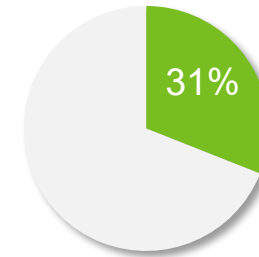
Wafer Bonder



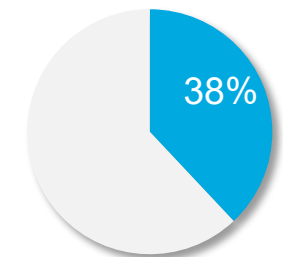
ALD



CVD



Oxidation/Diffusion



Wafer Prober

Source

Gartner®, Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2025, Bob Johnson and Menglin Cao, 2 April 2026, Revenue from Shipments basis. Chart created by TEL based on Gartner research.

Gartner research. Calculations performed by TEL.

Coater/Developer: Photoresist Processing (Track), Dry Etch System: Dry Etch, Deposition System: Tube CVD + Atomic Layer Deposition Tools + Oxidation/Diffusion Furnaces + Nontube LPCVD, ALD: Atomic Layer Deposition Tools, CVD: Tube CVD + Nontube LPCVD, Oxidation/Diffusion: Oxidation/diffusion Furnaces, Cleaning System: Single Wafer Processors + Wet Stations + Batch Spray Processors + Scrubbers + Other Clean Equipment, Wafer Bonder: Wafer Bonder.

GARTNER is a trademark of Gartner, Inc. and its affiliates. Gartner does not endorse any company, vendor, product or service depicted in its publications, and does not advise technology users to select only those vendors with the highest ratings or other designation. Gartner publications consist of the opinions of Gartner's business and technology insights organization and should not be construed as statements of fact.

Gartner disclaims all warranties, expressed or implied, with respect to this publication, including any warranties of merchantability or fitness for a particular purpose. The Gartner content described herein (the "Gartner Content") represents research opinion or viewpoints published, as part of a syndicated subscription service, by Gartner, Inc. ("Gartner"), and is not a representation of fact. Gartner Content speaks as of its original publication date (and not as of the date of this Presentation), and the opinions expressed in the Gartner Content are subject to change without notice.

Source

SPE (Wafer Prober) : Auto Probers,

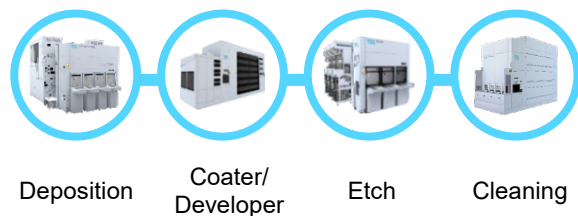
TechInsights Inc., April 2026

Charts/graphics created by Tokyo Electron based on :

TechInsights Inc.

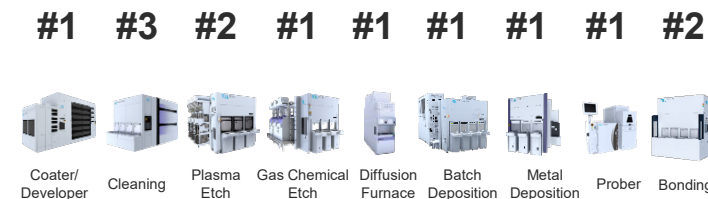
TEL's Strengths

Have advanced products
for the 4 key process



Top market
share

Major Products & Market Position*



*TEL estimate

100%

Market share of
coater/developer for EUVL

*TEL estimate



No.1

Worldwide installed base

Annual increase by about
4,000~6,000 units*
Industry's largest installed base
100,000~ units*

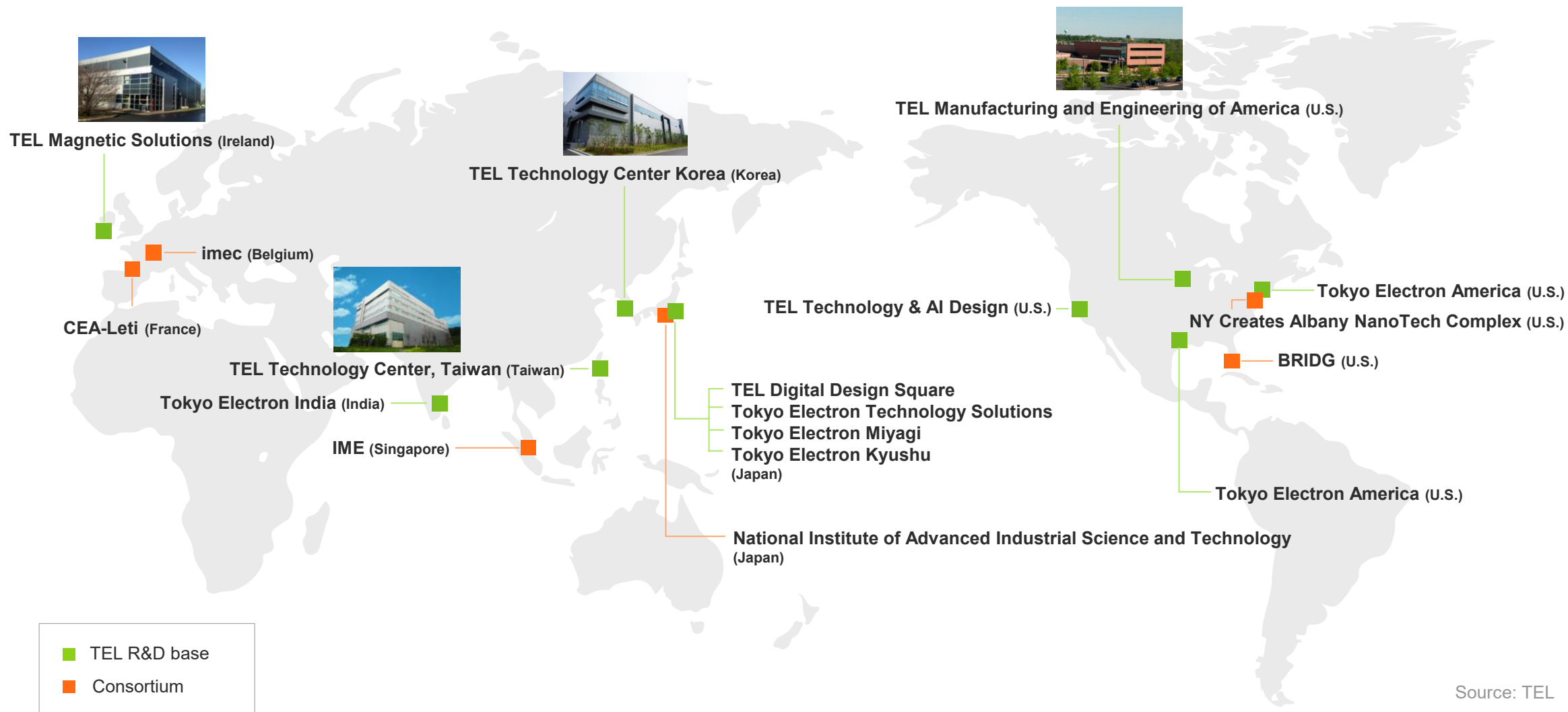


* As of March 2026

Source: Licensed Image

R&D Map

(As of Jul 1, 2026)



Source: TEL

Strengthen R&D Capabilities

Yamanashi R&D building

Deposition system, gas chemical etch system,
corporate R&D
(Completed in July 2023)



Miyagi R&D building

Etch system
(Completed in April 2025)



Kumamoto R&D building

Coater/Developers, surface preparation system, Bonder
(Completed in October 2025)



Miyagi Technology Innovation Center

Etch system
(Completed in September 2021)



TEL Digital Design Square

DX, Software
(Began operation in November 2020)



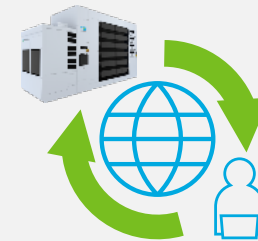
Source: TEL

Continually Pursuing the Best Products and Best Service

Front-loading



Advanced field solutions

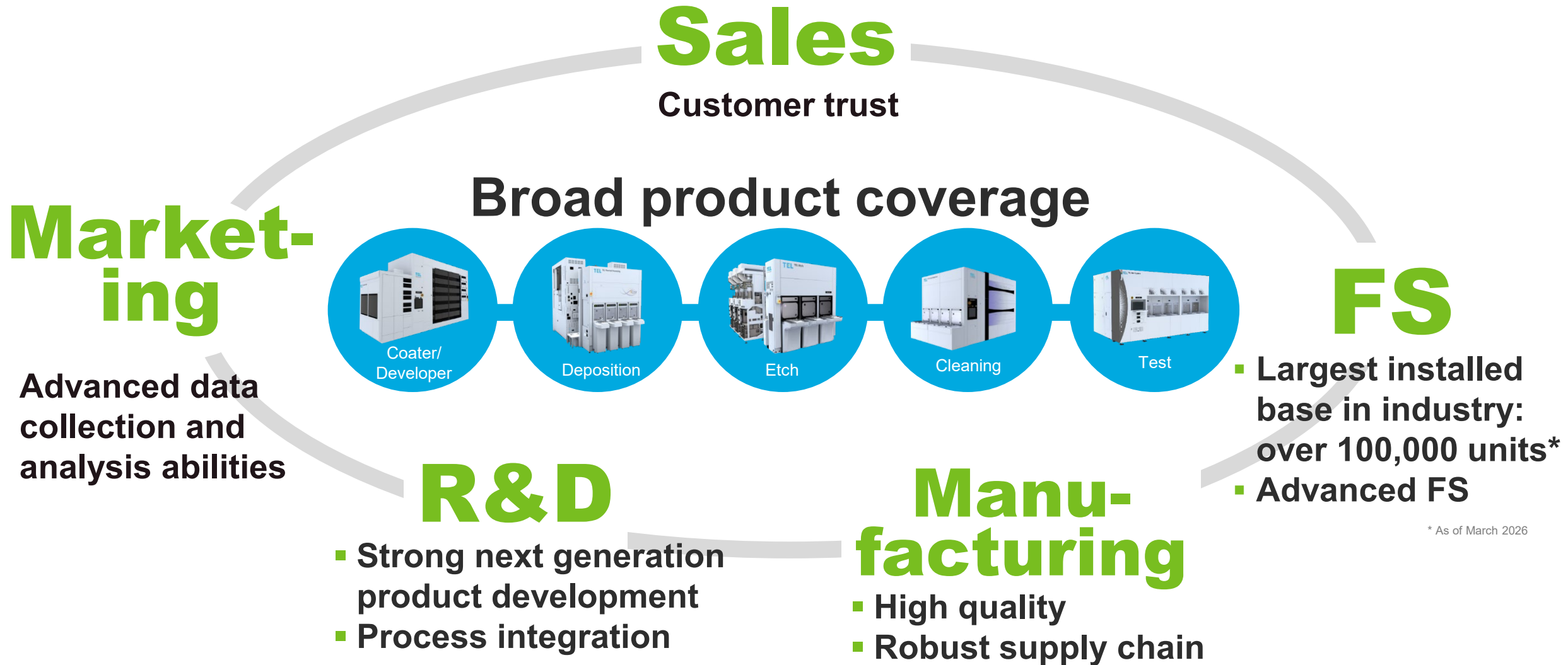


- Share roadmap for next several generations with customers
- Promote early engagement
- Realize maximum yield of customer devices and equipment availability from early stage of customers' mass production and reduce burden on the environment
- Further increase investment in human resources/R&D by raising operational efficiency and driving higher per-employee productivity

- Business development leveraging industry's largest installed base of over 100,000 units*
- TELeMetrics™ remote maintenance
- Predictive maintenance with machine learning

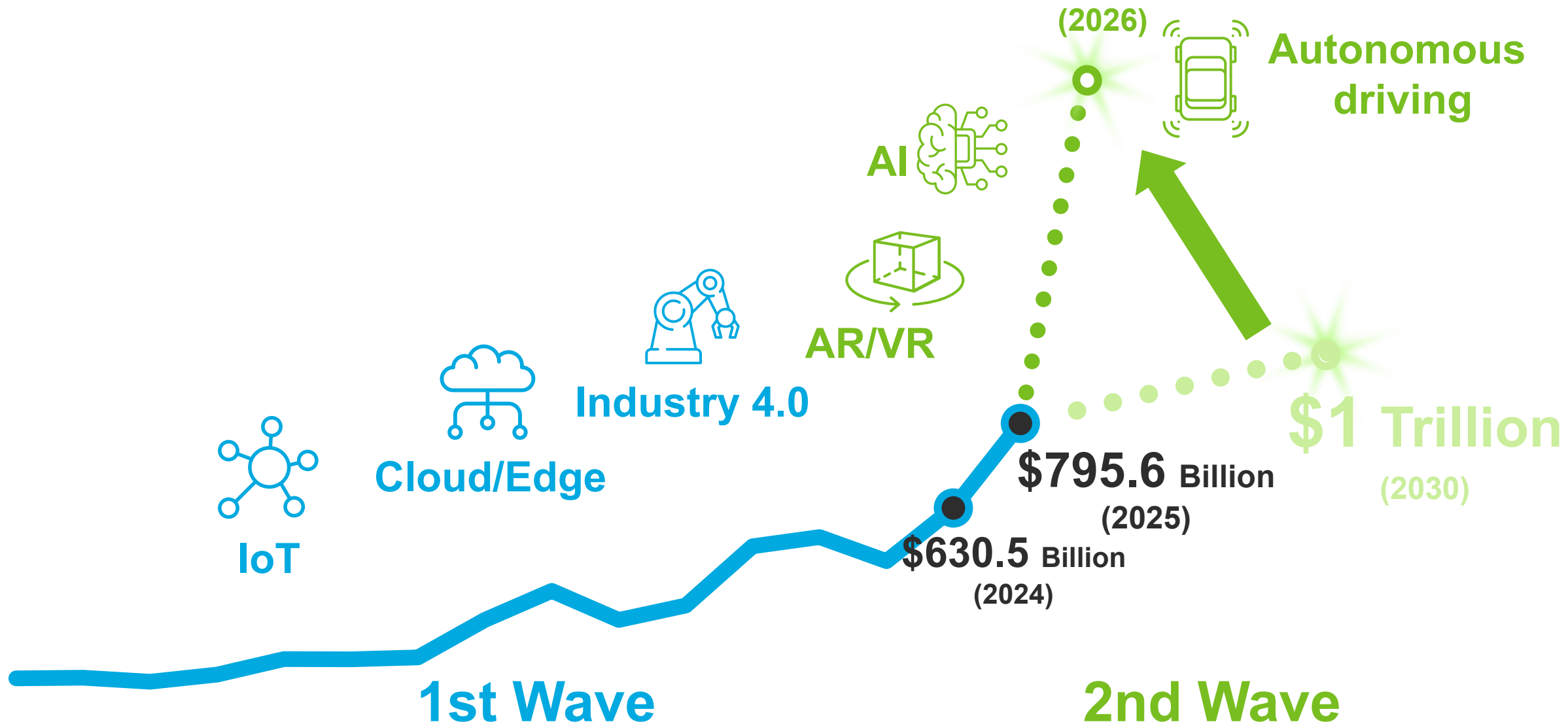
* As of March 2026

Maximize Utilization of TEL's Comprehensive Strengths

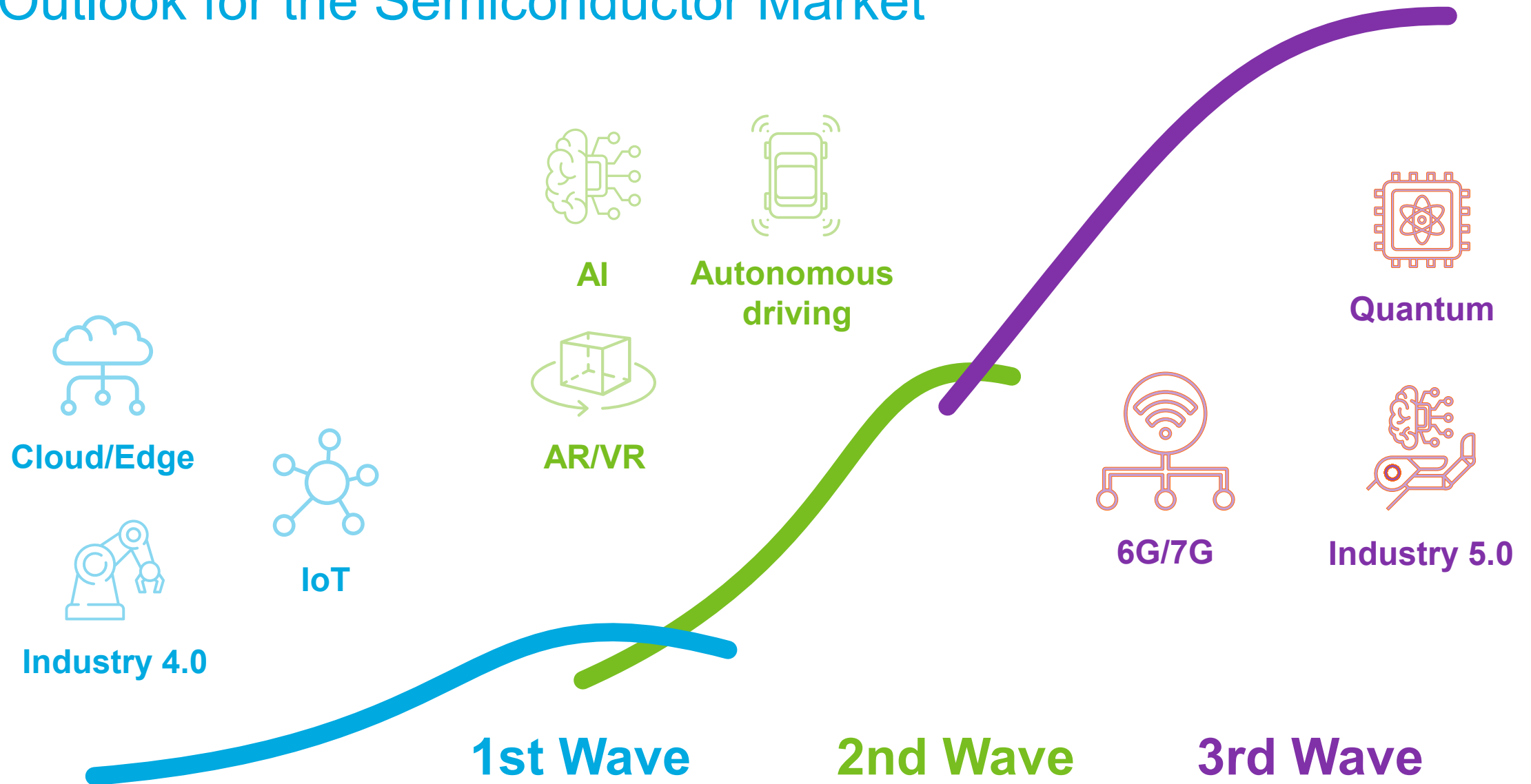


2. Semiconductor and SPE Market Outlook

Outlook for the Semiconductor Market **\$1.5 Trillion**

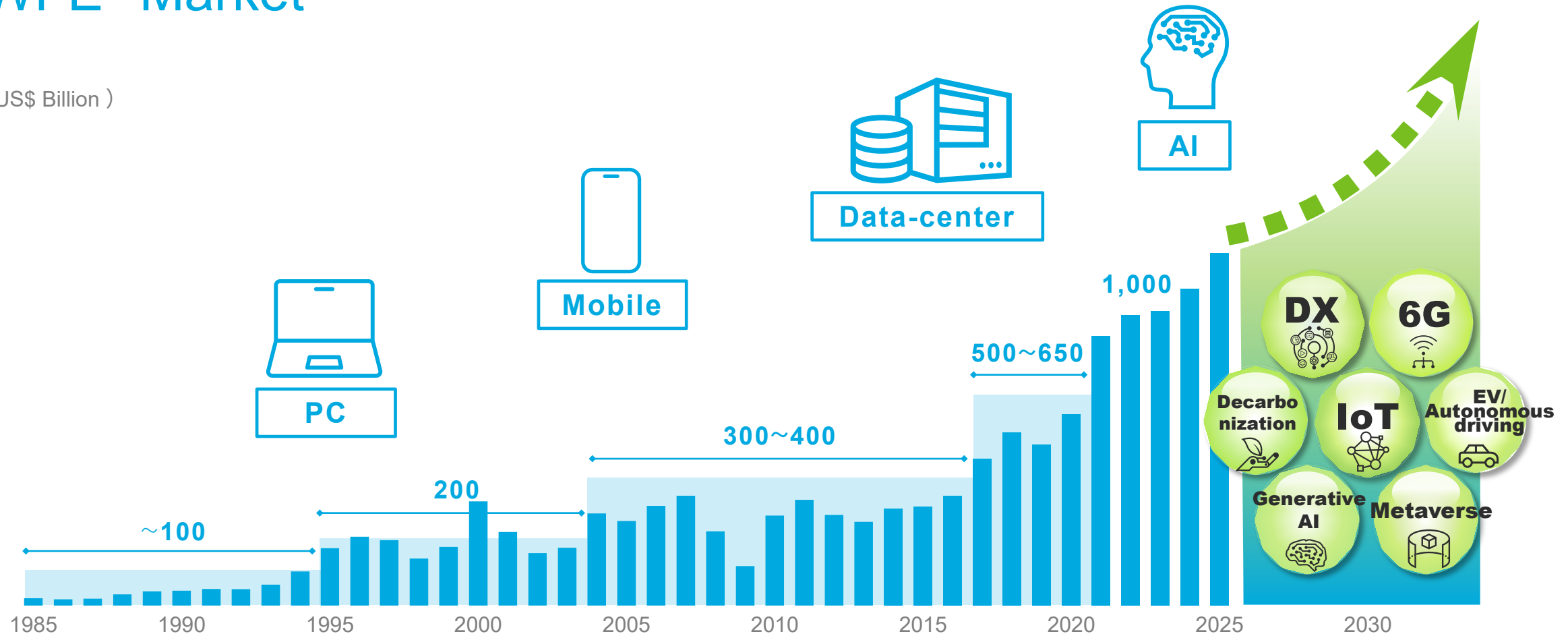


Outlook for the Semiconductor Market



WFE* Market

(US\$ Billion)



* WFE (Wafer Fab Equipment): The semiconductor production process is divided into front-end production, in which circuits are formed on wafers and inspected, and back-end production, in which wafers are cut into chips, assembled and inspected again. WFE refers to the production equipment used in front-end production and in wafer-level packaging production.

Source : TechInsights Inc. (1985~2025)

WFE Market will grow further with progress of digitalization
and evolution of semiconductors

Green Future Through Semiconductor Evolution

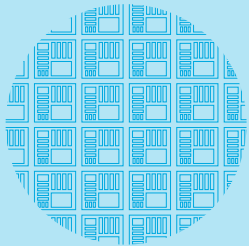
Digital & Green

Higher
Speed

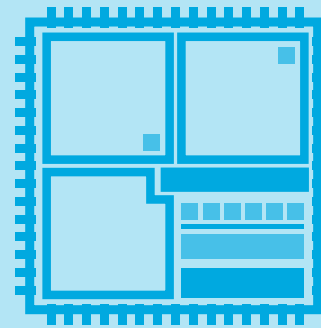
Larger
Capacity

Superior
Reliability

Lower Power
Consumption



Physical Scaling



Heterogeneous
Integration

Physical Scaling x Heterogeneous Integration

Frontend

AI Semiconductor

Advanced
Packaging

Logic
GAA * / CFET

Heat Spreader

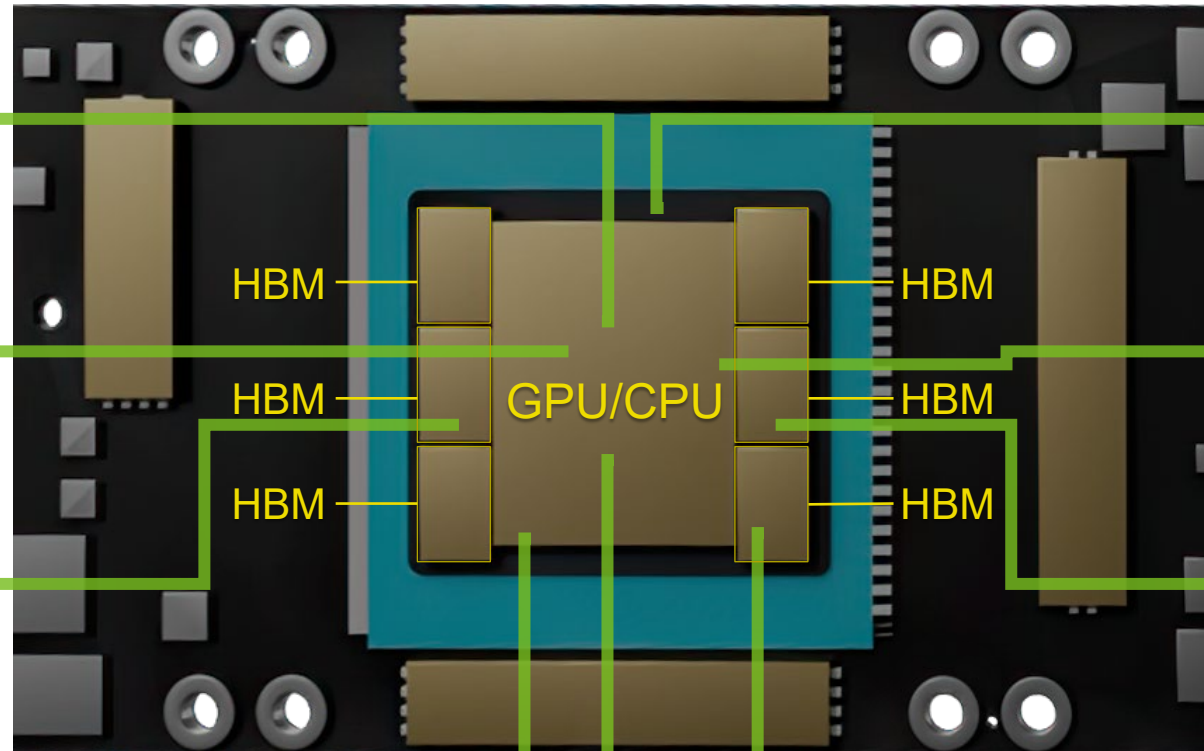
Logic
Backside PDN *

3DIC
Chiplet Integration

DRAM
4F² VCT * / 3D DRAM

Stack Memory
HBM, etc.

Super Flat Wafer



Source: TEL

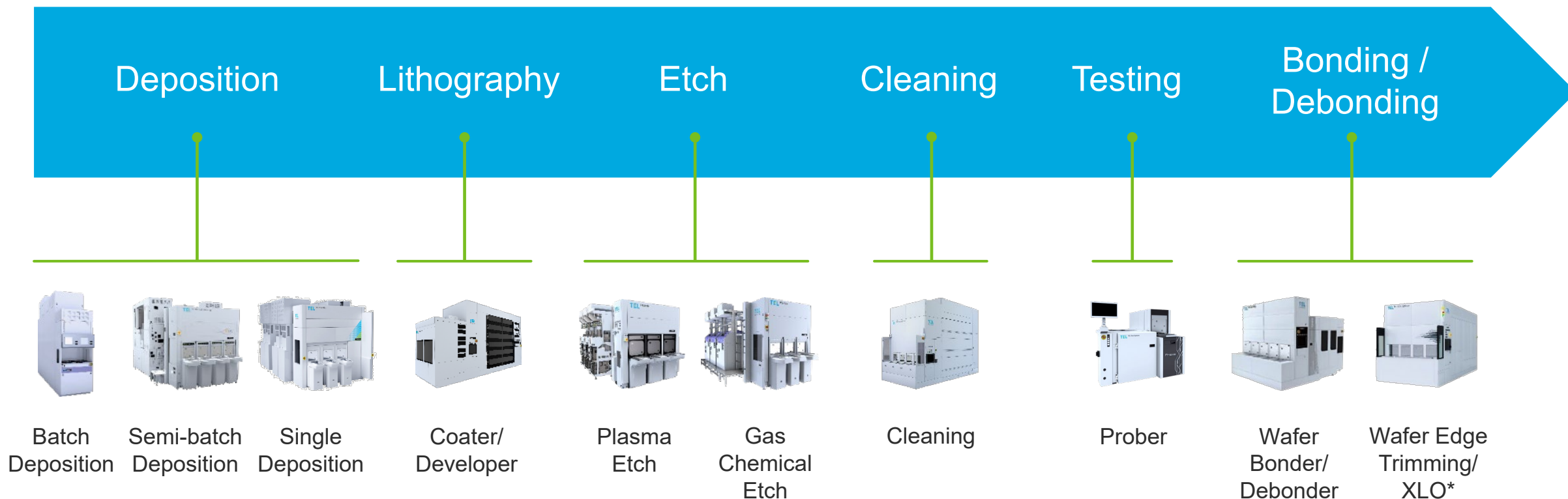
Known Good Die

* GAA : Gate All Around
* Backside PDN : Backside Power Delivery Network
* VCT : Vertical Channel Transistor

Expanding Opportunities: Wide Product Portfolio

Frontend

Advanced Packaging



*XLO: Extreme Laser Lift Off

Growing Opportunities: Scaling x Heterogeneous Integration

Etch

>500 B yen

- DRAM Etchers for Interconnect:
Growth driven by increased investment in HBM with more interconnect layers
Cumulative sales over 500 billion yen expected by 2030

Bonder Laser

>500 B yen

- 3D Integration Equipment including Bonders:
Rapid expansion across all applications
Cumulative sales over 500 billion yen expected by 2030

Prober

**CAGR
>15%**

- Probers for AI/HPC:
Driven by longer test times and more process steps, projecting CAGR over 15% (CY2025-CY2030)

Die Prober PECVD

**SAM
+10%**

- Die Probers:
Development and evaluation agreed with customers
Creating 10-15% of the prober market SAM
- PECVD for Gap Fill:
SAM estimated to be approx. 10% of PECVD market
Evaluations progressing with multiple customers

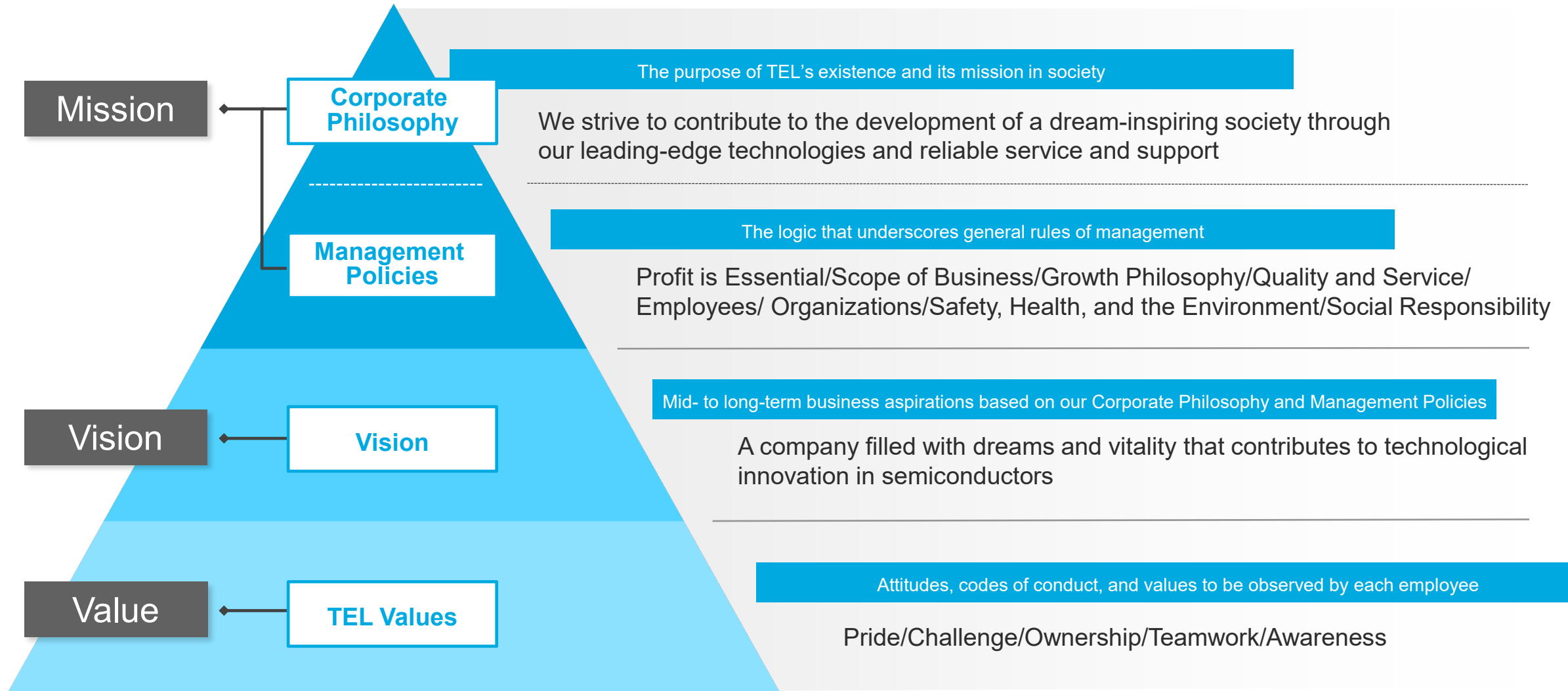


Strategic Technologies for Future Growth

Frontend		
Logic : GAA, BSPDN ▪ EUV Coater/Developer ▪ Gas Chemical Etch ▪ Conductor Etch ▪ PVD Metal Overburden ▪ CFET/Inner Spacer Plasma CVD for filling film ▪ Double-sided scrubber ▪ Backside/bevel cleaning ▪ Pattern Shaping ▪ Wafer Bonder ▪ Laser Tool	DRAM: 2D & 3D DRAM ▪ EUV Coater/Developer ▪ Capacitor Mold Etch ▪ Batch High-k Capacitor deposition ▪ PVD Metal Hardmask ▪ Supercritical Cleaning ▪ Backside/bevel Cleaning ▪ Wafer Bonder ▪ Laser Tool	NAND: Beyond 4xx ▪ Slit Etch ▪ Channel Hole Etch (Plug) ▪ Batch low-resistance metallization ▪ Batch Cleaning WL Separation ▪ Wafer Bonder ▪ Laser Tool
Advanced Packaging		
Logic Packaging ▪ Interposer, Polyimide & PR Coater/Developer ▪ TDV Etch ▪ Batch High-k Capacitor depo ▪ Wafer Bonder ▪ Laser Tool	HBM Packaging ▪ Polyimide & PR Coater/Developer ▪ Metal Etch for HBM ▪ Aerosol Cleaning ▪ Temporary Bonder/Debonder	Advanced Logic / Memory Test ▪ Prober

3. Corporate Principles and New Medium-term Management Plan

Corporate Principles System



Vision

A company filled with dreams and vitality that contributes to technological innovation in semiconductors

Tokyo Electron pursues technological innovation in semiconductors that supports the sustainable development of the world.

We aim for medium- to long-term profit expansion and continuous corporate value enhancement by utilizing our expertise to continuously create high value-added leading-edge equipment and technical services.

Our corporate growth is enabled by people, and our employees both create and fulfill company values. We work to realize this vision through engagement with our stakeholders.

Technology Enabling Life

“Technology Enabling Life” is our corporate message that expresses the Corporate Principles which consist of our Corporate Philosophy, Management Policies, Vision and TEL Values.

CSV

(Creating Shared Value)

The concept is to create social and economic value by leveraging corporate expertise to solve social issues, hereby enhancing corporate value and achieving sustainable growth.



TSV

TEL's Shared Value



- Pursue technological innovation in semiconductors that supports the sustainable development of the world
- Continuously create high value-added leading-edge equipment and technical services
- Medium- to long-term profit expansion and continuous corporate value enhancement
- Engagement with our stakeholders

Realization of Vision = Creating Shared Value in TEL

Our Approaches to Social Issues

Sustainable development of the world / Diversification of values and happiness

Solutions

Online/Metaverse



AI diagnosis/Prevention/Robots



Smartification



EV/Autonomous driving/MaaS



Technologies

Higher speed
communication
(5G/6G)

Cloud/Edge
Computing

AI

IoT

AR/VR/MR

Semiconductors

Logic

Memory

Power

Analog

Sensor

Display

TEL

**Pursue technological innovation in semiconductors :
Larger capacity/Higher speed/Higher reliability/Lower power consumption**

Higher definition/Flexible
/Lower power consumption

Source: Licensed Image

Vision & Medium-term Management Plan

FY2023

FY2027

FY2031 (CY2030)

■ Goals for 2030

- Supporting sustainable development in the world
 - ① Driving the semiconductor market through technological innovation
 - ② Contributing to a sustainable global environment
- Medium- to long-term profit expansion and continuous corporate value enhancement
- Engaging with our stakeholders

■ Medium-term Management Plan (FY2023-2027)

- Achievement of Financial Model
(Five-year goal toward 2030)

Realization of Vision

A company filled with dreams and vitality
that contributes to technological
innovation in semiconductors

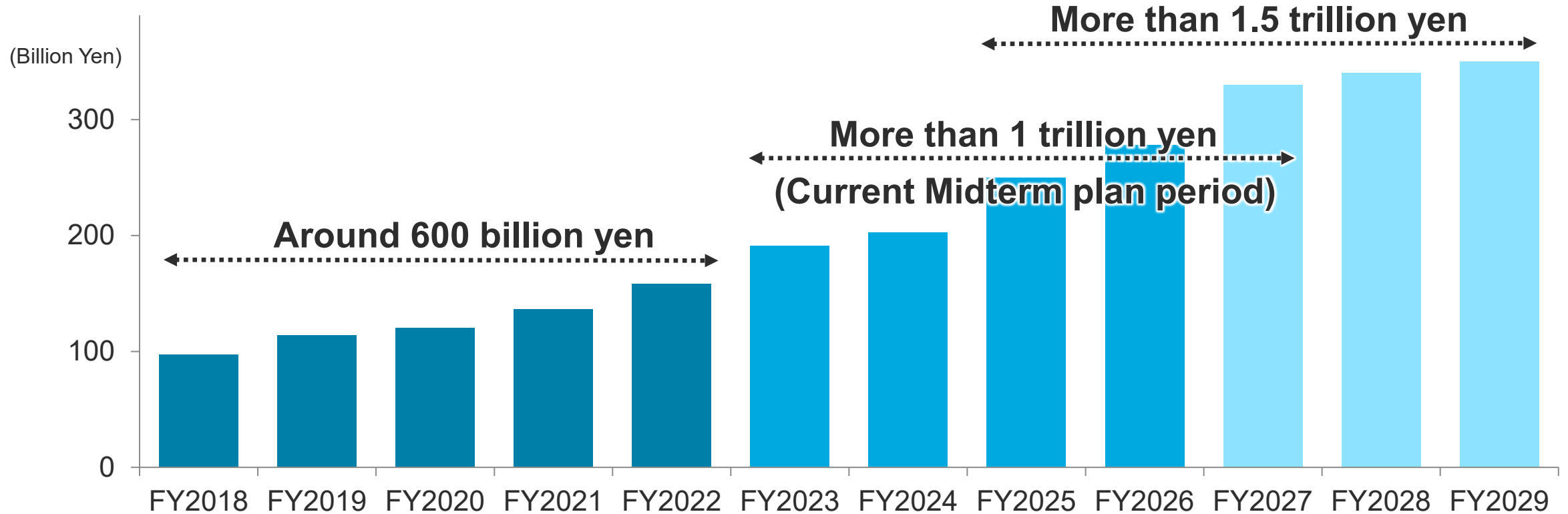


Aiming to achieve the Medium-term Management Plan
by FY2027 with a view to realizing Vision in 2030

The New Medium-term Management Plan : Financial Targets

Financial Targets (FY2023 - FY2027)	
Net sales	≥ 3 trillion yen
OP margin	$\geq 35\%$
ROE	$\geq 30\%$

Aggressive Investment in R&D

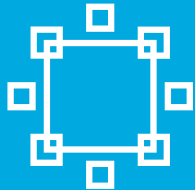


Driving the creation of high-value next-generation products
through further growth investments

Investment for Future Growth (FY2025 to FY2029)

R&D Investment

1.5
trillion yen



Capex

700
billion yen



Recruitment

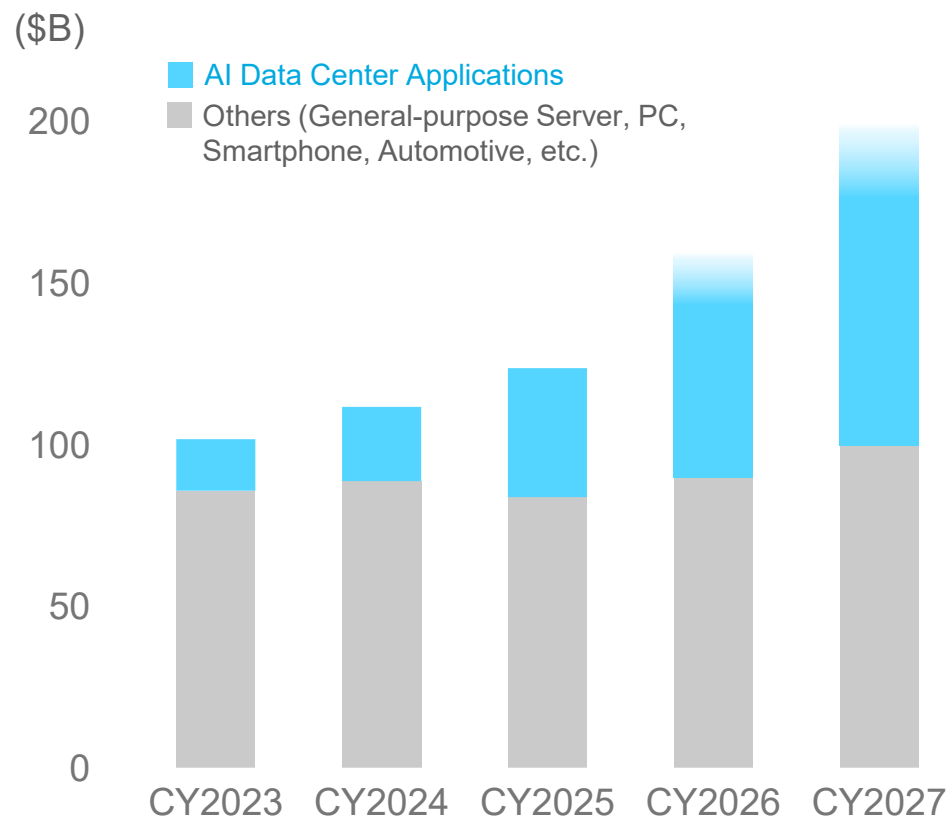
10,000
people
2,000 people/year



4. Business Environment and Financial Estimates

Business Environment (WFE Market Outlook as of July 2026)

WFE Market Trend



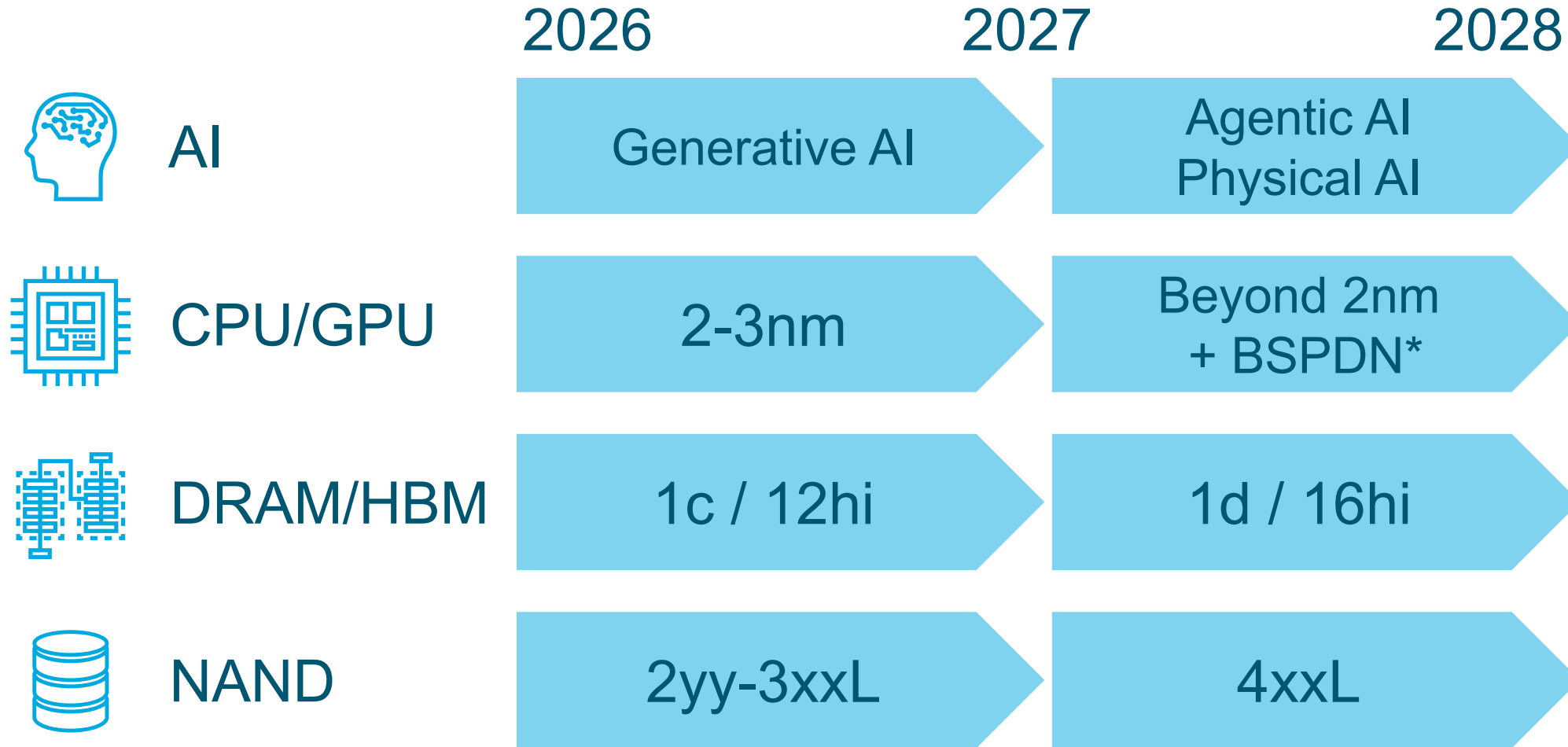
WFE Market Outlook

- CY2026: \$150B+
- CY2027: \$190B+
- Demand for general-purpose memory /CPU is increasing as well as for GPU/HBM
- Investment plans for leading-edge chips are accelerating

WFE for AI data centers are growing to exceed 50% of total

With our strong position in advanced areas, our opportunities are expanding even further

Evolution of AI and Semiconductor Technology Trends



Significant technological innovations are happening across devices as AI evolves

* BSPDN (Backside Power Delivery Network) : Structures that arrange power delivery networks on the backside of silicon wafer

Status of Financial Targets for Medium-term Management Plan

Financial Targets (~March 2027)		
Net Sales	≥ 3 trillion yen	On Track
OPM	≥ 35%	In Progress
ROE	≥ 30%	On Track

While achieving our operating profit margin target remains challenging, steady progress to date is putting operating profit of 1 trillion yen within reach

Initiatives to Improve Profitability

1. Develop next-generation systems with higher added value

2. Drive productivity gains through system upgrades

3. Roll out AI- and robotics-enabled service + *Epsira*

4. Enhance startup efficiency and reduce startup lead times

5. Pricing optimization

We will strengthen our ability to generate earnings while remaining agile to market changes

FY2027 Update: Progress and Business Opportunities Ahead

Business Progress (FY2027 Sales Growth Drivers)

Coater/ Developer	Sales Growth 50%+ YoY	- Newly released CLEAN TRACK™ LITHIUS Pro DICE™ ramping steadily POR*¹ advancing across multiple process steps in leading-edge logic/DRAM
----------------------	------------------------------------	--

Etch	Sales Growth 25%+ YoY	Full-year sales of 1T yen is within reach with accelerated investment in leading-edge logic/memory - Evaluations progressing with new model for DRAM HARC etch
------	------------------------------------	--

Advanced Packaging	Sales Growth 70%+ YoY	In particular, our probers hold an overwhelming position in high-end logic. Expect to significantly exceed 100B yen for full year. Evaluations of new model progressing well
--------------------	------------------------------------	---

Future Business Opportunities (Highlights)

From POR to High Volume Manufacturing	- Cryogenic etch - Low-resistivity metal deposition - Hybrid bonding
---------------------------------------	--

Cumulative Sales through 2030	- DRAM interconnect etch: 1T yen - Bonding-related equipment: 500B yen
-------------------------------	--

New Entrants/ SAM Expansion	- Single wafer PECVD for gap fill: 10% of PECVD market - Device prober: 10-15% of prober market. Released Prexa™ SDP*²
-----------------------------------	---

*1 POR (Process of Record): Certification of the adoption of equipment in customers' semiconductor production processes

*2 SDP: Singulated Device Prober

Financial Estimates for H1 FY2027

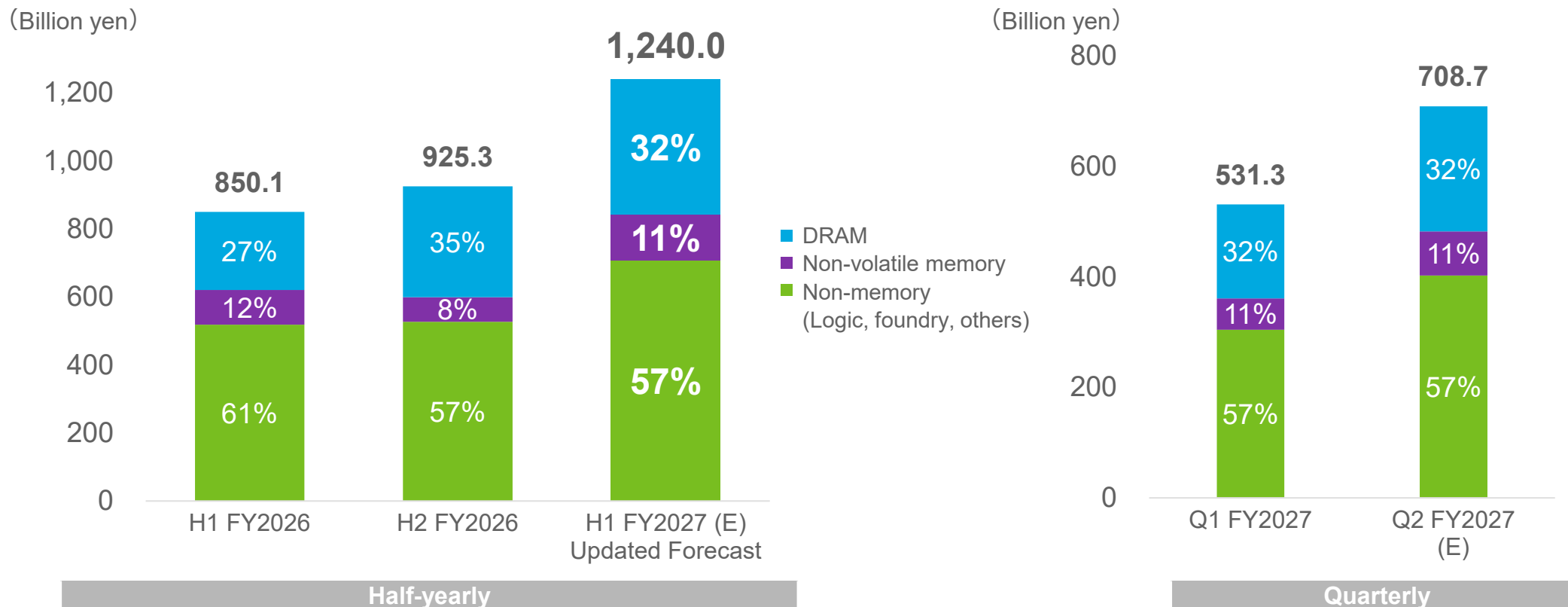
(Billion Yen)

	FY2026 (Actual)			FY2027 (Updated Forecast)	FY2027 (Forecast as of 4/30)
	H1	H2	Full Year	H1	H1
Net sales	1,179.6	1,263.8	2,443.5	1,620.0	1,570.0
Gross profit	538.8	569.0	1,107.8	748.0	715.0
Gross profit margin	45.7%	45.0%	45.3%	46.2%	45.5%
SG&A expenses	235.7	247.2	482.9	290.0	284.0
R&D	134.8	143.0	277.8	160.0	160.0
Other than R&D	100.8	104.1	205.0	130.0	124.0
Operating income	303.1	321.7	624.9	458.0	431.0
Operating margin	25.7%	25.5%	25.6%	28.3%	27.5%
Income before income taxes	312.9	435.1	748.1	464.0	437.0
Net income attributable to owners of parent	241.6	332.8	574.4	349.0	328.0
Net income per share (Yen)	527.31		1,254.57	767.51	721.12

- H1 FY2027:
Revised net sales upward to 1,620B yen due to customers' robust investment in leading-edge applications
- H2 FY2027:
Demand is expected to gain momentum further, raising expectations for a significantly better performance in H2
 - Closely monitoring the impact of the Middle East and supply chain developments

H1 FY2027 SPE New Equipment Sales Forecast

Sales by Application

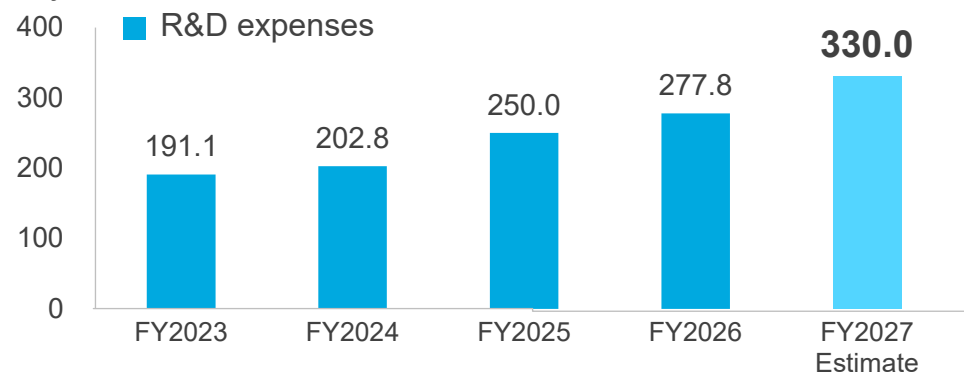


* Percentages on the graph show the composition ratio of new equipment sales. Field solutions sales are not included.

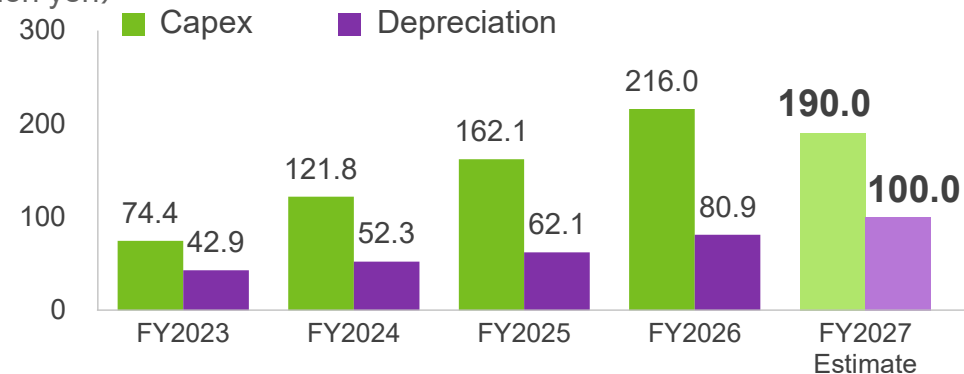
Revised New Equipment sales upward to 1,240B yen
Q2 anticipated to be new record high of 708.7B yen (+33% QoQ)

FY2027 R&D Expenses and Capex Plan

(Billion yen)



(Billion yen)



Kurokawa-gun, Miyagi Prefecture/ Completion scheduled for summer 2027

Goal of the Smart Production Concept

Labor Productivity

4x

Space Efficiency

3x

Production Leadtime

1/3

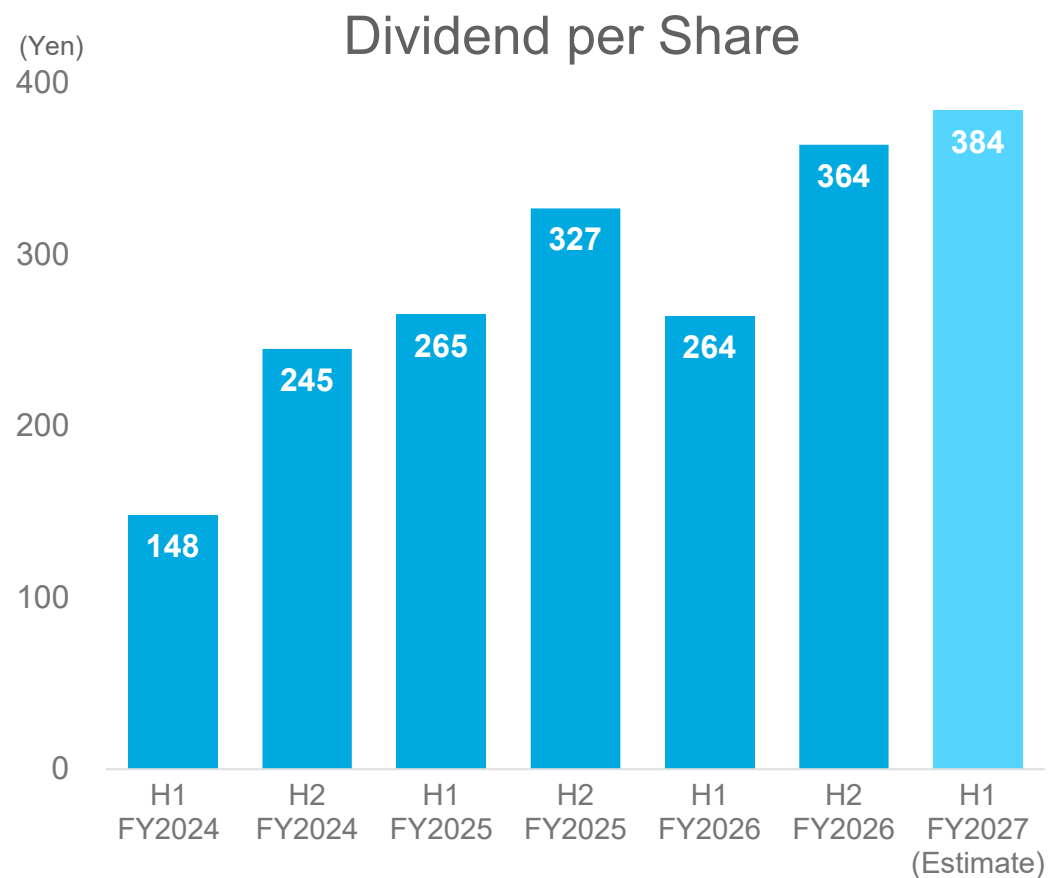
Production Capacity

3x

Continue strengthening competitiveness with a focus on R&D investment
Leveraging this solid infrastructure to steadily capture future gains

Source: TEL

Dividend Forecast



TEL shareholder return policy

Dividend payout ratio: 50%

Annual DPS of not less than 50 yen

We will review our dividend policy if the company does not generate net income for two consecutive fiscal years

We will flexibly consider share buybacks

Dividend per share for H1 FY2027 (interim dividend) is updated to 384 yen

Status of Share Repurchase

- As of June 30, 2026

- Total number of shares acquired 207,100 shares
- Total cost of acquisition 11,474,246,000 yen

Reference

- As of July 31, 2026 (Completed)

- Total number of shares acquired 2,443,900 shares
- Total cost of acquisition 149,999,015,000 yen

(Resolutions of the Board of Directors' meeting held on May 29, 2026)

- Type of shares to be acquired Shares of common stock
- Total number of shares to be acquired Up to 7.5 million shares
(Equivalent to 1.6% of outstanding shares excluding treasury stock)
- Total cost of acquisition Up to 150 billion yen
- Period of acquisition From June 1, 2026 to March 31, 2027

Stock Split

■ Purpose	By implementing the stock split to lower the minimum investment, we intend to make shares more affordable for investors, with a view to expanding the investor base
■ Split Method	Each share of common stock owned by shareholders listed or recorded in the closing register of shareholders on the record date of Wednesday, September 30, 2026, will be split into 5 shares
■ Schedule	Date of public notice of record date: September 15, 2026 (Tuesday) Record date: September 30, 2026 (Wednesday) Effective date: October 1, 2026 (Thursday)
■ Dividends	As the effective date of the stock split is October 1, 2026, the interim dividends for the fiscal year ending March 2027, to all shareholders with a record date of September 30, 2026, will be implemented based on the number of shares issued prior to the stock split

Introducing Our New Organizational Structure

■ Corporate Officers

Toshiki Kawai^{*1}
President & CEO

Shinichi Hayashi^{*1 *2}
Development and Production

Shingo Tada ^{*2}
Customer Strategy, Global Customer Engineering

Kazuhiro Doh ^{*2}
Corporate Strategy & Planning

Hiroshi Ishida^{*1}
Senior Executive Vice President & COO

Keiichi Akiyama
Product Business

Tatsuya Aso^{*2}
Global Business Platform

^{*1} Concurrently serves as TEL Corporate Director

^{*2} New Representative

■ CxO under the New Organization (Highlights)

Toshiki Kawai,
CEO



Hiroshi Ishida,
COO



Hiroshi Kawamoto,
CFO



TEL will clearly define a person in charge of execution for each function and business domain
to enhance velocity and effectiveness of management execution

Source: TEL

5. Sustainability

Sustainability Initiatives

The 14 material issues (key issues) that require prioritized attention and actions are identified to implement sustainability initiatives through our business operation and contribute to the resolution of industrial and social issues.



Source: TEL

Risk Management System and Implementation

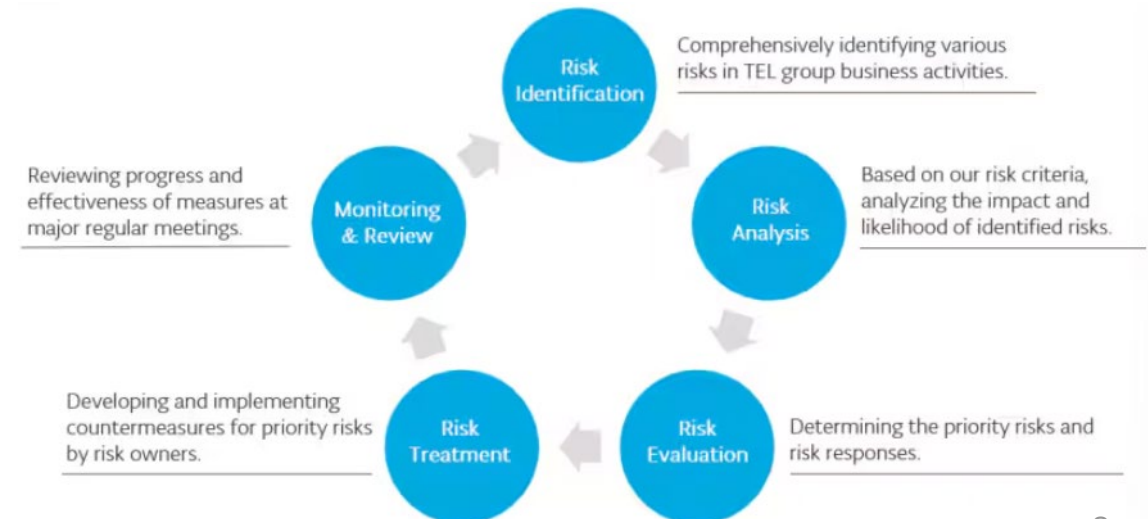
System

- Established the Corporate Project & Risk Management Office in the Corporate Planning Division at the head office to promote more effective risk management in the Group as a whole, while actively working toward advancing enterprise risk management^{*1}
- The Group's risk management activities are regularly reported to the Board of Directors, which oversees various initiatives implemented by each risk owner
- To raise awareness of risk management and provide basic knowledge, we regularly conduct web-based training on risk management for our Group employees and training programs for managers.

Implementation of the PDCA cycle

To address major risks^{*2} in our business activities, we have implemented the following PDCA cycle throughout the entire Group.

By reviewing and revising the major risks, we push risk management initiatives forward for each identified risk even further.



^{*1} Enterprise risk management: Group-wide systems and processes related to risk management activities

^{*2} Major risks: For details on identifying risk items and each risk item, please refer to the "Risk Management" section of our website <https://www.tel.com/sustainability/management-foundation/risk-management/index.html>

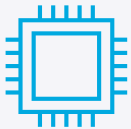
Environmental Approaches in the Supply Chain

E-COMPASS

Environmental Co-Creation by Material, Process and Subcomponent Solutions

Semiconductors

Pursuing higher device performance and lower power consumption



Products

Achieving both high process performance and environmental performance of the equipment



Business activities

Reduction of CO₂ emissions in all business activities

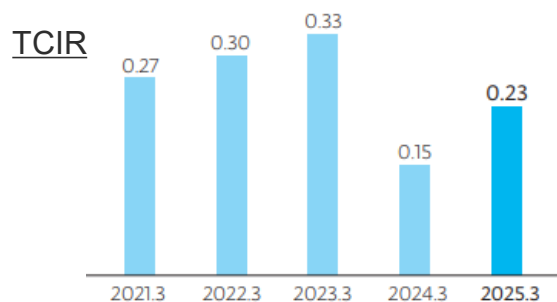


Promoting technological innovation of semiconductors and reducing environmental impact throughout the supply chain

Safety & Quality

Safety

Under the “Safety First” slogan, everyone at Tokyo Electron, from top management to field representative, is actively and continuously improving safety and promoting health, giving safety and health the highest priority when carrying out different types of operations such as development, manufacturing, transportation, installation and maintenance.



Safety Goals
(by FY2027)
TCIR ≤ 0.1

In fiscal 2025, through enhancement of safety training and continuous efforts toward safe design of equipment, we achieved a TCIR of 0.23, an industry-leading position in the semiconductor production equipment industry.

TCIR: Total Case Incident Rate (Number of workplace injuries per 200,000 work hours)

Incident Prevention Initiatives

- Experiential training and VR (Virtual Reality)
- Comprehensive safety inspections
- Feedback on safety specifications
- Safety activities for suppliers



Source: TEL

Quality

The Tokyo Electron Group seeks to provide the highest-quality products and services. This pursuit of quality begins at development and continues through all manufacturing, installation, maintenance, sales and support processes. Our employees must work to deliver quality products, quality services and innovative solutions that enable customer success.

Quality Policy

1 Quality Focus

2 Quality Design and Assurance

3 Quality and Trust

4 Continual Improvement

5 Stakeholder Communication

TEL Values as codes of conduct



Engagement



Career



Corporate growth is enabled by **people**, and our employees both create and fulfill company values

Retention



Work-life balance



Diversity, Equity and Inclusion



3G
Global • Generation • Gender

Human Rights Initiatives

The five focus areas in human rights (Tokyo Electron Group Human Rights Policy)

Freedom, equality & non-discrimination

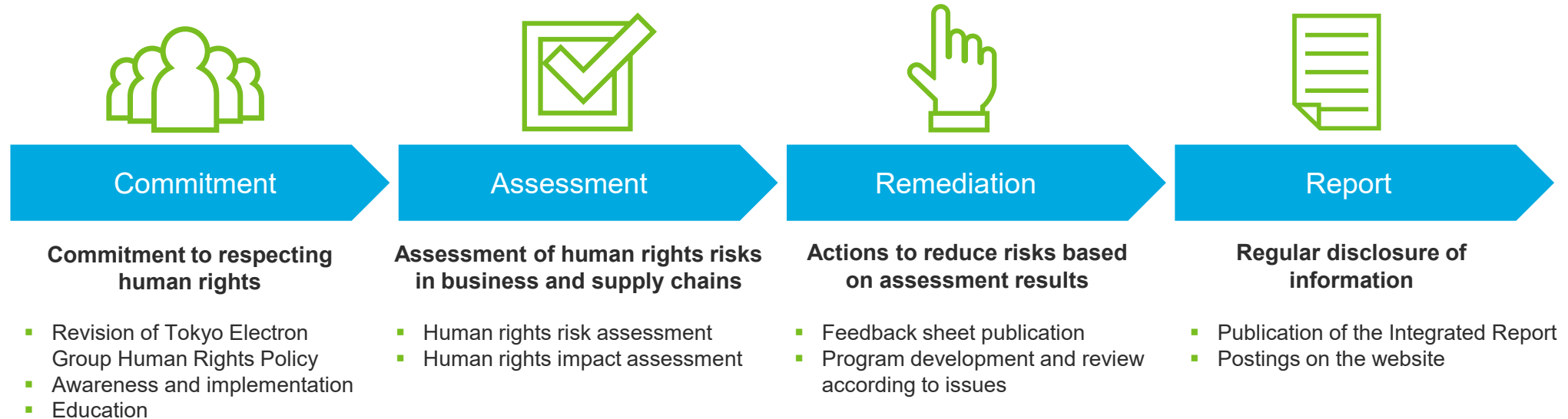
Freely chosen employment

Product safety & workplace health and safety

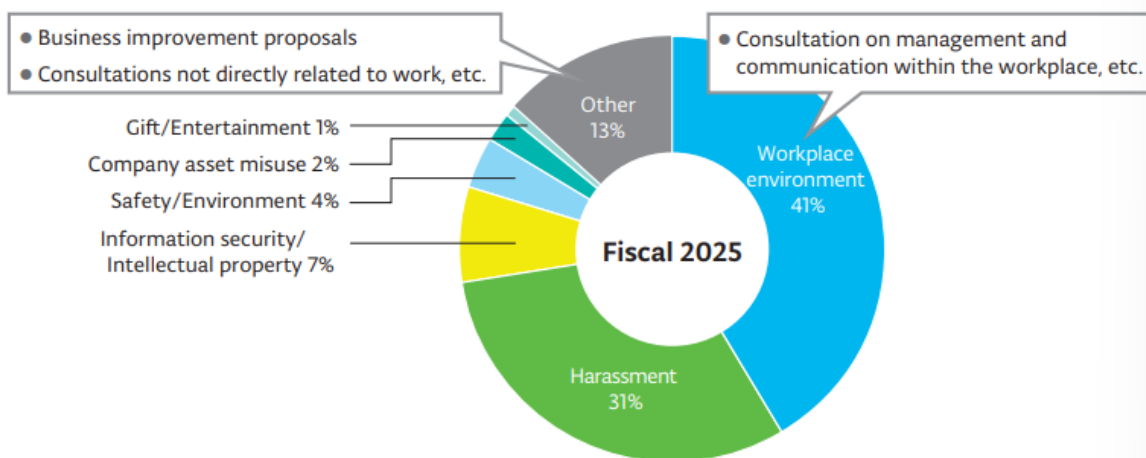
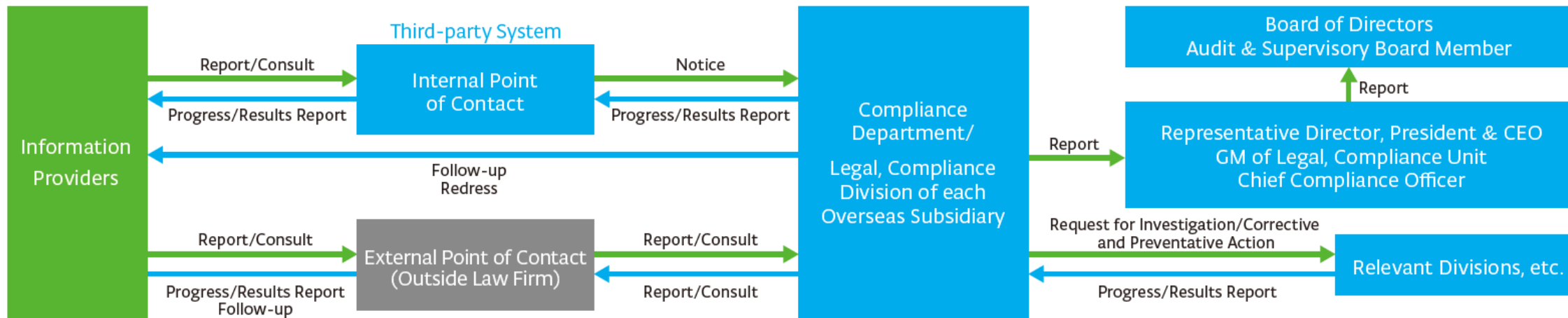
Freedom of association

Appropriate working hours & breaks/ holidays/vacations

Human Rights Due Diligence



Internal Reporting System

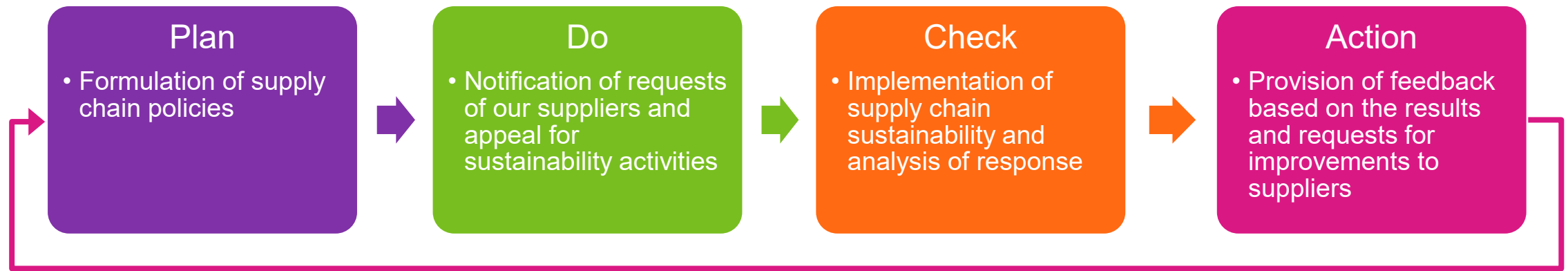


* Percentages may not add up to 100 because they have been rounded.

Respect for human rights with a strong sense of integrity

Supply Chain Management

Supply chain sustainability process

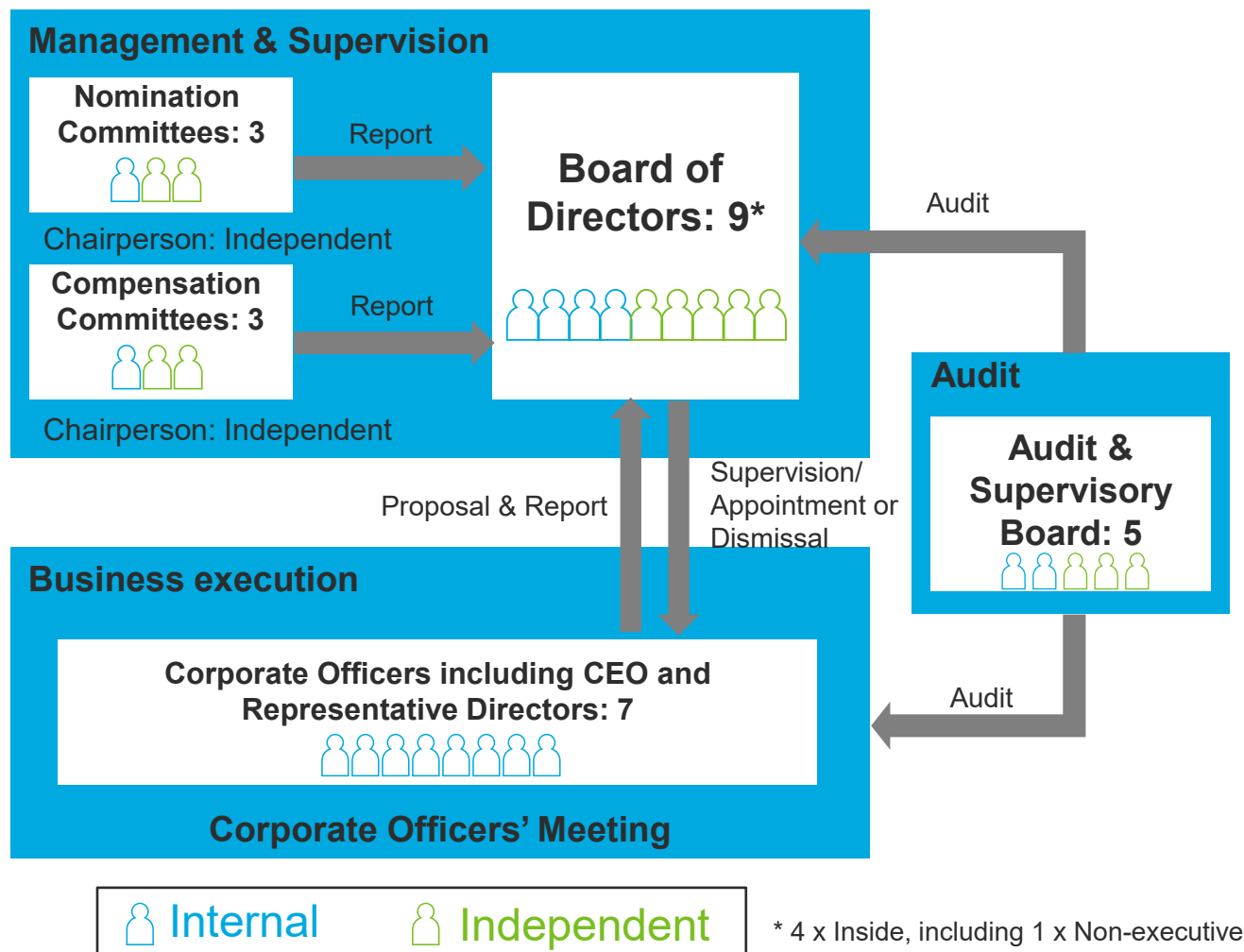


- Annual Sustainability Assessment
 - Assessment base on RBA code of conduct
 - Corrective Action Plans
- RBA Audit
 - At primary manufacturing sites
 - Continuous improvement in respective operations

Pursuit of sustainability conscious operations throughout the supply chain

Corporate Governance Framework (Audit & Supervisory Board System)

<Framework (Excerpt)>



Evaluation of the Effectiveness of the Board of Directors



Internal and external experts analyze and evaluate the effectiveness of the Board of Directors

Global Initiatives

Sustainable Development Goals (SDGs)

Clarify initiatives through business by materiality and deploy company-wide



Source: United Nations Information Centre (<https://www.unic.or.jp/>)

Tokyo Electron supports the SDGs

Participation in International Initiatives

Signed the UN Global Compact, joined the Responsible Business Alliance (RBA), endorsed the Task Force on Climate-related Financial Disclosures (TCFD)



External Evaluation on our ESG Initiatives

Highly rated by evaluation organizations around the world

Dow Jones Best-in-Class Asia Pacific Index

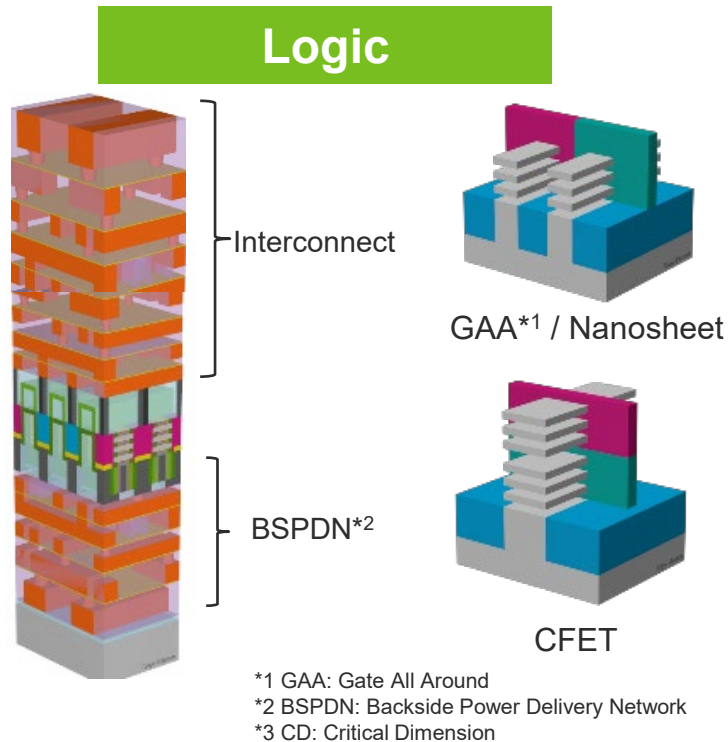


The inclusion of Tokyo Electron Limited in any MSCI Index, and the use of MSCI logos, trademarks, service marks or Index names herein, do not constitute a sponsorship, endorsement or promotion of Tokyo Electron Limited by MSCI or any of its affiliates. The MSCI Indexes are the exclusive property of MSCI. MSCI and the MSCI Index names and logos are trademarks or service marks of MSCI or its affiliates.

6. Diversifying Semiconductor Technology

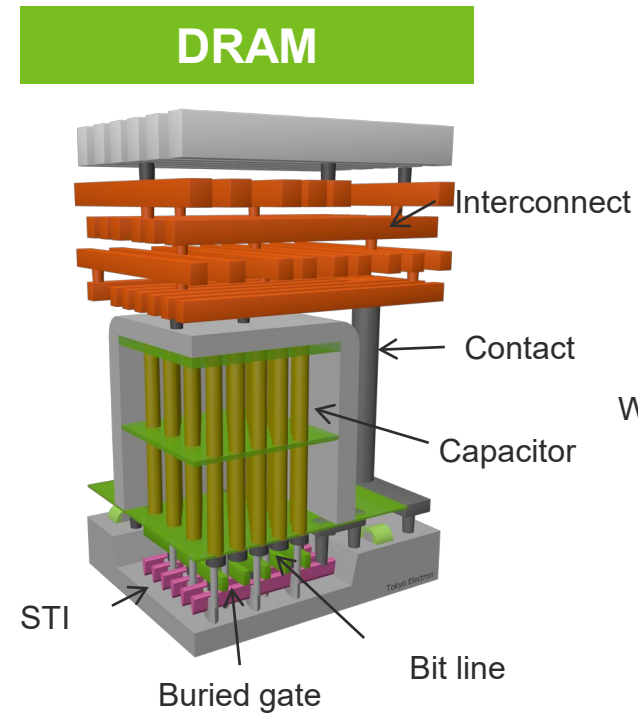
~ Technology Roadmap~

Semiconductor Devices: Direction of Development



Through miniaturization with structural changes

- Lowered cost per transistor
- Lower power consumption
- Higher speed

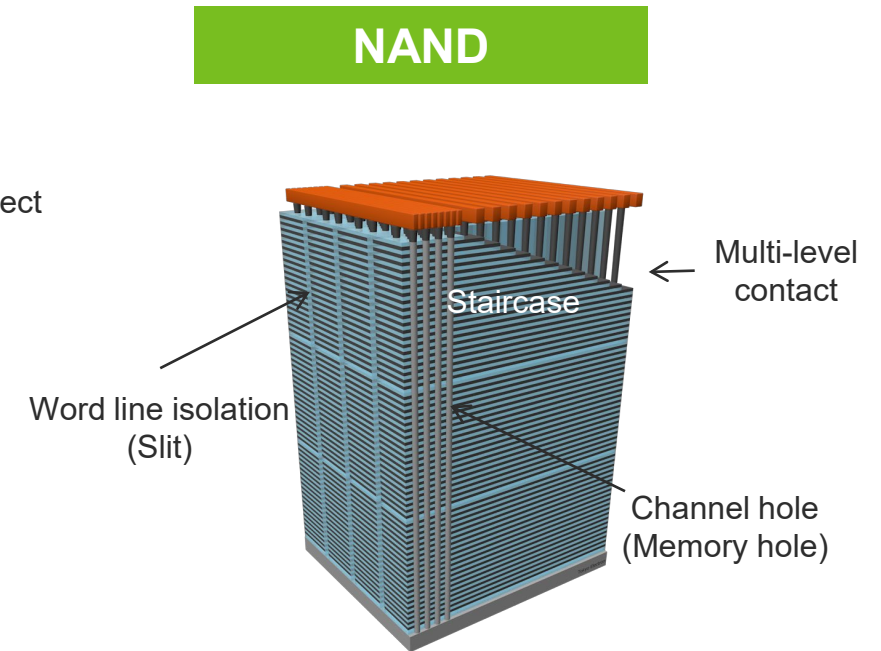


Through miniaturization

- Lower cost per bit
- Lower power consumption
- Higher speed

Through new structures

- Lower cost per bit

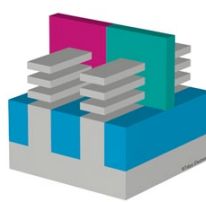
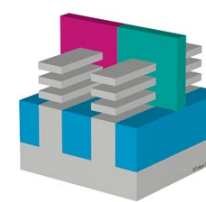
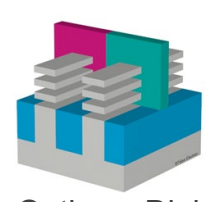
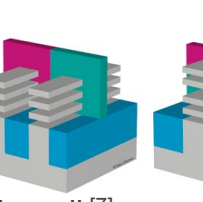
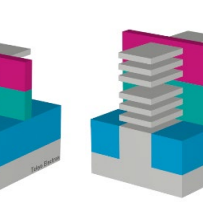
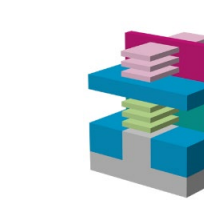
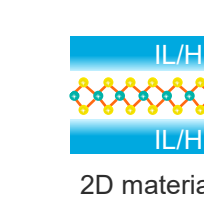


Through high stacking

- Lower cost per bit

[1] Chih-Hao Chang (TSMC) et al., IEDM 2022
 [2] Shien-Yang Wu (TSMC) et al., IEDM 2022
 [3] Geoffrey Yeap (TSMC) et al., IEDM 2024
 [4] Kevin Fischer (intel) et al., Symp. VLSI 2025
 [5] Geoffrey Yeap (TSMC) et al., Symp. VLSI 2026
 [6] Sandy Liao (TSMC) et al., IEDM 2024
 [7] Mertens and Horiguchi (imec), EDTM 2024

Source: TEL estimates

Year of HVM (20k/month)	2022~24	2025~2027	2028~29	2030~31	2032~33	2034~35	2036~37	2038~39	
Node	3nm	2nm/18A/16A	14A/12A	10A	7A	5A	3A	2A	
Transistor	2~1 Fin	GAA NS	GAA NS scaling	GAA NS extension	NS or CFET		CFET	CFET extension	2D material stack
									
	Options: Dielectric wall [7]								2D material: TMDC MoS ₂ , WS ₂ , MoSe ₂ , WSe ₂ etc.
Poly Pitch [nm]	48~45 [1]		45~42		48 [6] ~39		45~39		36
Min. Metal Pitch [nm]	23 [2]		20	18	18~16		16	14	12
Interconnect booster	Cu Barrier/Seed CIP Backside PDN (HPC) [4,5]			Cu CIP or Ru subtractive	Ru subtractive AR>3, Airgap		New alloy AR>5, Airgap, BEOL Transistor (OS*5, 2D material)		
EUV Patterning Technology	EUV MP*1, SE*2		EUV MP, SE High-NA SE			High-NA MP, SE EUV MP, SE			
Resist	CAR*3			CAR (+MOR*4)		CAR+MOR			

*1 MP: Multi-Patterning, *2 SE: Single-Exposure, *3 CAR: Chemically Amplified Resist, *4 MOR: Metal Oxide Resist, *5 OS: Oxide Semiconductor

Logic scaling will continue by changing transistor structure and material evolution

DRAM Technology Roadmap (Generic)

[1]Seokhan Park (Samsung) et al., IEDM 2023

[2]Daewon Ha (Samsung) et al., IEDM 2023

[3]Joodong Park (SK hynix) et al., VLSI 2025

[4]Kiseok Lee (Samsung) et al., VLSI 2024

[5]Dwaipayan Biswas (imec) IMW26

[6]Daewon Ha (Samsung) et al., VLSI 2023

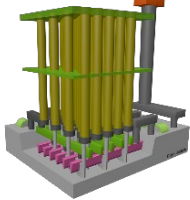
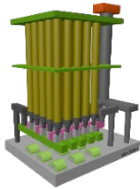
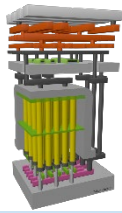
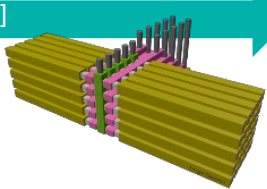
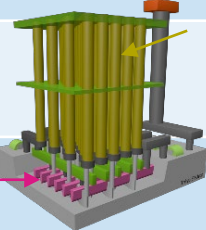
[7]Joodong Park(SK hynix) et al., VLSI 2024

[8]Van Tuong Pham et al., SPIE2026

[9]Alexander C. Marwitz et al., SPIE2026

[10]Shinichiro Kawakami (TEL Kyushu Ltd.) et al., SPIE 2022

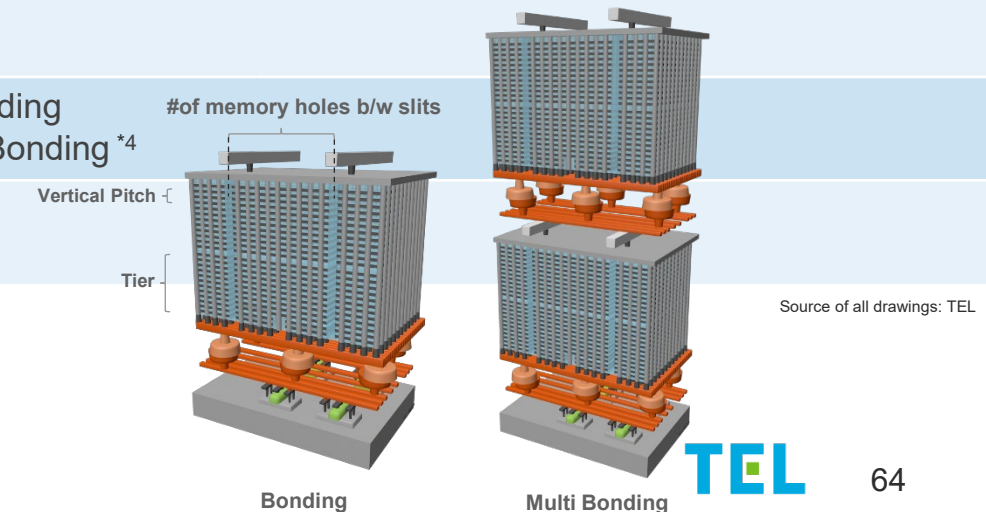
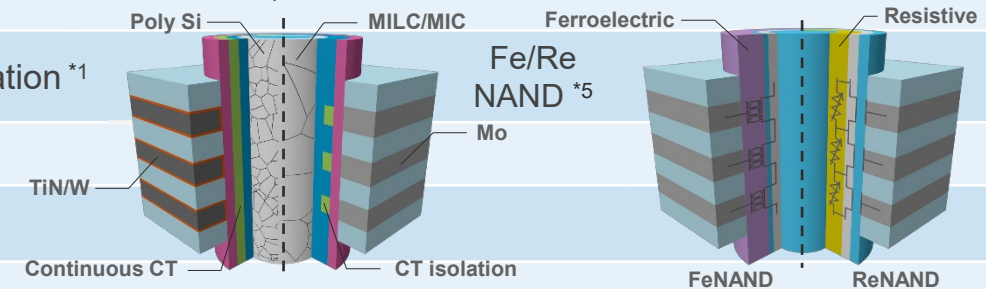
Source: TEL estimates

Year of HVM (20k/month)	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036
Node	1c		1d	0a		0b	0c		0d	0e		
Cell layout / Structure	6F²  4F² VCT  4F² VCT^[1,2,3] or 6F² + Peri Bonding^[4,5]  3D DRAM^[6,7] 											
F [nm]	12~11		10	(6F ²) (VCT)	9 15	8 13.5	12		(3D ~1xxL)		(3D >1yyL)	
Capacitor pitch [nm]	36~33		30	(6F ²) (VCT)	27 30	24 27	24		Aspect ratio 			
Capacitor aspect ratio	40		>40	>40		>40	>50		Word line 			
EUV Patterning	EUV MP,SE				EUV MP, SE, / hNA in R&D ^[8,9]					(No EUV for 3D DRAM)		
Resist	CAR + MOR ^[10]								CAR			
Word line	TiN		Low Rs metal						w/ Bonding			
Peri. CMOS	Gate First HKMG					Gate last Planer MOS or FinFET						
HBM	HBM4	HBM4E	HBM5	HBM5E	HBM6	HBM6E	HBM7	HBM7E				

NAND Technology Roadmap (Generic)

Source: TEL estimates

Year of HVM (20k/month)	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036
Stack (~1.3x/1.5years)	3xxL	4xxL	5xxL	6xxL	8xxL	*1xxxL	*1yyyL	*1zzzL				
Tier	2 or 3	3	3 or 4	3 or 4	4 - 6							
Min vertical pitch	40 nm	39 nm	38 nm	37 nm	36 nm					~ 30 nm		
Max memory height	14 μm	19 μm	25 μm				40 μm	> 60 μm				
Charge trap (CT)	Continuous CT						CT isolation *1					
Channel	Poly Si grain CIP			MILC *2/MIC *3								
WL metal	W or Mo			Mo								
WL contact	Stair or Stairless				Stairless							
Layout/Structure	Under array or Bonding	Bonding					Bonding or Multi Bonding *4					
Peri. CMOS	Poly Si Gate			HKMG								

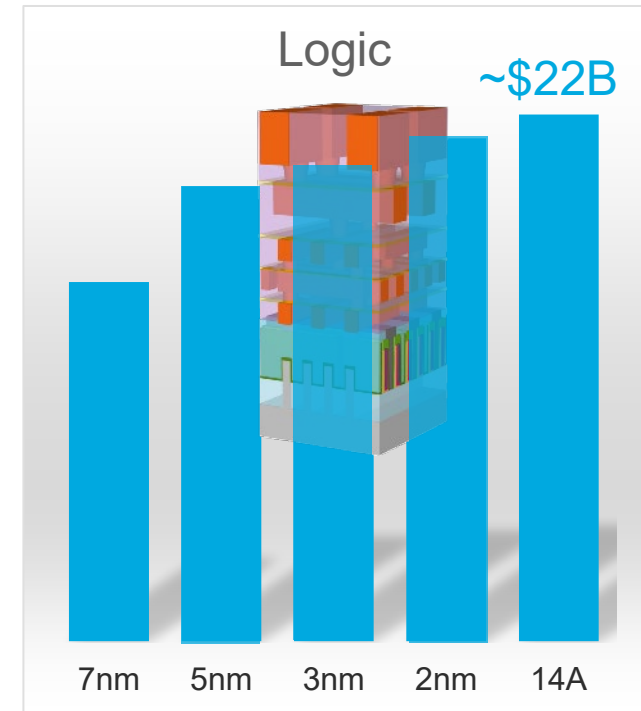
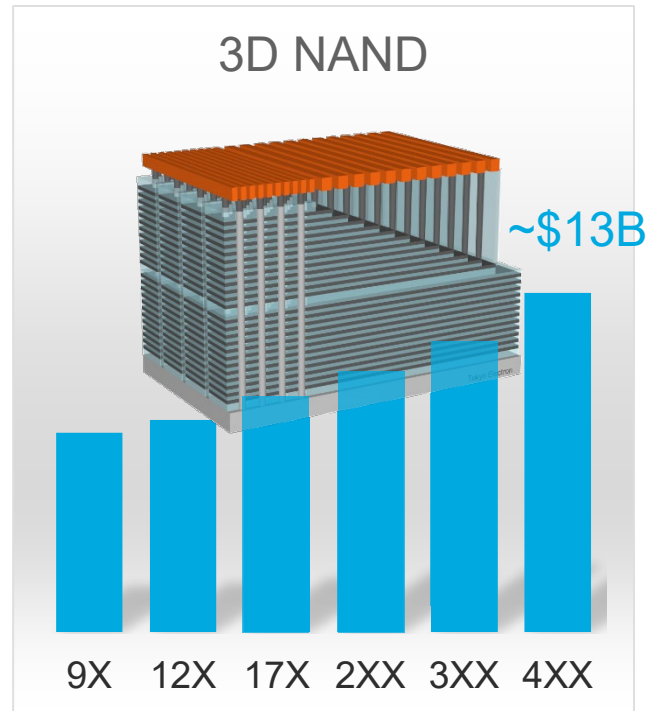
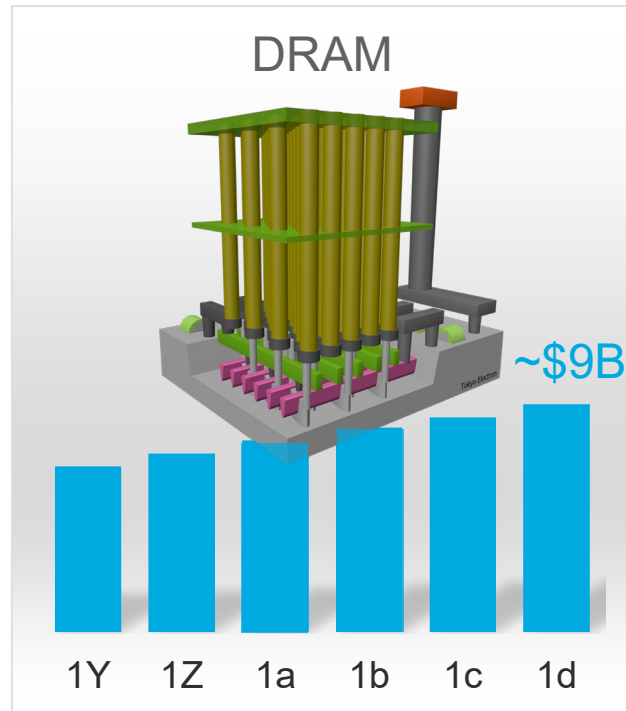


Source of all drawings: TEL

* Trend Extrapolation
¹ Sang-wan Jin (SK hynix) et al., IEDM 2025
² Metal Induced Lateral Crystallization
³ Metal Induced Crystallization
⁴ Mitsuhiro Noda (KIOXIA) et al., VLSI 2026
⁵ Jecheon Han (Samsung) et al., IEDM 2023

Raising Added-value in SPE

WFE investment (100k WSPM*, Greenfield/TEL estimates)

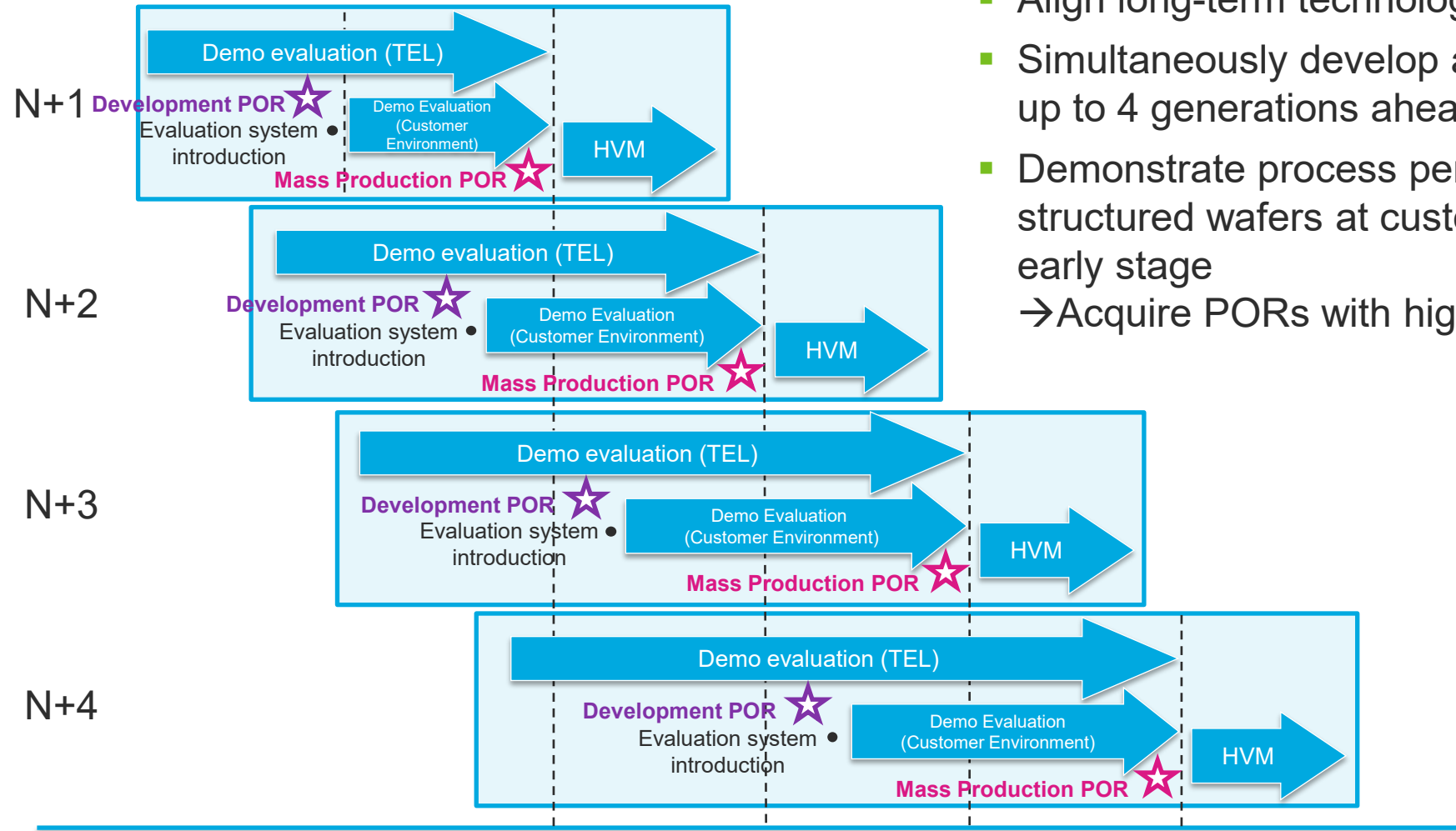


Expanding business opportunities for SPE manufacturers on arrival of new applications and rising level of technological difficulty

7. SPE New Equipment Initiatives

Development Efforts

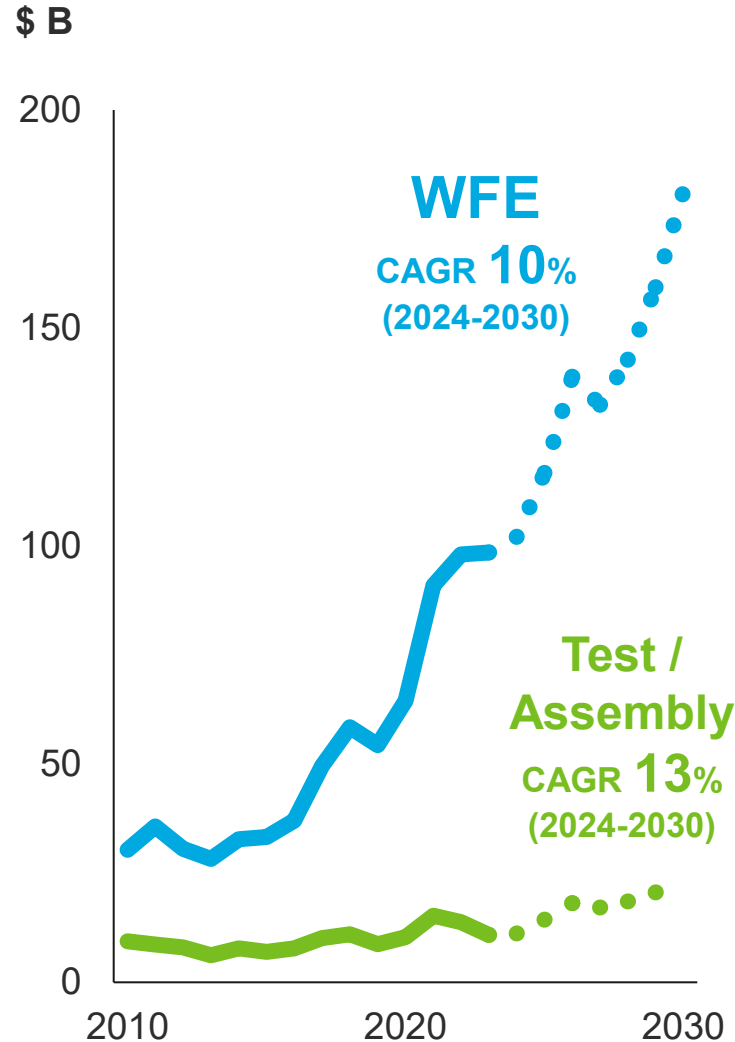
Simultaneous 4-Generation Developments



- Align long-term technology roadmap with customers
- Simultaneously develop and evaluate technologies up to 4 generations ahead
- Demonstrate process performance on customer structured wafers at customer's environments at early stage
→ Acquire PORs with high value-added products

Our Growth Opportunities in the Frontend Market

Presented at IR Day in February 2025



WFE
CAGR 10%
(2024-2030)

**Test /
Assembly**
CAGR 13%
(2024-2030)

- CAGR driven by AI-related devices to continue to drive high growth of WFE's CAGR
- Leveraging TEL's strengths to address high-growth market areas:
 - Leading-edge logic: The etch market is expected to grow by 2.7 times, the deposition market by 2.5 times*
 - DRAM: The etch market is expected to grow by 2.3 times, exceeding the CAGR of WFE*
- By introducing new products focused on the key technological inflection points, we aim to further expand our areas of entry

* TEL Estimates

Source : TechInsights

Growth opportunities at Technological Inflection Points in Frontend Process

■ Logic: GAA^{*1}, BSPDN^{*2}, CFET

- Adaption of High-NA lithography, combined with multi-patterning and MOR technologies, presents opportunities for new technology Acrevia™
- Adoption of multi-patterning to increase demand for deposition, etch, and cleaning processes.
- GAA and CFET transistors to drive an increase in gas chemical etch processes
- New materials like ruthenium and structural innovations such as air gaps to generate fresh opportunities

■ DRAM: HBM, VCT^{*3}, 3D DRAM

- Adoption of multi-patterning driving increased demands in deposition and etch
- Capacitor formation remains essential, driving ongoing demand for advanced etch and deposition
- 3D DRAM leading to increased processes in deposition, etch and gas chemical etch

■ NAND: Beyond 4xx

- Increased layer counts leading to higher investments in deposition and etching processes
- High aspect ratio etch to become increasingly important
- New materials and low-resistance channel silicon to be utilized

^{*1} GAA: Gate All Around

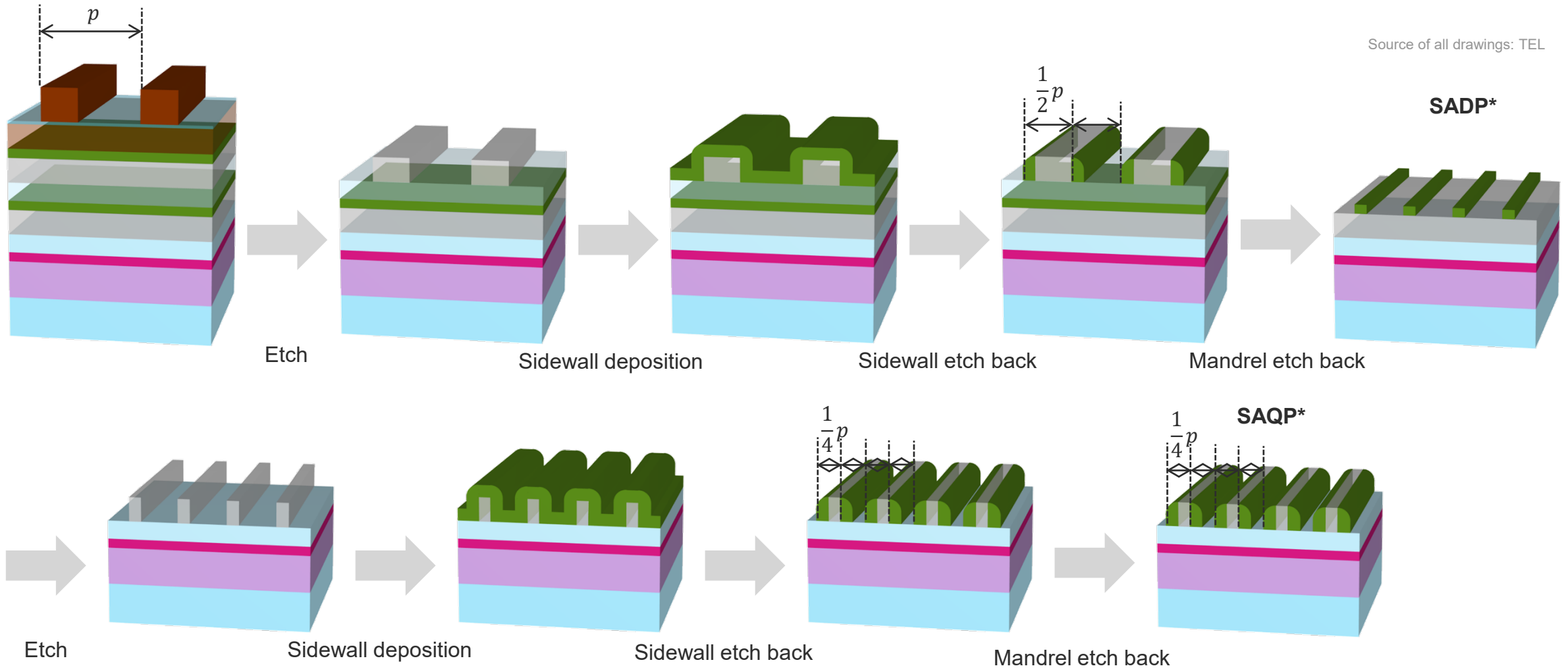
^{*2} Backside PDN: Backside Power Delivery Network

^{*3} VCT: Vertical Channel Transistor

7-1. Frontend, Patterning Technologies

Self-aligned Multiple Patterning to Supplement Lithography

Source of all drawings: TEL

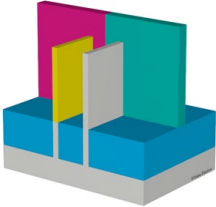
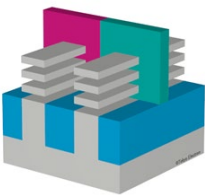
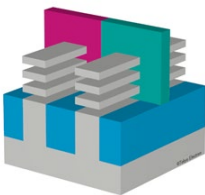
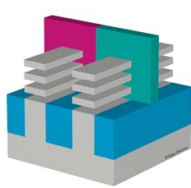
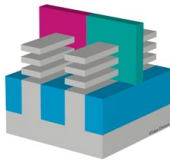
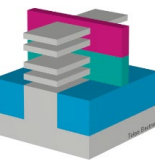
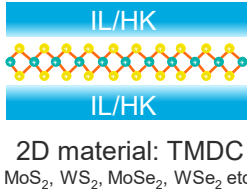


SADP: Self-aligned double patterning
SAQP: Self-aligned quadruple patterning

EUV Lithography Technology Roadmap in Logic

[1] Chih-Hao Chang (TSMC) et al., IEDM 2022
[2] Shien-Yang Wu (TSMC) et al., IEDM 2022
[3] Geoffrey Yeap (TSMC) et al., IEDM 2024
[4] Kevin Fischer (intel) et al., Symp. VLSI 2025
[5] Geoffrey Yeap (TSMC) et al., Symp. VLSI 2026
[6] Sandy Liao (TSMC) et al., IEDM 2024
[7] Mertens and Horiguchi (imec), EDTM 2024

Source: TEL estimates

Year of HVM (20k/month)	2022~24	2025~2027	2028~29	2030~31	2032~33	2034~35	2036~37	2038~39
Node	3nm	2nm/18A/16A	14A/12A	10A	7A	5A	3A	2A
Transistor	2~1 Fin	GAA NS	GAA NS scaling	GAA NS extension	NS or CFET	CFET	CFET extension	2D material stack
								
	Options: Dielectric wall [7]							
Poly Pitch [nm]	48~45 [1]		45~42		48 [6] ~39	45~39		36
Min. Metal Pitch [nm]	23 [2]		20	18	18~16	16	14	12
EUV Patterning Technology	EUV MP*1, SE*2		EUV MP, SE High-NA SE			High-NA MP, SE EUV MP, SE		
Resist	CAR*3			CAR (+MOR*4)		CAR+MOR		

*1 MP: Multi-Patterning, *2 SE: Single-Exposure, *3 CAR: Chemically Amplified Resist, *4 MOR: Metal Oxide Resist

Enhancing versatility of coater/developer to respond to future EUV lithography technologies including MOR and high-NA EUV

Coater/Developer: CLEAN TRACK™ LITHIUS Pro™ Z for EUV

LITHIUS Pro™ Z released in 2012
(> 3000 systems shipped)

New features to support EUV CAR*1/MOR*2
to be released as on an ongoing basis

High Reliability
High share in EUV market

High Productivity
Maximizes output of EUV lithography tools,
and reduces chemical consumption

High Versatility
Supports CAR, MOR and underlayers



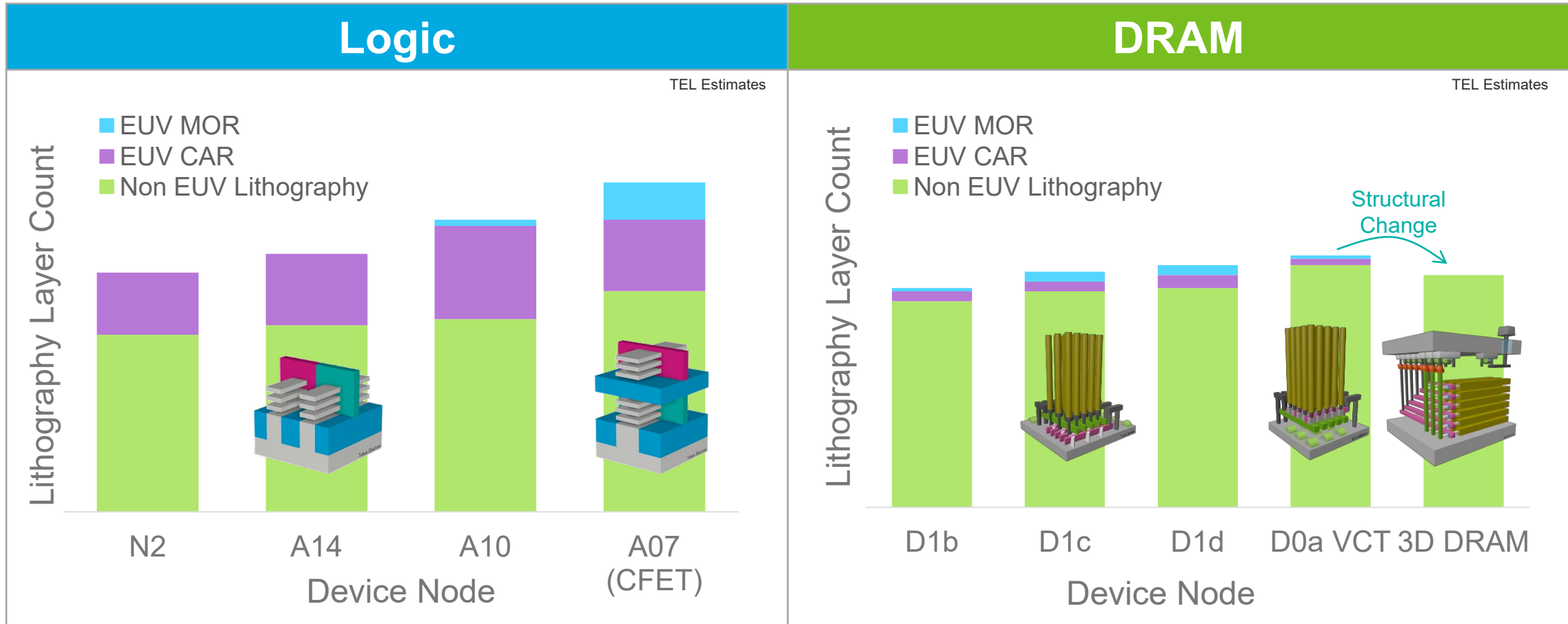
*1 CAR: Chemically Amplified Resist

*2 MOR: Metal Oxide Resist

LITHIUS Pro™ Z platform with its proven mass production for various litho tools, ensures high reliability and productivity for EUV litho, along with high versatility for next-generation EUV

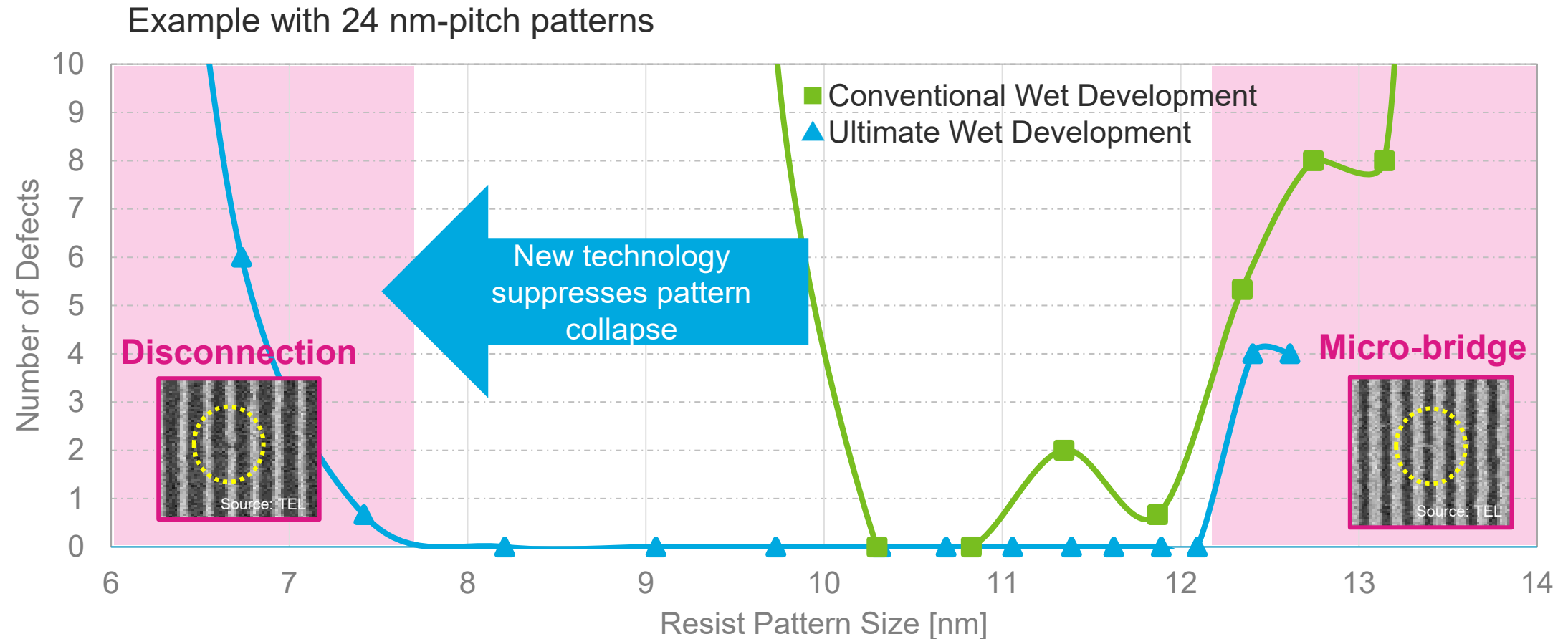
Outlook on Lithography Layer Count

Source of all drawings: TEL



MOR expected for Logic 10A/ DRAM D1b, development ongoing for MOR

Example of MOR Process: The Ultimate Wet Development



The Ultimate Development technology enables the suppression of pattern collapse

Example of MOR Solution: The Ultimate Wet Development

*1 Based on internal information and development targets

*2 Based on results of developing 24 nm-pitch lines

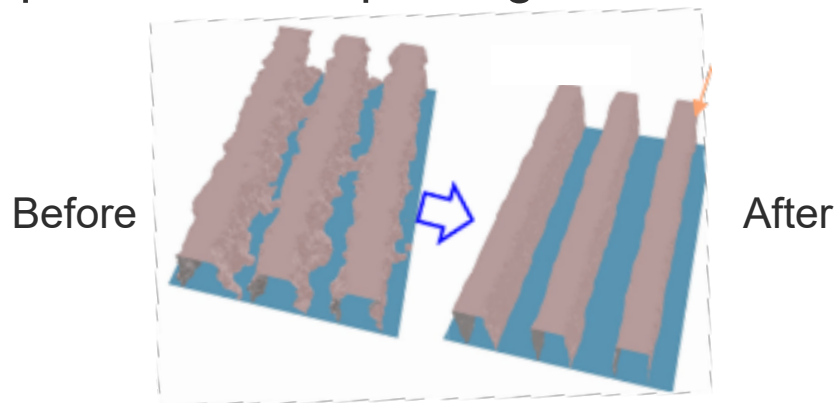
	Ultimate Wet Development Technology	Conventional Wet Technology	Alternative Technology
Base Technology	Coater/Developer	Coater/Developer	Etch
Process Ambient	Atmospheric	Atmospheric	Vacuum
Reaction	Chemicals	Chemicals	Corrosive Gas
Throughput* ¹	4x	4x	1x
Chemical Consumption* ¹	50% (vs. conventional)	100 %	N/A (uses gas) exhaust processed in combustion abatement post process
Anti-Pattern Collapse* ¹ Performance	< 8 nm* ²	> 10 nm* ²	< 8 nm* ¹
Footprint* ¹	In-Line	In-line	Additional Footprint

Evaluation of Ultimate Wet Development ongoing with key customers, with emphasis on productivity (throughput, footprint, maintainability, utilize existing facilities)

Acrevia™

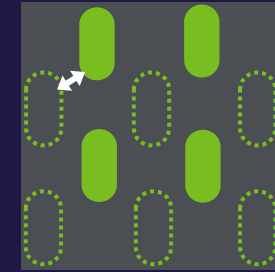
TEL's Original Gas Cluster Beam (GCB) System

- Beam Angle is freely Adjustable
- LSP (Location Specific Processing) Wafer Scan
→ Enable 3 Dimetional Etching
- ✓ Drastically Improve EUV productivity by EUV step reduction with fine patterning
- ✓ Realize yield by removing defect between pattern and improving LER/LWR*

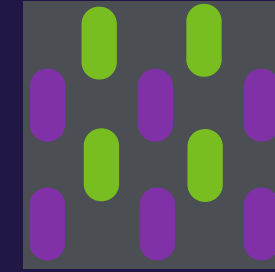
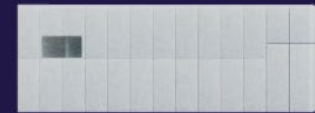


* LER/LWR: Line Edge Roughness / Line Width Roughness

Too Narrow



1st EUV



2nd EUV

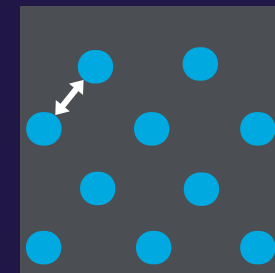
Etch



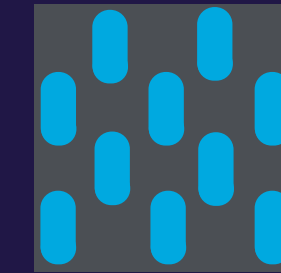
Etch



Wide



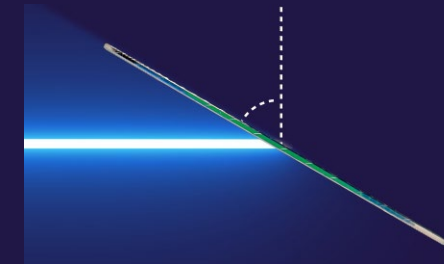
1st EUV



Acrevia™



Etch

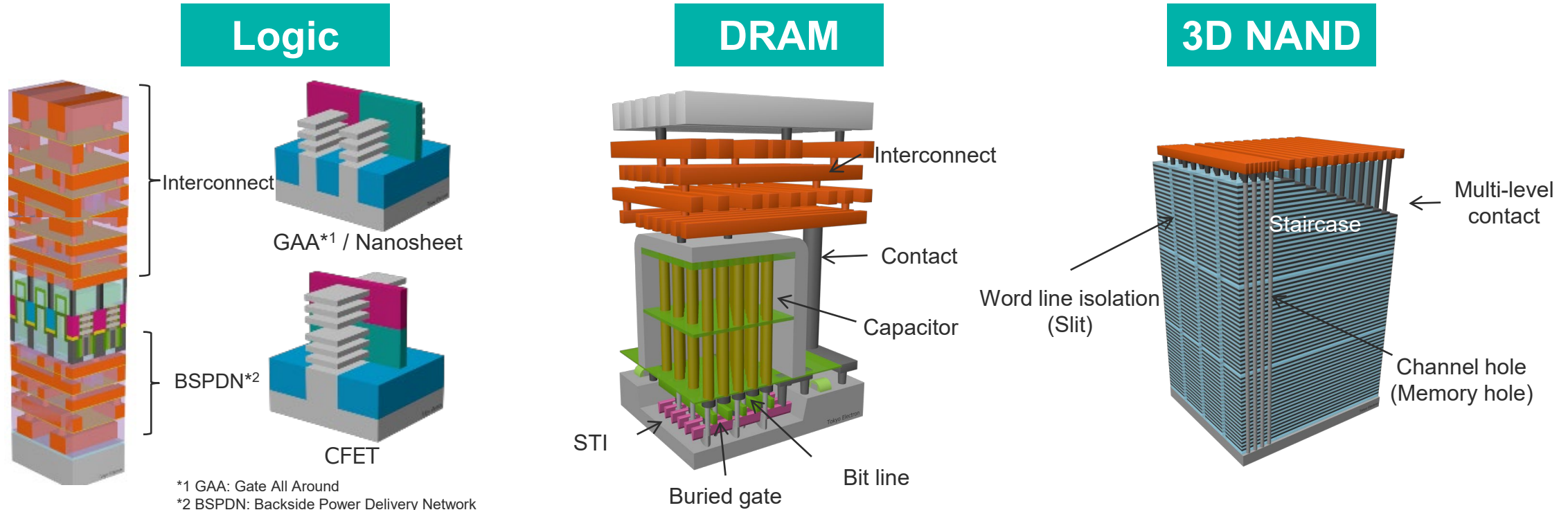


Productivity
2x

7-2. Frontend, Unit Process

7-2-1. Etch System

Requirements and Various Etch Technologies



Device trend

Technology
Required

Scaling/new structure

High selectivity through precise ion control
 Low-damage process
 Profile control (vertical, etc.)

Scaling/new structure

Small CD*³, high aspect ratio capacitor etch
 Scaled mask etch (EUV, multi patterning)
 HBM (increase in interconnect, etc.)

Stacking

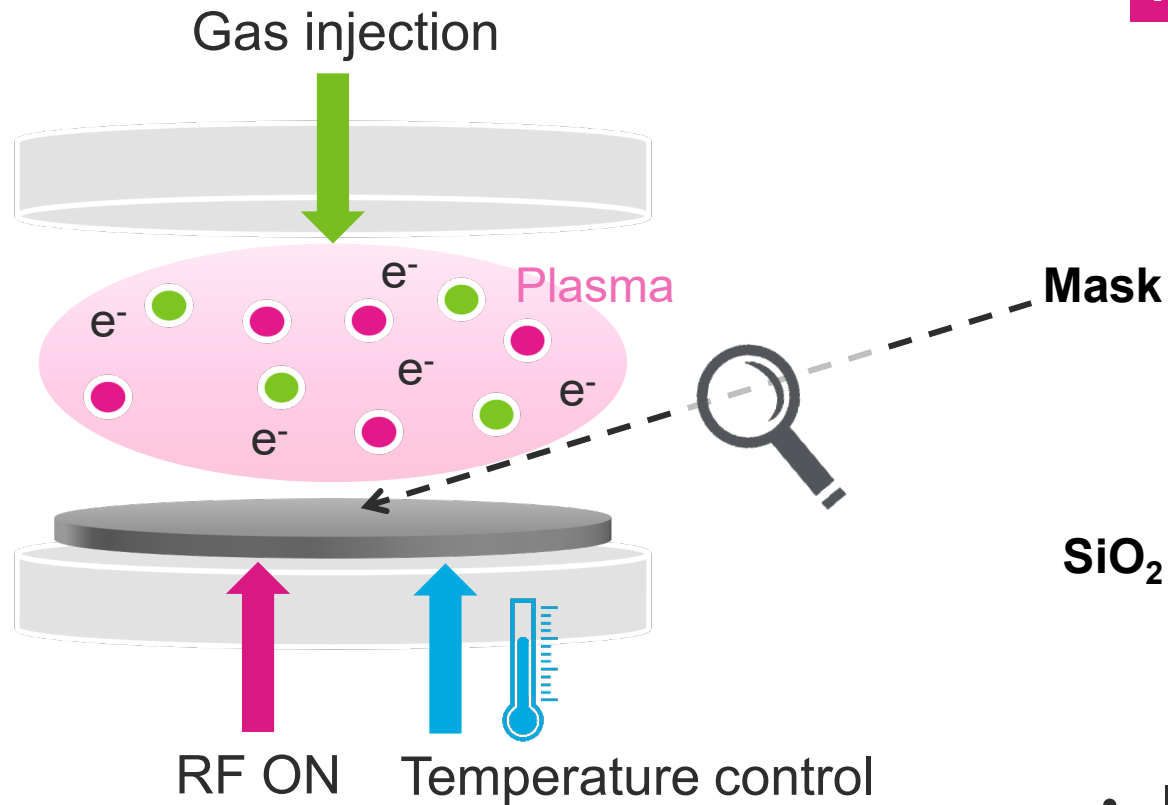
Fast and vertical high aspect ratio etch
 Depth monitoring and process control
 Within wafer uniformity control

Etch technology with precise controllability is required for further evolution of devices

Overview of Etching and Key Parameters

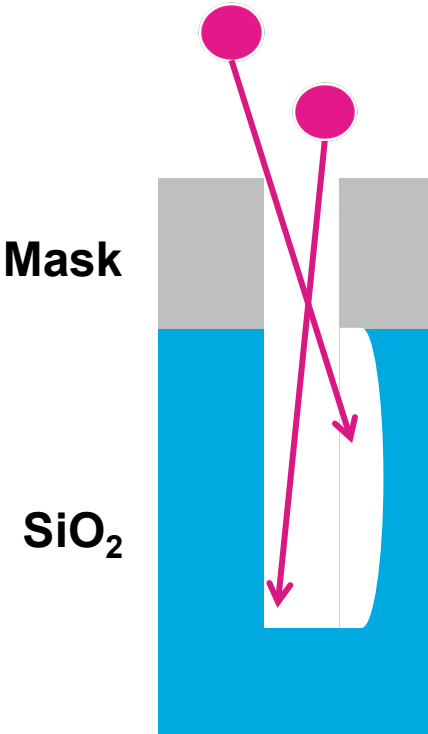
Source of all drawings: TEL

e^- electron ● ion ● radical



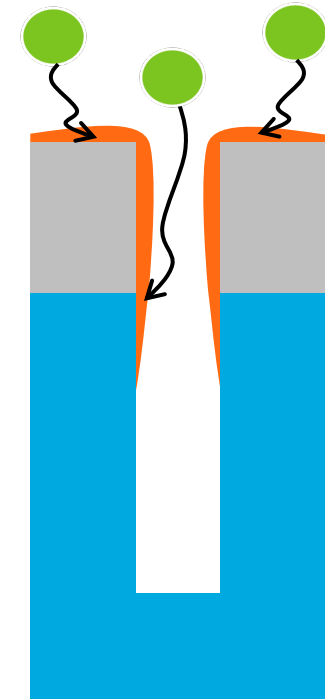
Key Parameters for Etch Controllability

Ion transportation



- Ion energy
- Ion incident angle

Radical transportation

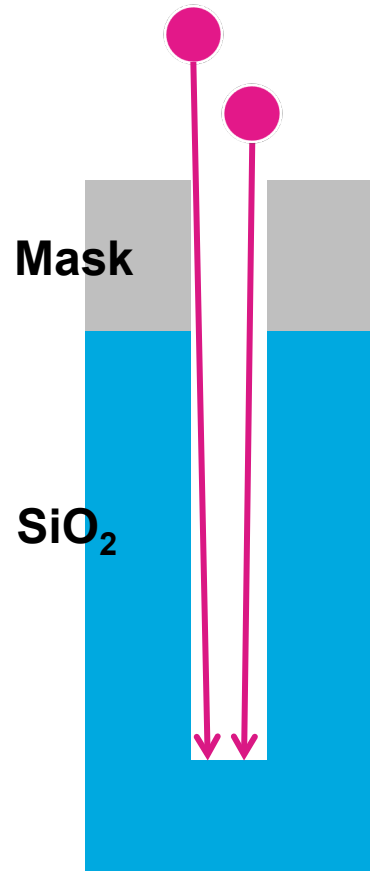


- Gas species
- Wafer temperature

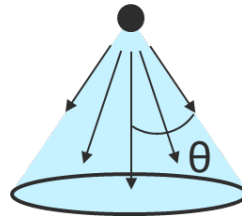
Our Unique Technology 1: HERB™

Source of all drawings: TEL

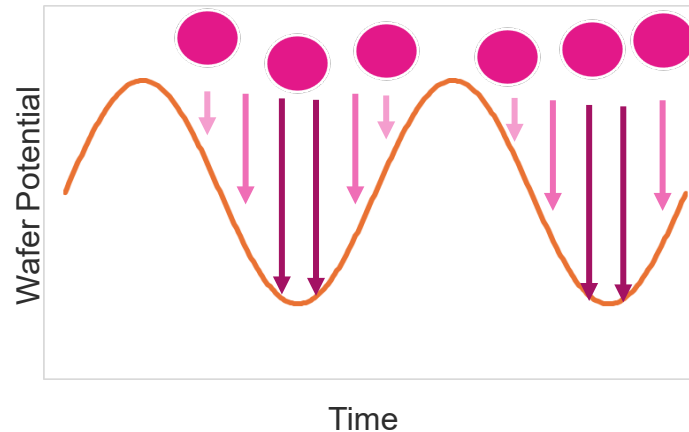
Ion transportation



Conventional Technology (Sine wave)



The force attracting ions varies
→ incident angle varies

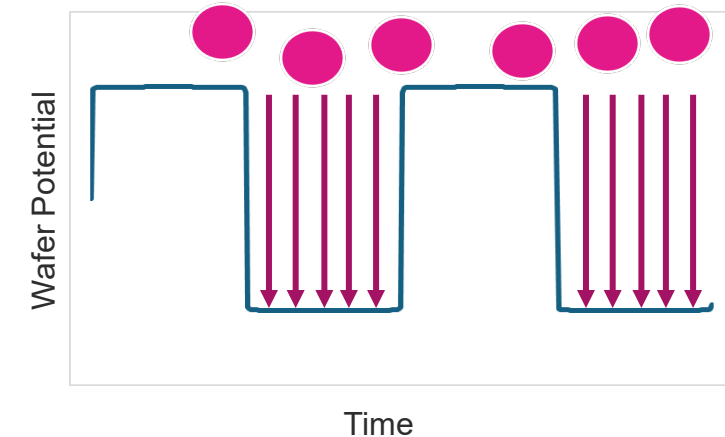


(HERB™: High Efficiency Rectangular Bias™)

Novel Technology (HERB™)



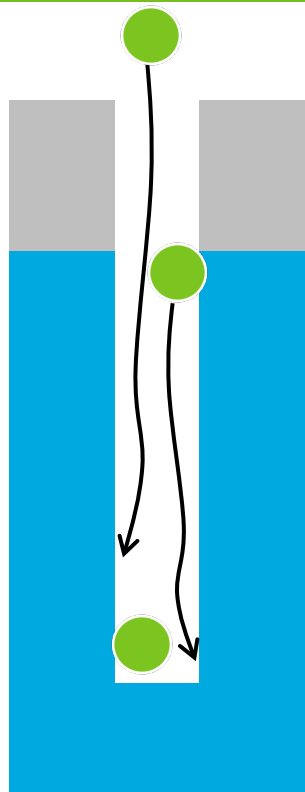
Force attracting ions are strong and consistent
→ incidence angle becomes perpendicular



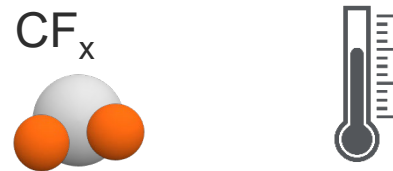
Our Unique Technology 2: PHastIE™

Source of all drawings: TEL

Radical transportation

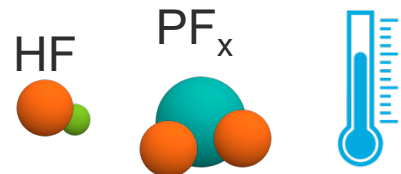


Conventional Technology
(CF_x + room temp.)



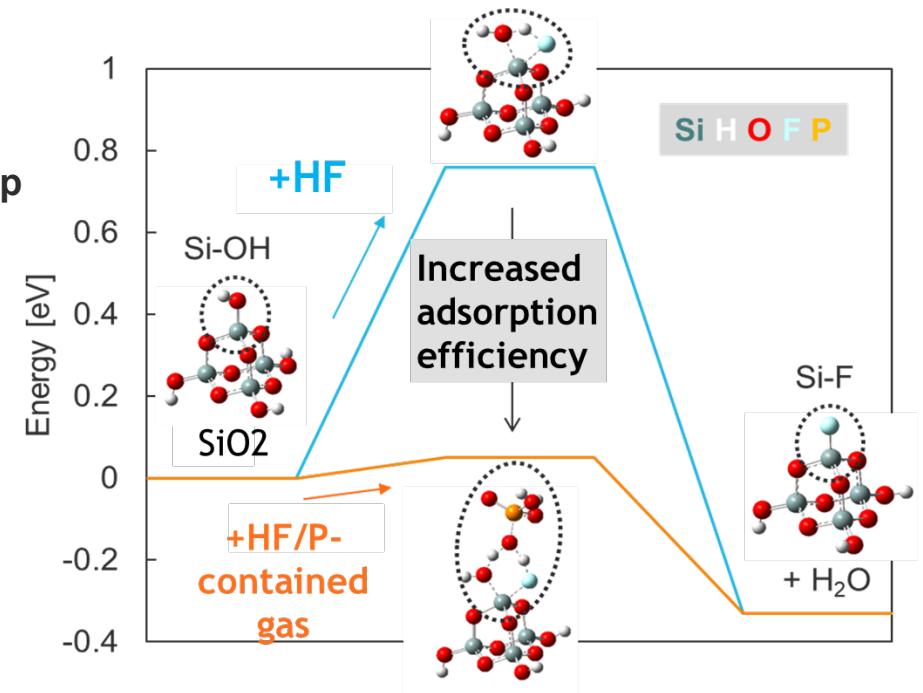
CF_x tends to polymerize/adsorb easily
Hinders transportation when accumulated at top

Novel Technology
(PHastIE™)



Resolved the issue with novel gas
Achieved high etch rate in combination with low temp.

(PHastIE™: Phosphorus + Hydrogen based “Fast” Ion Etch™)



Novel Cryogenic HARC Etch



Beyond



Source: TEL

10 μ m

2.5x

Faster

Process

Cryogenic temp.

More Linear,
Deeper & Faster

Plasma Control

Deep-learning Optimization

Environment

Power Consumption

Less Power

-43%

CO₂e

Less Carbon Footprint

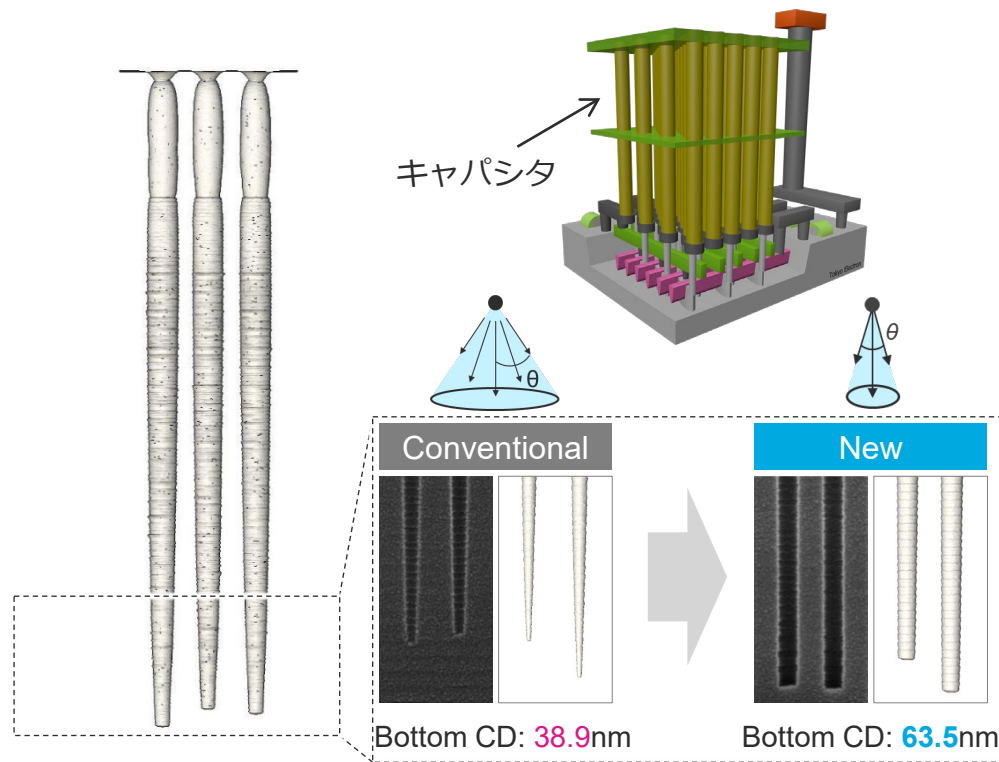
-83%

Presented world's first new cryogenic process in 2023 (@VLSI 2023),
achieving both high process and environmental performance

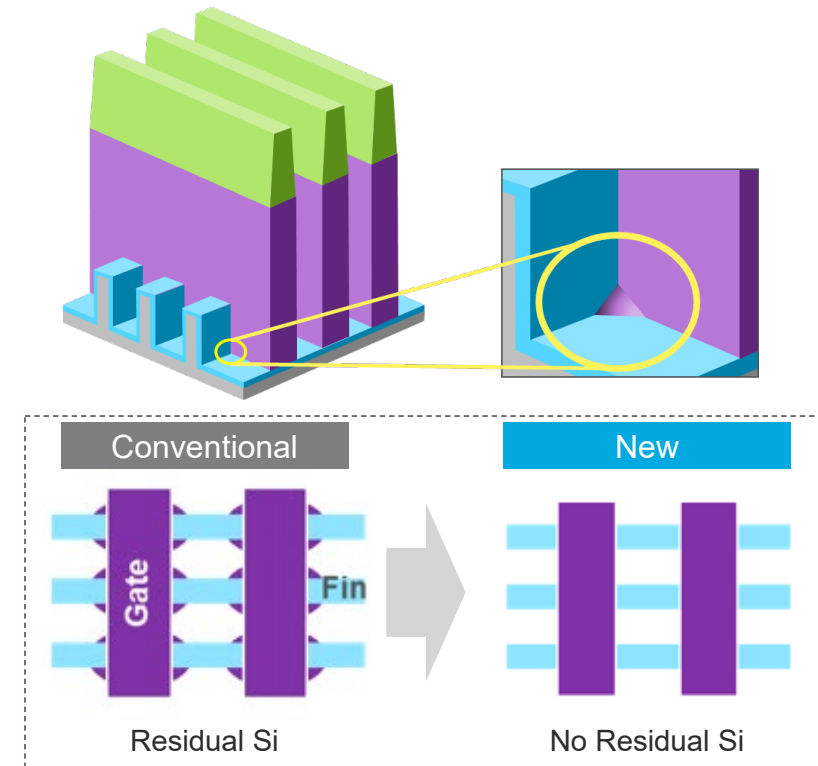
Future of New Etch Technologies

Source of all drawings: TEL

DRAM: Capacitor SiO₂ Etch



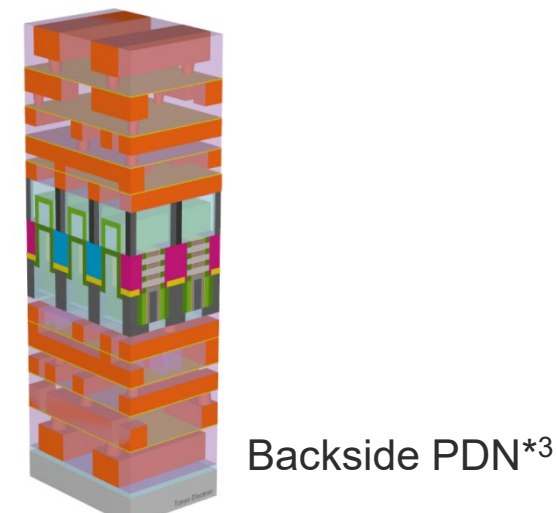
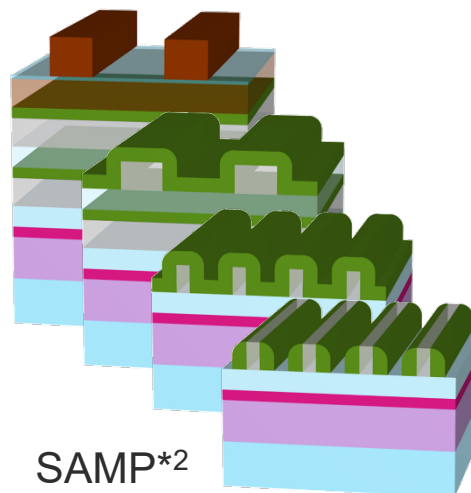
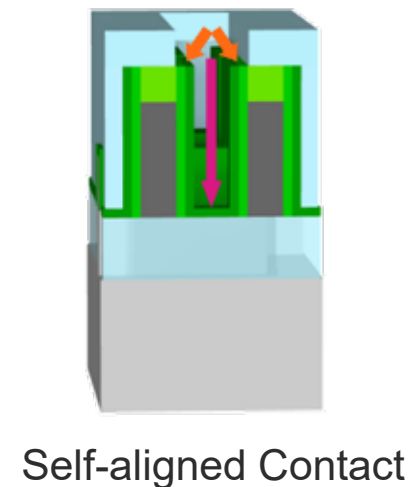
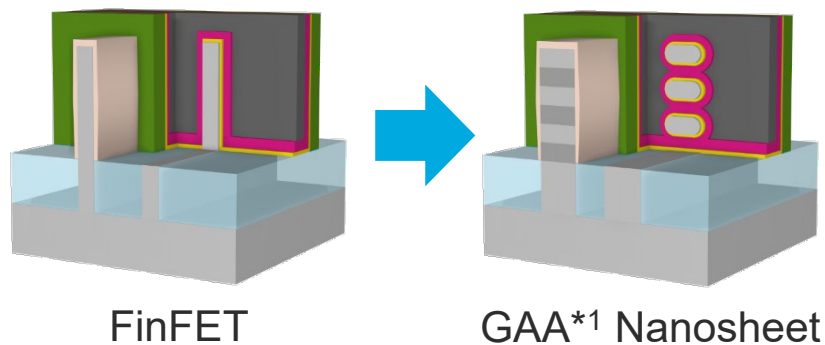
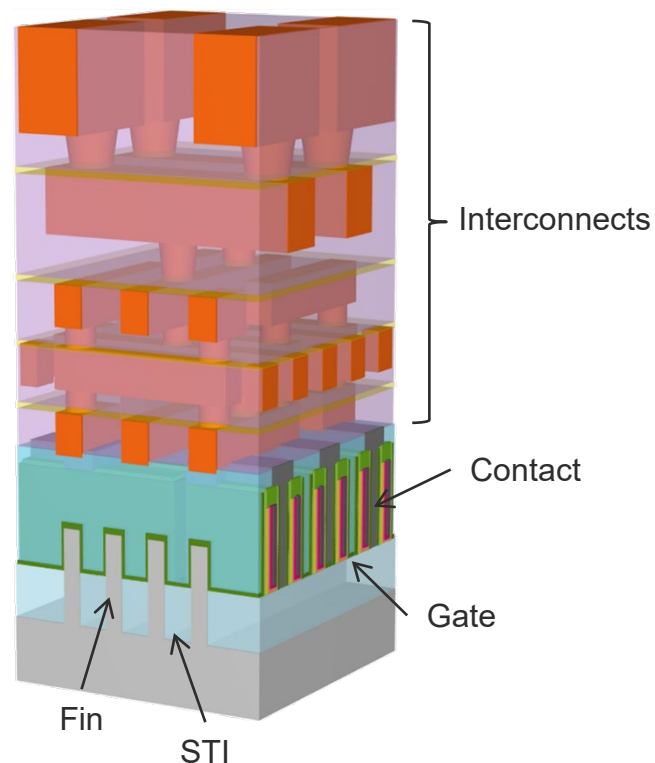
Logic: Gate Silicon Etch



New technologies created through the development of ideal etching process development, will be applied to a variety of critical processes

Business Opportunities in Logic

Source of all drawings: TEL



*1 GAA: Gate all around

*2 SAMP: Self-aligned multiple patterning

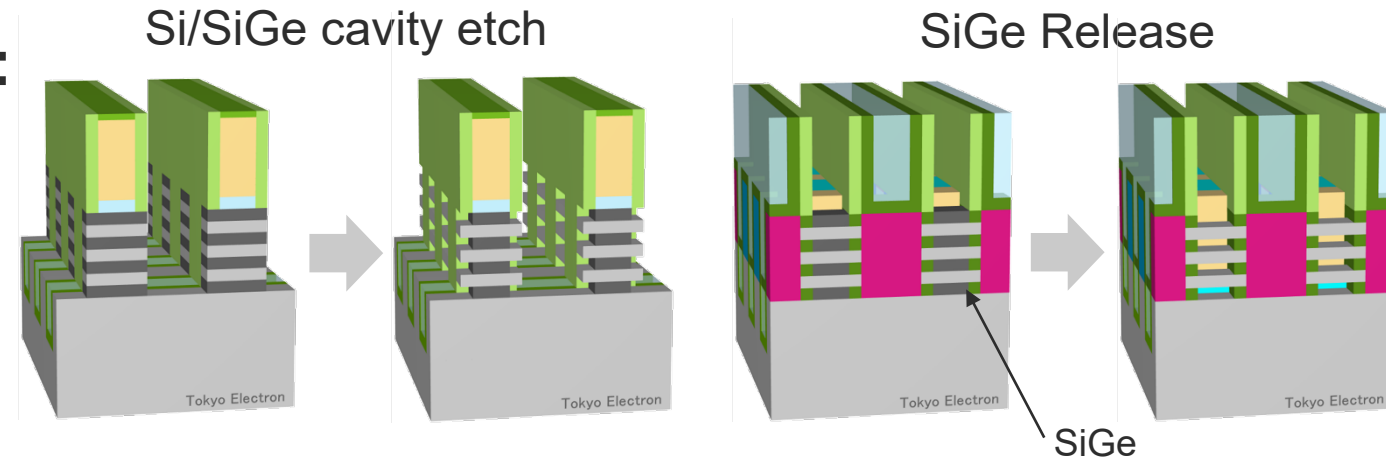
*3 PDN: Power delivery network

Respond to changes in device manufacturing and EUV lithography for further scaling

Initiative for GAA Nano Sheet Structures

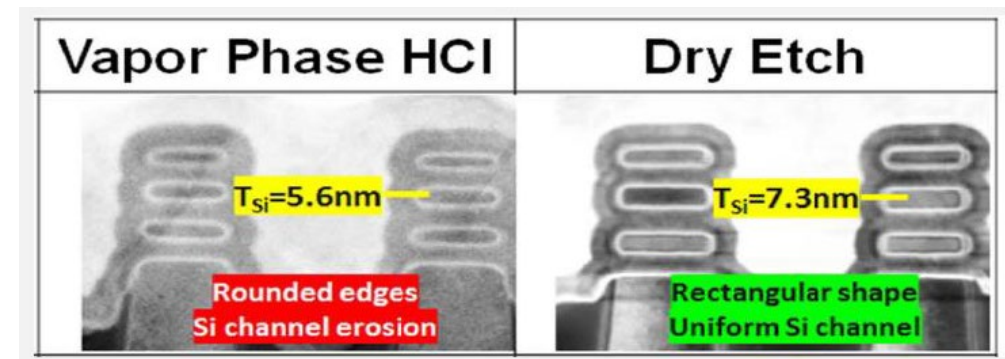
Nano Sheet process challenges:

- Uniformity in rectangle shape
- Mitigation of roughness/residue on patterned surface



TEL's initiative: Gas chemical etch

- High etch selectivity
- High uniformity
- Residue removal/decreased roughness



Source: N. Loubet, et al., IBM, TEL Technology Center, America (IEDM2019)

Leveraging the advantages of gas chemical etch to
contribute to leading-edge processes

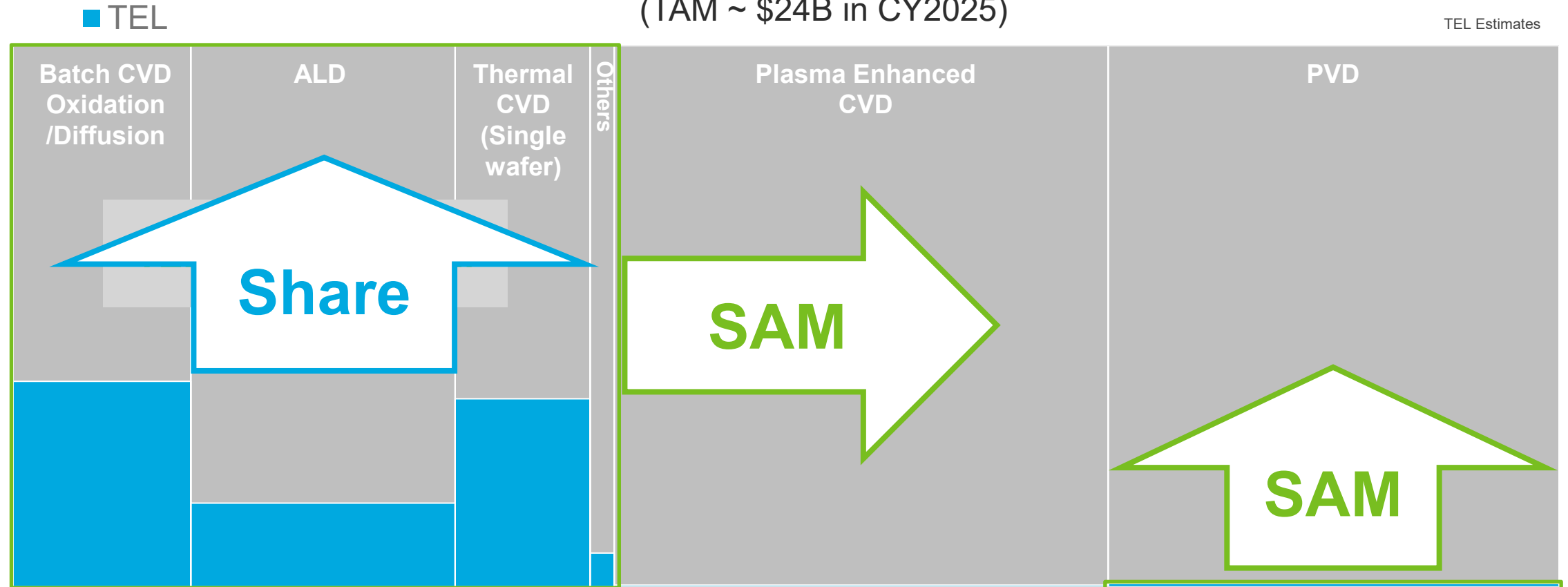
7-2-2. Deposition System

Business Strategy in the Thin Film Deposition Market

Expanding Market Share and SAM*

TEL's Market Share and SAM in Thin Film Deposition

(TAM ~ \$24B in CY2025)



* SAM: Served Available Market

Strategies in the Deposition Business 1:

Expand SAM with Single Wafer CVD

Triase⁺™



Single Reactor

Existing Platform

Episode™ 1



Single Reactor

Equipped with up to eight process modules

Episode™ 2 DMR*



*Duo Matched Reactor

Achieved high productivity
by processing 2 wfs/PM

Episode™ 2 QMR**



**Quad Matched Reactor

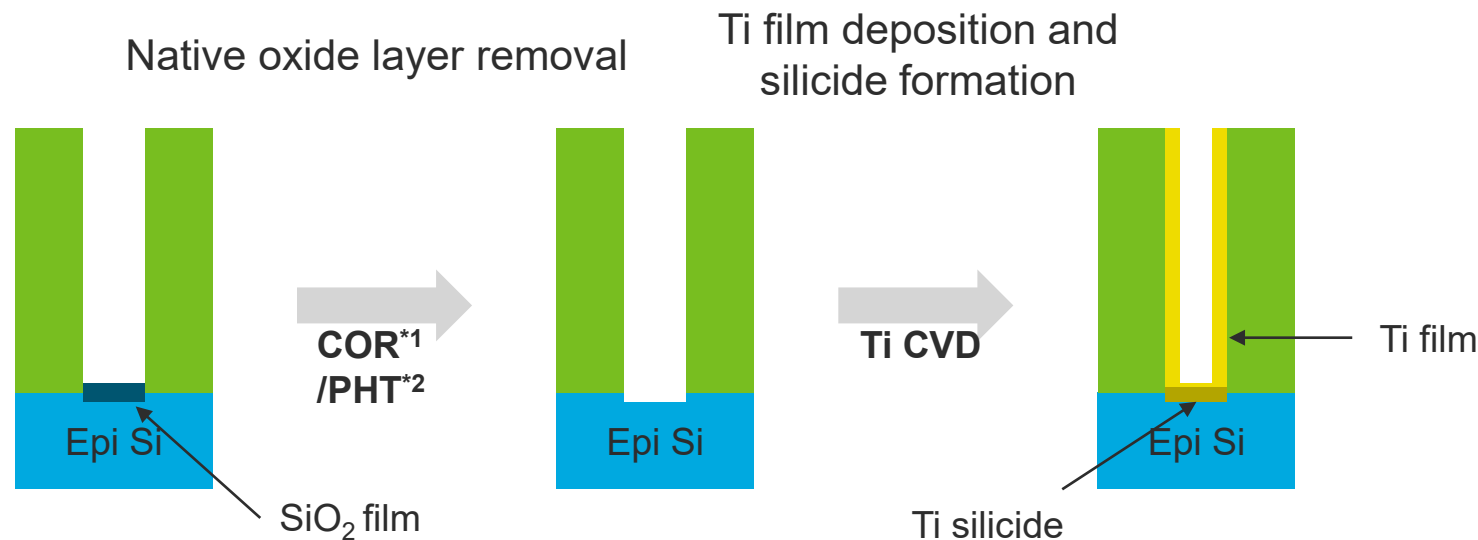
Equipped with a newly developed
high-density plasma source

Upcoming Release

Episode™ 1: Contact Formation Process

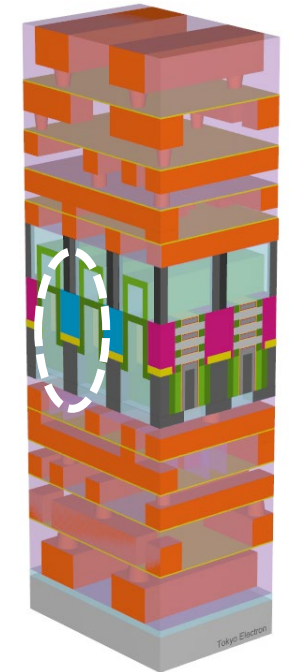
Source of all drawings: TEL

- Example of process flow



*1 COR: Chemical Oxide Removal

*2 PHT: Post Heat Treatment



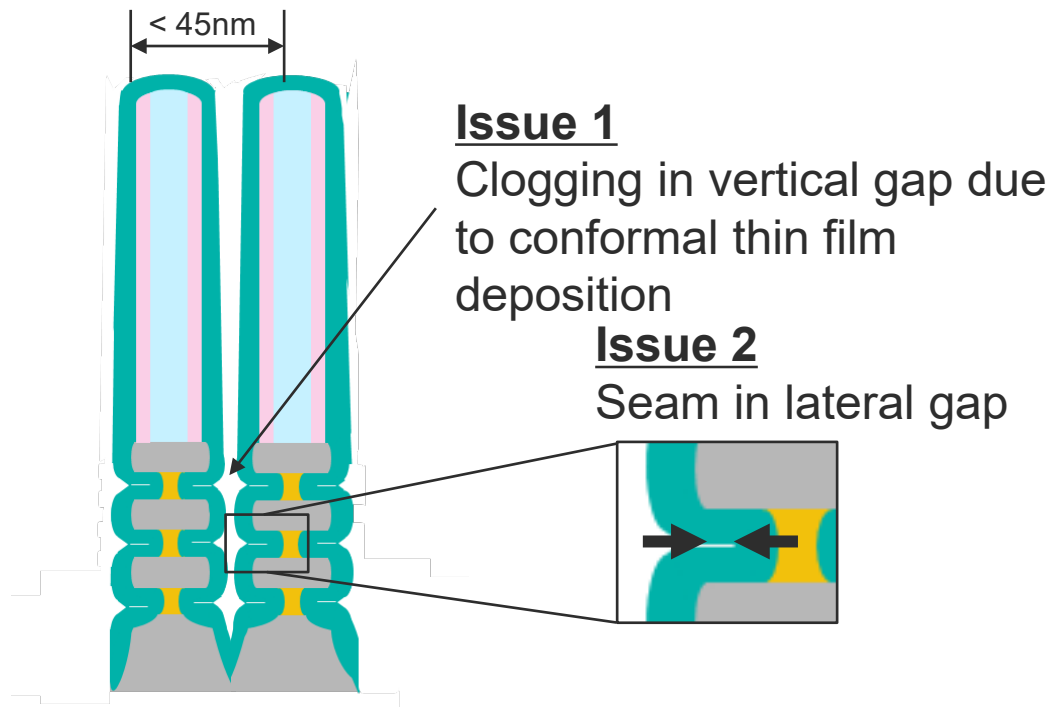
Multiple types of process modules are equipped on a high-vacuum transfer module, and low-resistance contacts are achieved by sequentially processing native oxide layer removal and metal film formation

Episode™ 1: Inner Spacer Formation - Lateral Gapfill

Source of all drawings: TEL

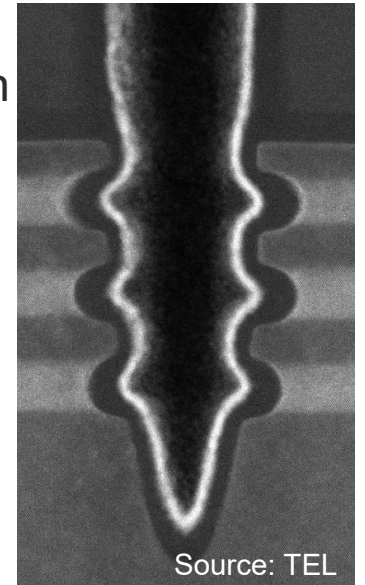
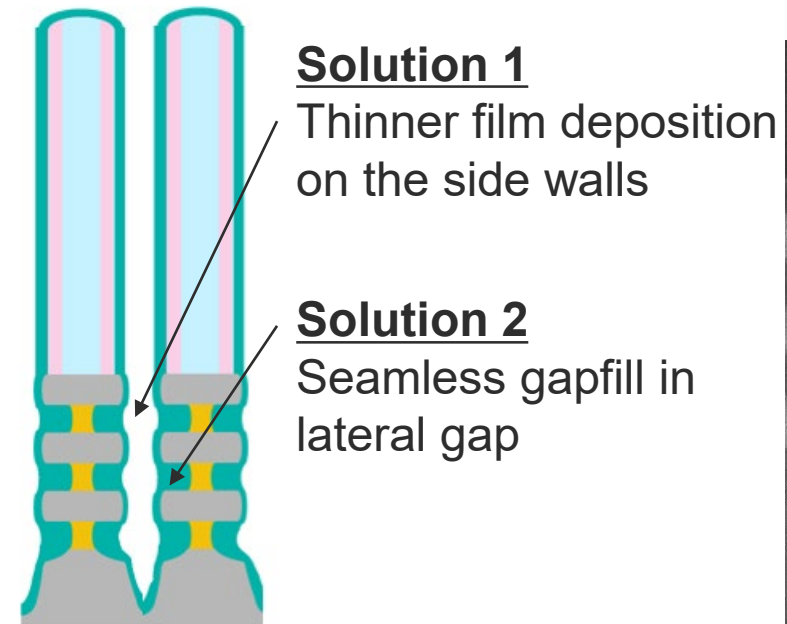
■ Issues :

Leak due to dielectric breakdown due to etching



■ Solutions :

Improve lateral gapfill performance



Realized seamless lateral gapfill using a unique thin film deposition technique and laterally uniform film modification using a newly developed high-density plasma

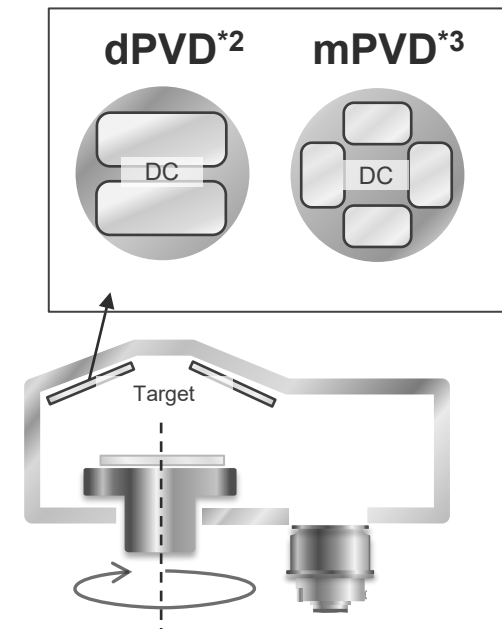
Strategies in the Deposition Business 2:

SAM Expansion with PVD

Source of all drawings: TEL

LEXIA™ -EX

- Oblique angle sputter with wafer rotation system
 - Excellent thickness uniformity (1σ 0.5%)
- Unique multi-cathode^{*1} configuration
 - High deposition rate
 - Capability of tuning film composition ratio with multiple materials
- High throughput (~100WPH)
- Significant footprint reduction vs conventional model



*1 Cathode: An electrode for material deposition

*2 dPVD: Dual cathode PVD

*3 mPVD: Multiple cathode PVD

Strategies in the Deposition Business 3:

Growth in Batch Thermal Process/Deposition



EVAROS™

- Major applications: ALD and CVD
 - General silicon processes (contact Si, channel Si, etc.)
 - ALD processes (SiN, SiO₂)
 - PE-ALD processes (SiN)
- Features
 - Maximum 200 wafers per batch
 - Larger reactor exhaust diameter to improve exhaust conductance, enabling uniform deposition on large-surface-area patterns
 - 25% less CO₂ emissions per wafer vs TELINDY PLUS™
 - Enhance labor reduction (one-touch start-up, self-maintenance, DX)

7-2-3. Cleaning System

Single Wafer Cleaning Strategy

■ Single wafer cleaning

– Bevel wet etch

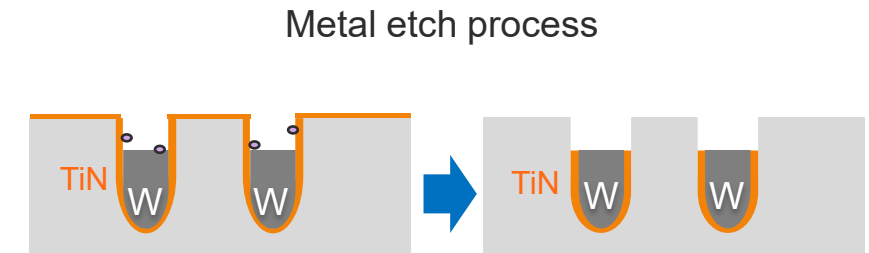
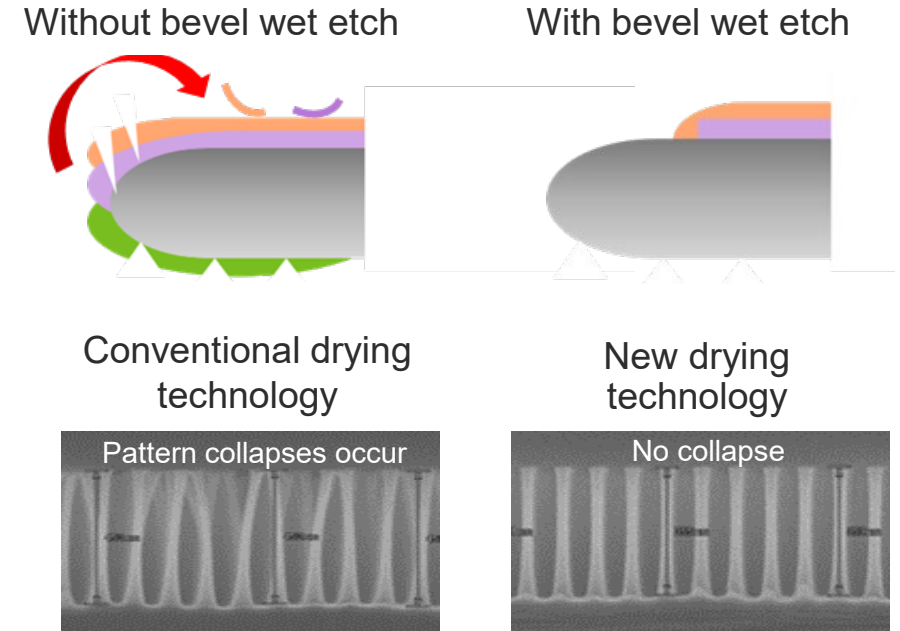
- Expect annual market growth rate of around 10%
- Contribute to improving customers' yields.
Maintain a high market share by differentiating through performance in precisely removing film from the outer part of the wafer

– Prevent pattern collapse

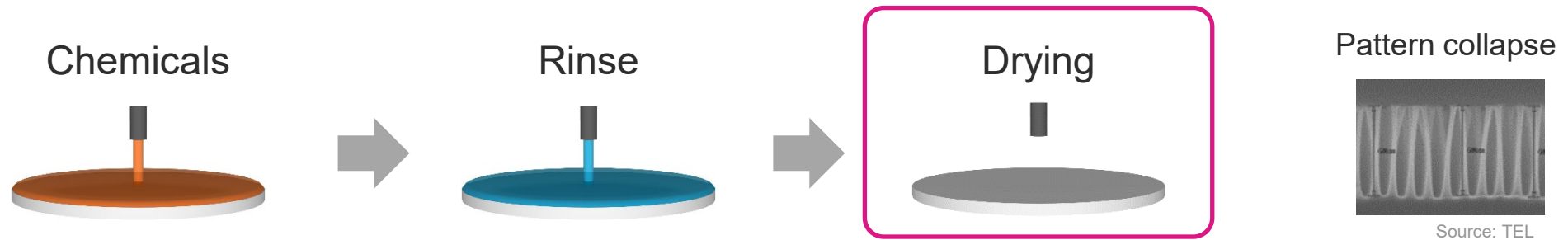
Expand market share by TEL original technology to reduce collapse of high aspect ratio pattern

– Metal etch

Launched new dedicated SPM chambers for controlling selectivity for metal in order to solve reduced yield issues caused by dry etch damage and residue

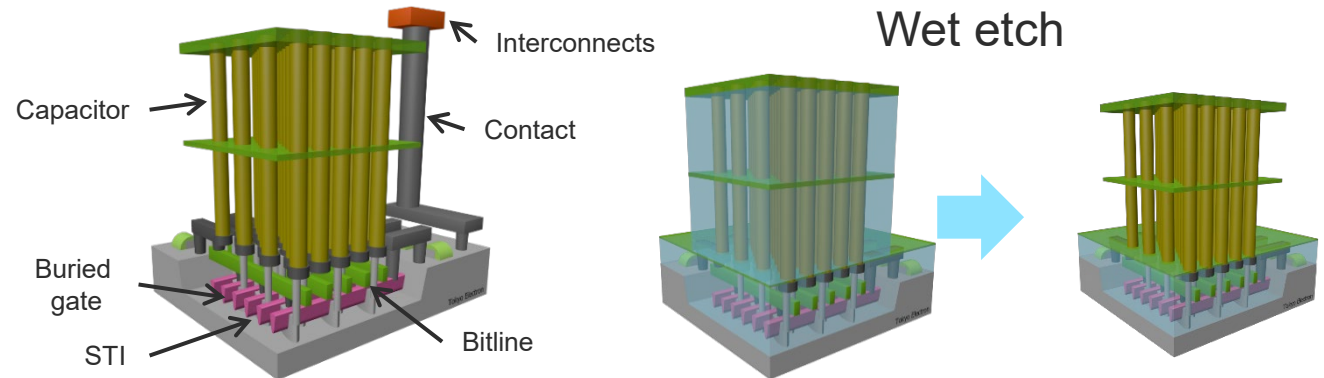


Technology Challenges in Cleaning for State-of-the-Art Devices



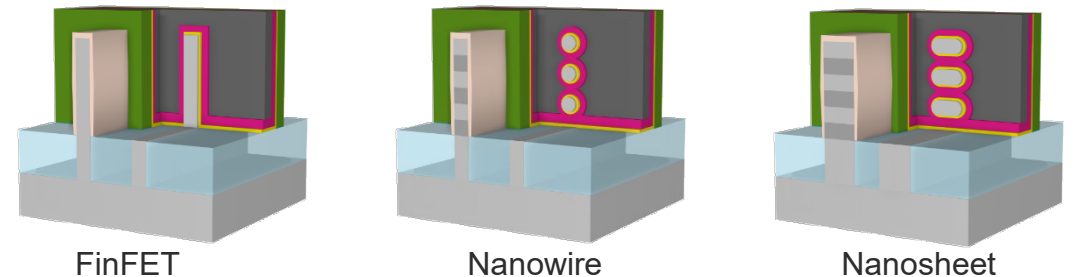
■ DRAM

- Post-STI etch cleaning
- Mold wet etch after capacitor electrode formation



■ Logic

- Post-fin etch cleaning
- Post-nanowire/nanosheet formation cleaning



FinFET

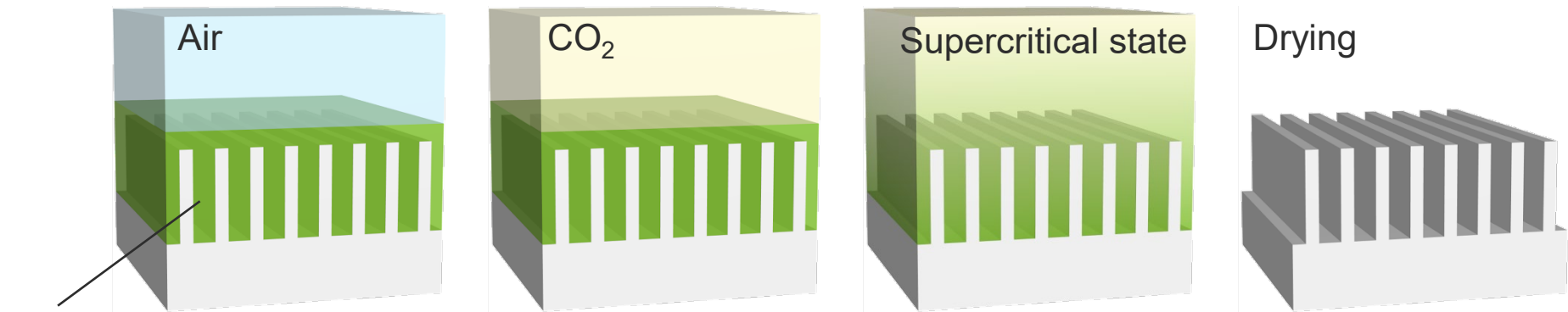
Nanowire

Nanosheet

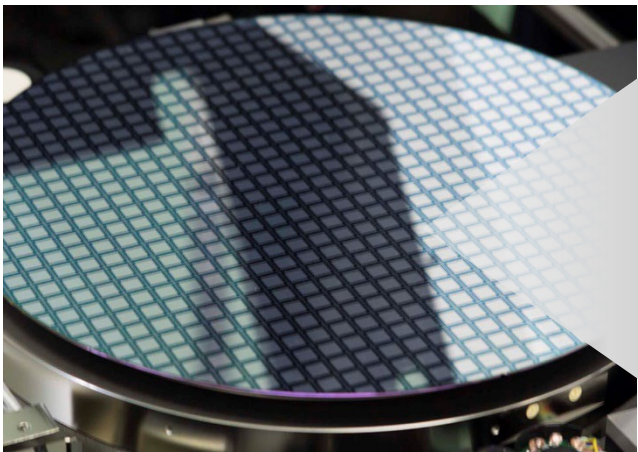
Source of all drawings: TEL

Drying technology more difficult due to further scaling and higher aspect ratios
in device manufacturing

Supercritical Drying Technology



Source of all drawings: TEL



	Traditional drying	TEL's supercritical drying
Top View		
Side View		

Source: TEL

Supercritical drying technology prevents pattern collapse

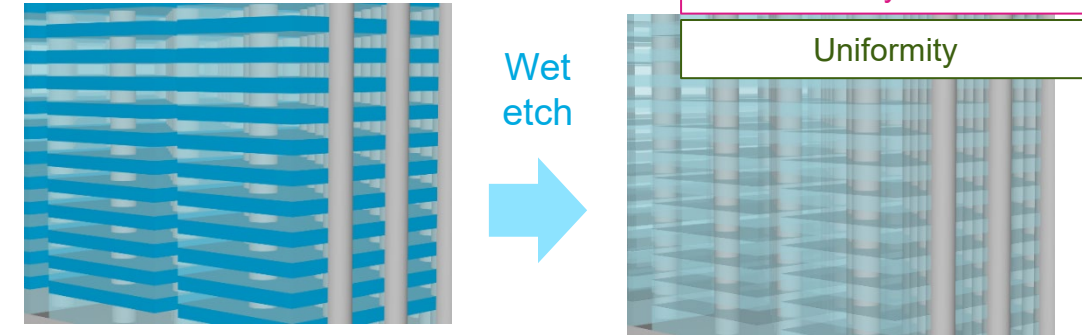
Batch and Scrubber Cleaning Strategy

Source of all drawings: TEL

■ Batch cleaning

- SiN etch and W etch processes for 3D NAND
Focus on processes that require long durations and advanced process technology. Differentiate by realizing high uniformity, high selectivity and high productivity in wet etch

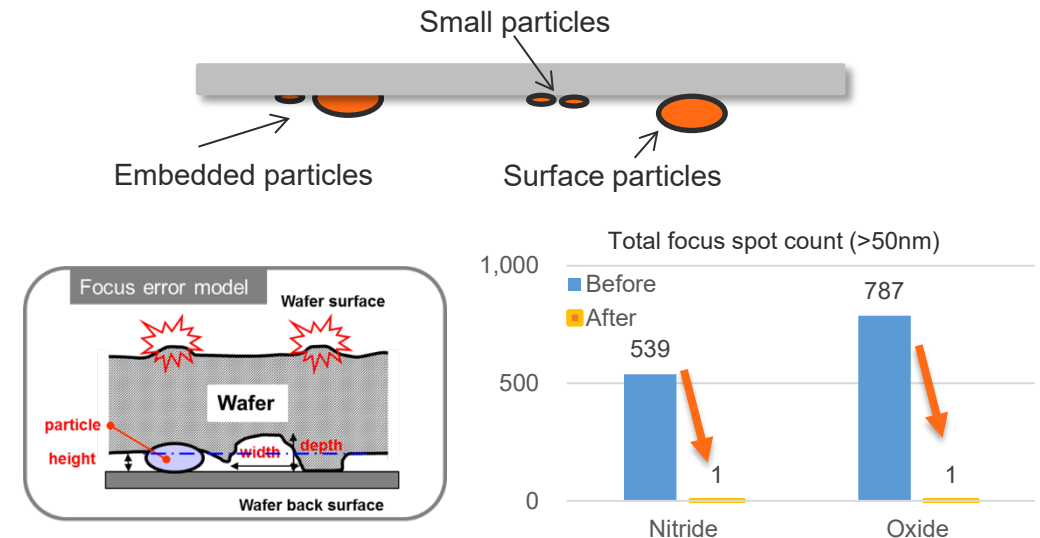
SiN etch process



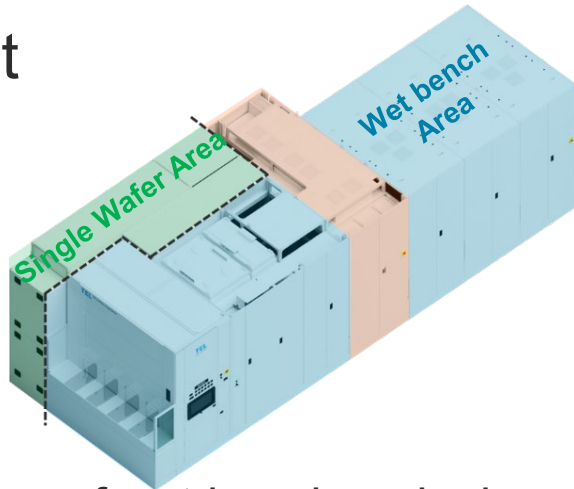
■ Scrubber cleaning

- Pre-lithography process
Provide high-value solutions such as reducing particles brought in by wafers, contributing to the improvement of exposure tool availability which have grown increasingly important due to the introduction of EUV

Wafer back and defocus diagram



■ Concept



A combination of wet bench + single-wafer process

Method	Features
Wet Bench	High-temp/ long-duration process, wet etch
Single Wafer	Advanced drying technology, particle control

■ Target Application

- Advanced wet etch + advanced dry tech



- Highly selective wet etch process will be required for also 3D DRAM in addition to 3D NAND

- High throughput + surface cleanliness



- High surface cleanliness is required for logic and DRAM

TEL will contribute to customer technology development by continuing to create new value, overcoming the constraints of traditional equipment classifications

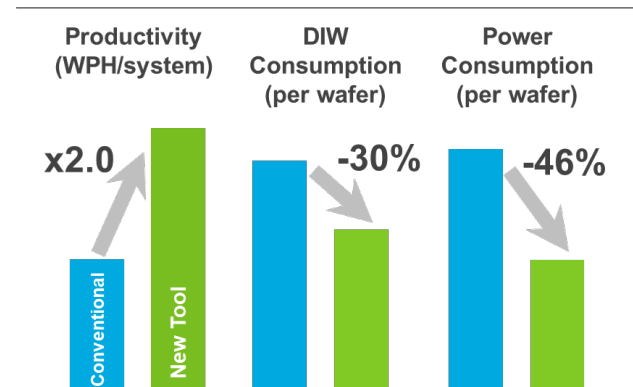
Development of Cleaning Systems

Source of all drawings: TEL

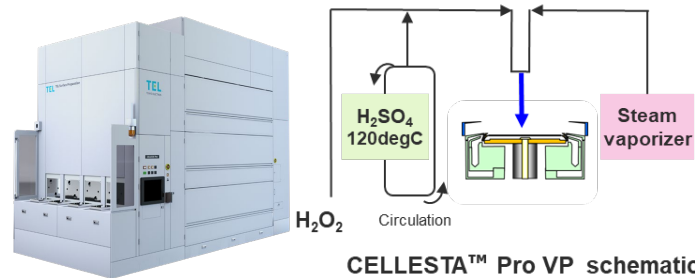
High Productivity Wet Bench (EXPEDIUS™-R)



Industry's first large-batch process
(increased wafer counts)

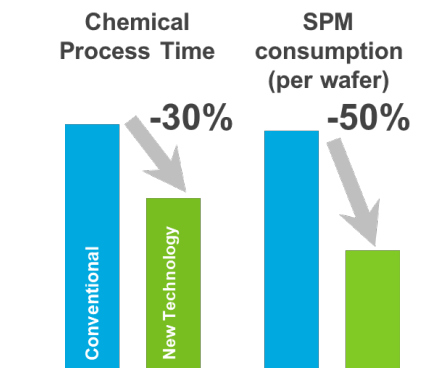


SPM^{*1} Vapor Technology (CELLESTA™ Pro VP)

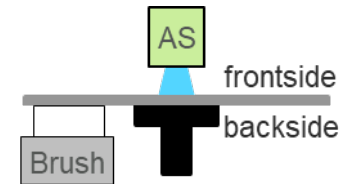


Enabled higher temperature process due to
a more effective reaction by adding water
vapor to chemicals

*1 SPM: Sulfuric Acid and Hydrogen Peroxide Mixture

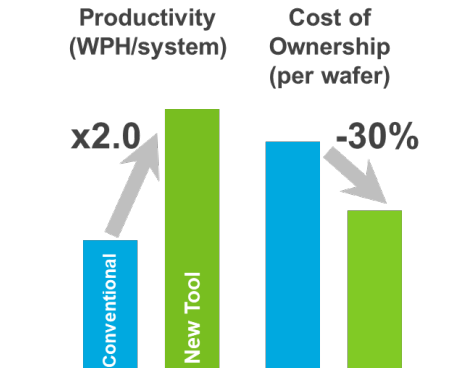


Simultaneous Scrubber (CELLESTA™ MS2)



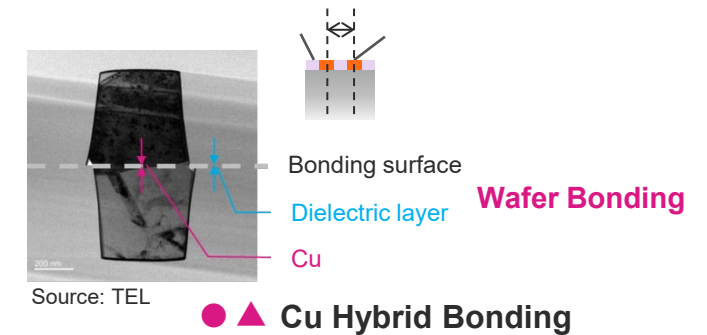
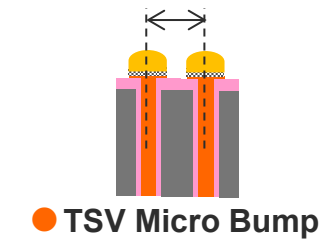
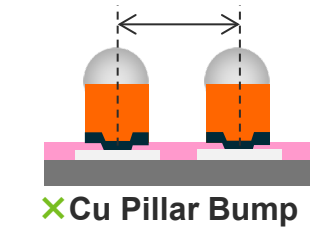
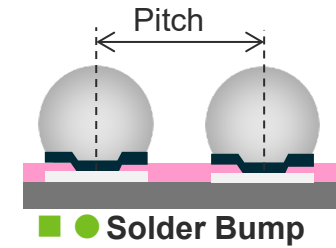
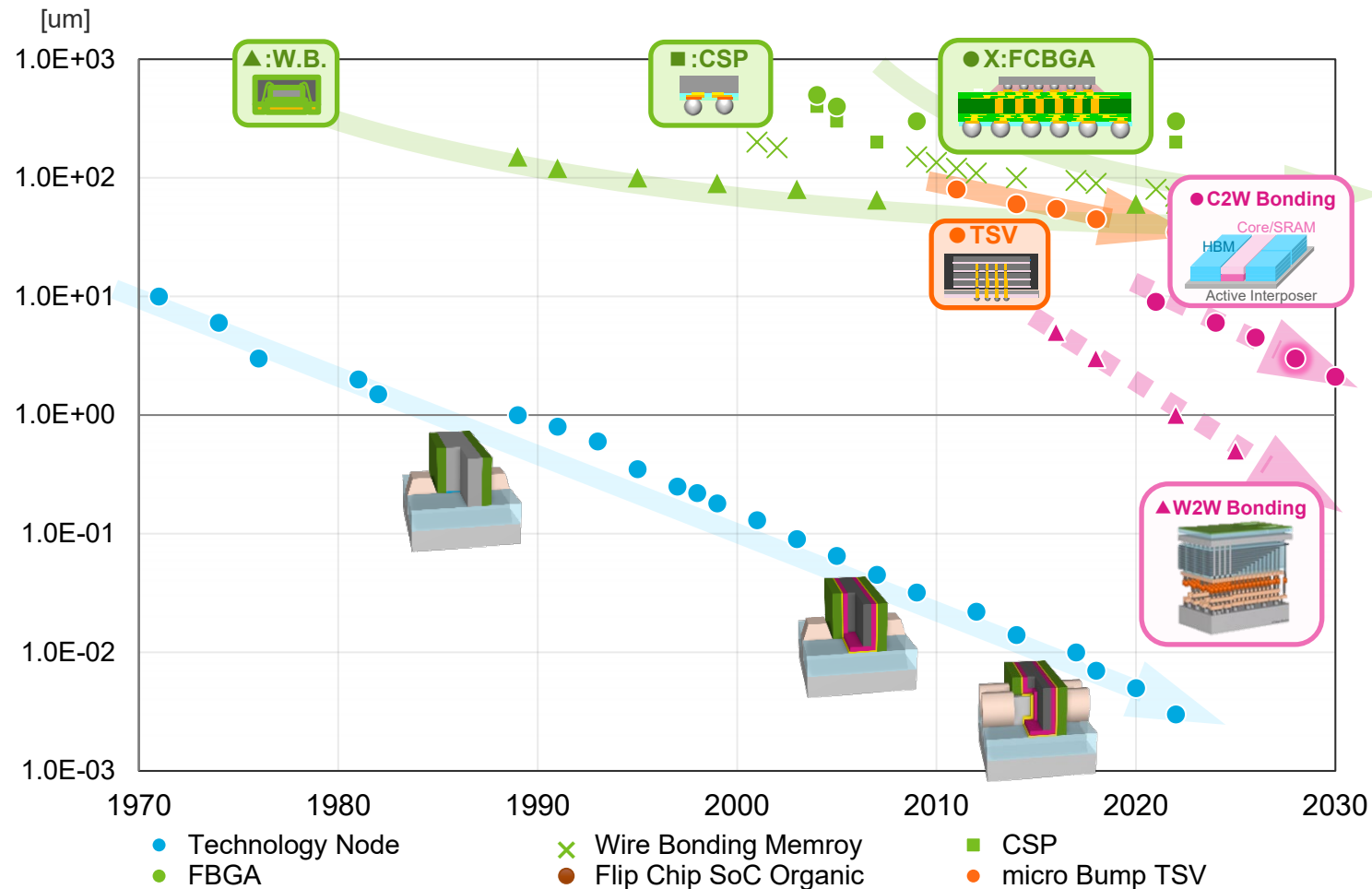
A tool enabling AS^{*2} process on wafer
frontside and physical brushing process on
wafer backside simultaneously in a single
chamber

*2 AS: Atomized Spray



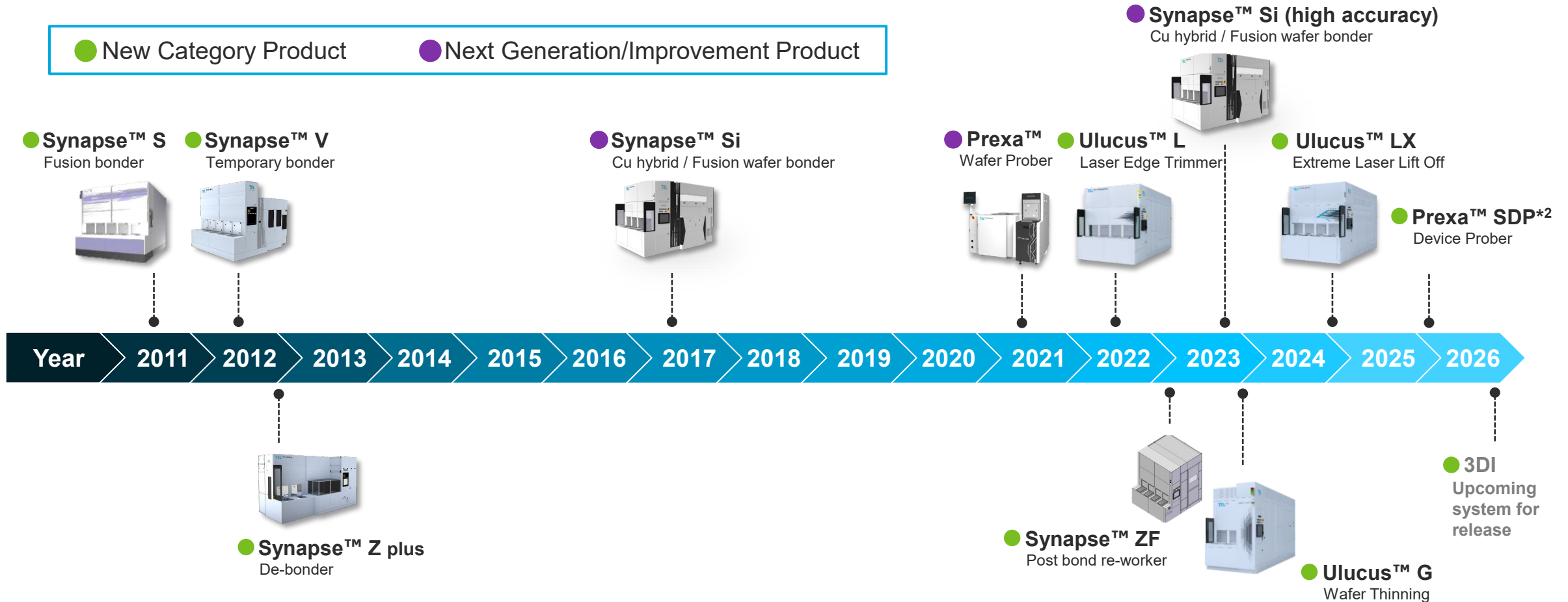
7-3. Backend Business Strategy

Semiconductor Technology Node and Bump Pitch



Introduction of wafer bonding technology accelerates further reduction of pitch

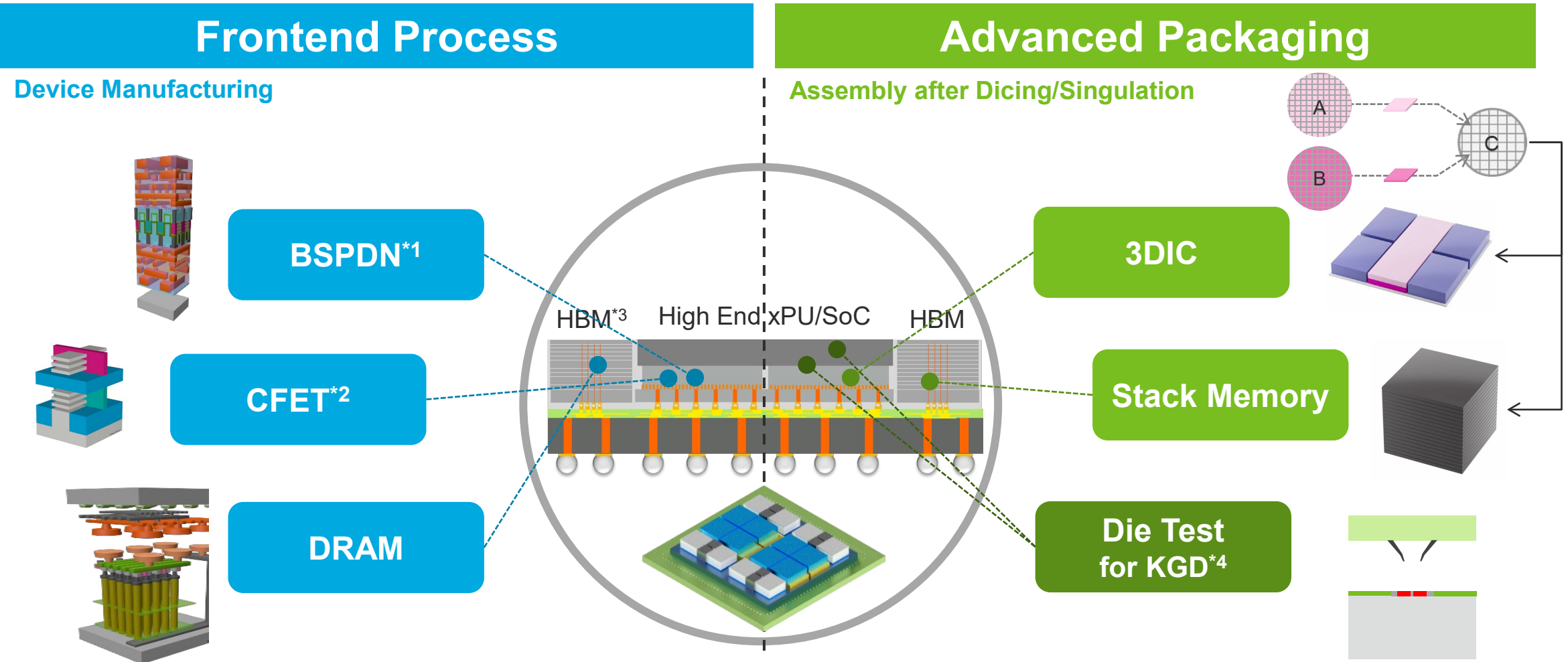
History of Product Launches in Assembly and Test*1 Systems



Accelerating product development to prepare for the era of 3D integration

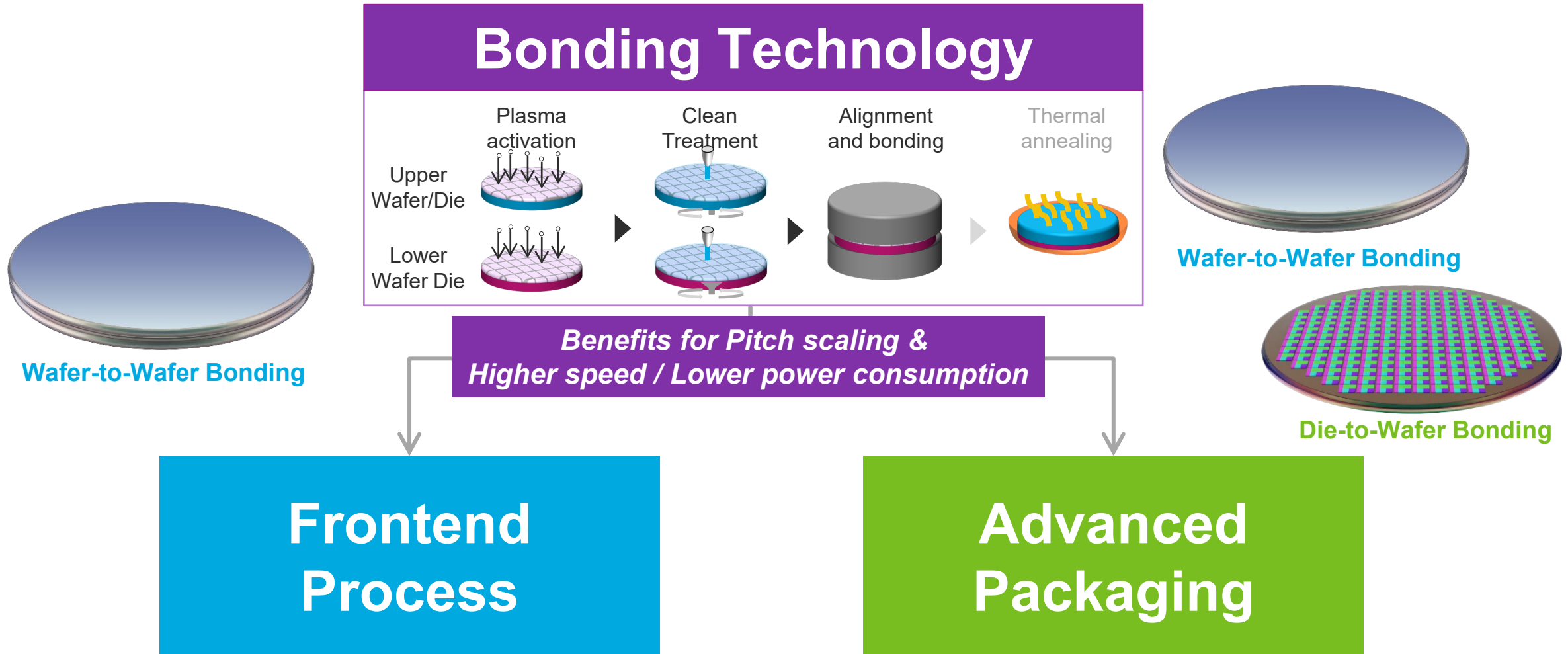
*Test : Prober for Advanced Packaging Test
 *2 SDP : Singulated Device Prober

3DI / Test Business Expands Opportunities for HPC/AI Device

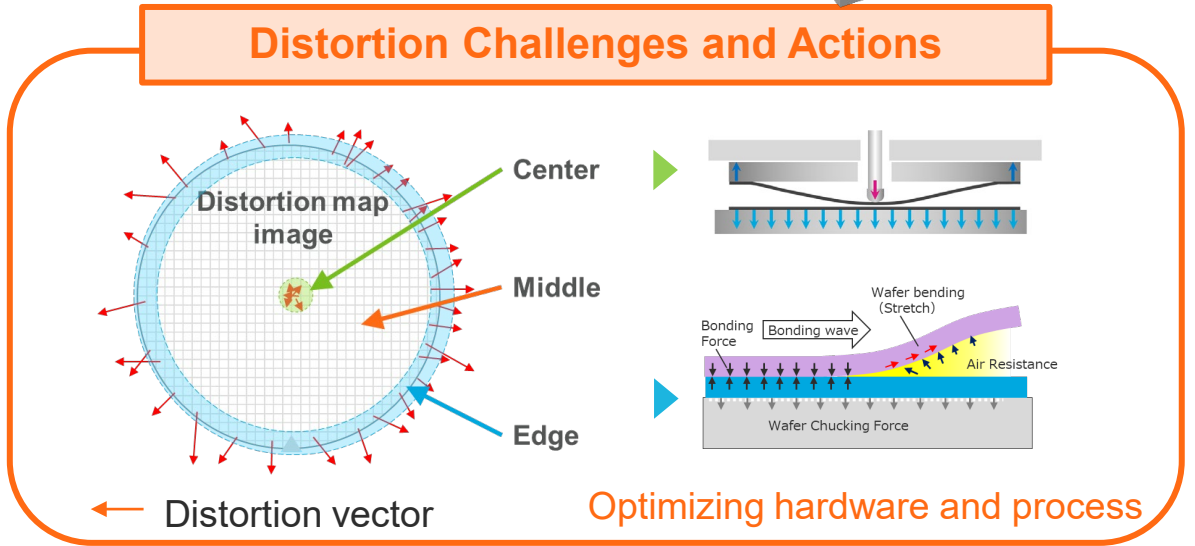
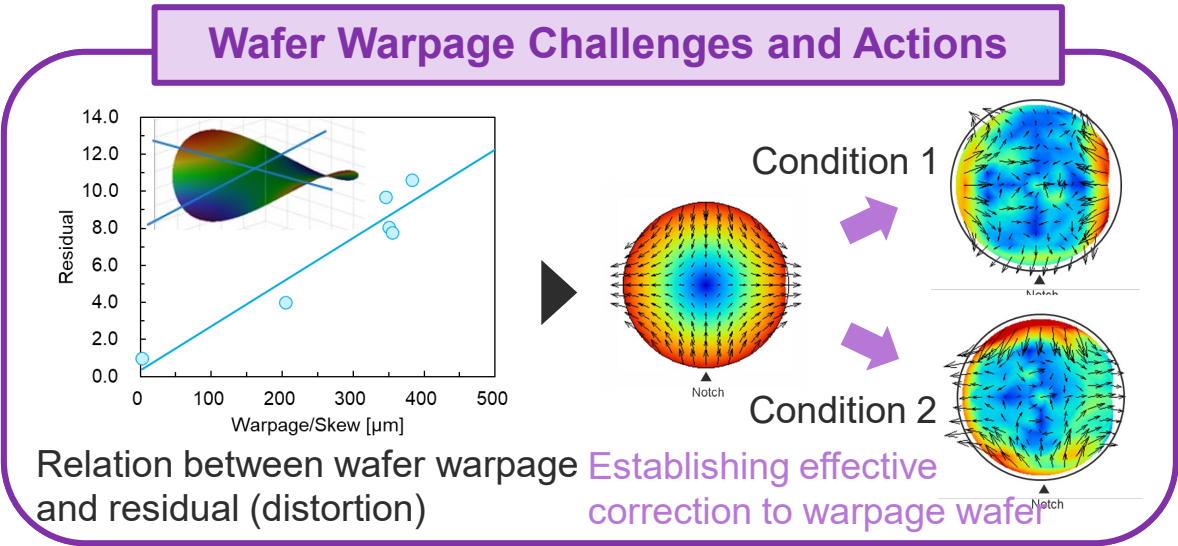
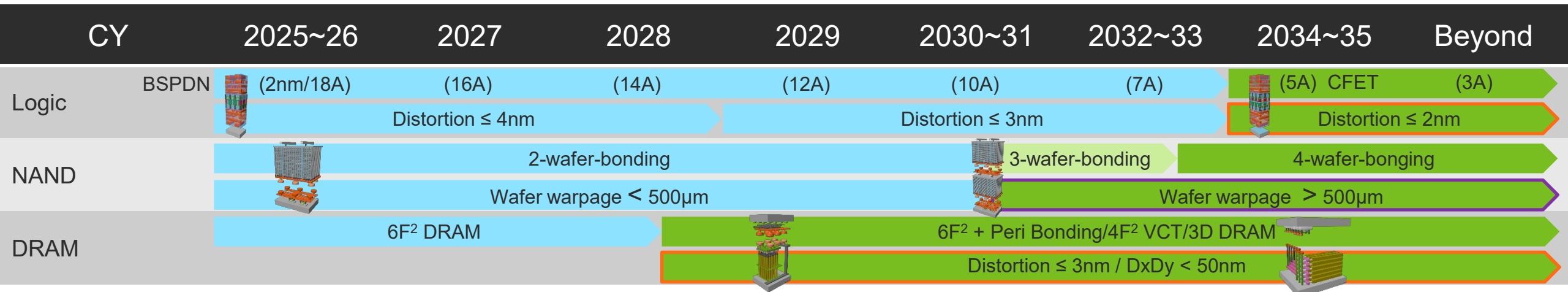


*1 BSPDN: Back Side Power Delivery Network
 *2 CFET: Complementary Field Effect Transistor
 *3 HBM: High Bandwidth Memory
 *4 KGD: Known Good Die

TEL's Opportunities for Bonding Technology

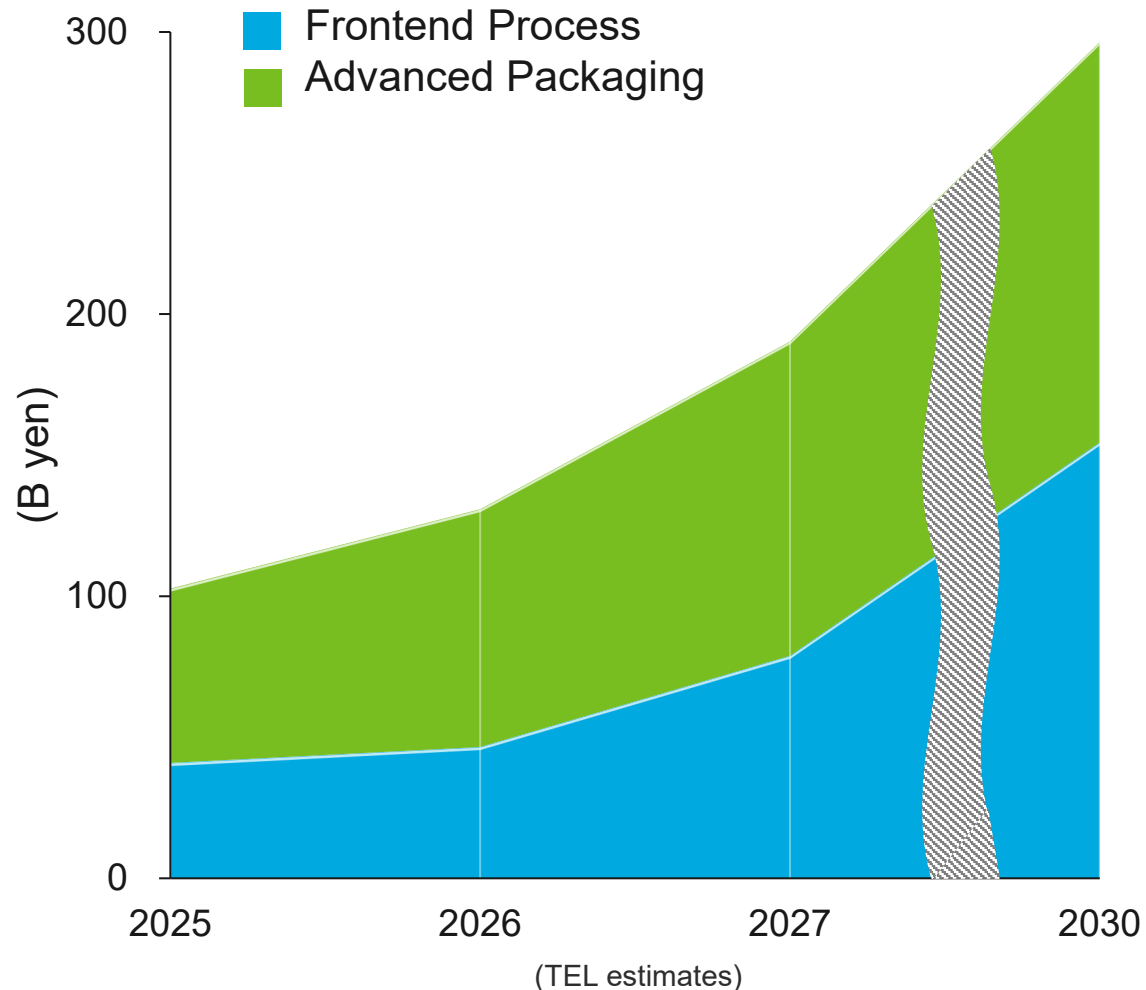


Wafer Bonder Technology Roadmap and Challenges



TEL is developing various technologies in advance to prepare for next-generation devices

Bonding Process Equipment TAM*

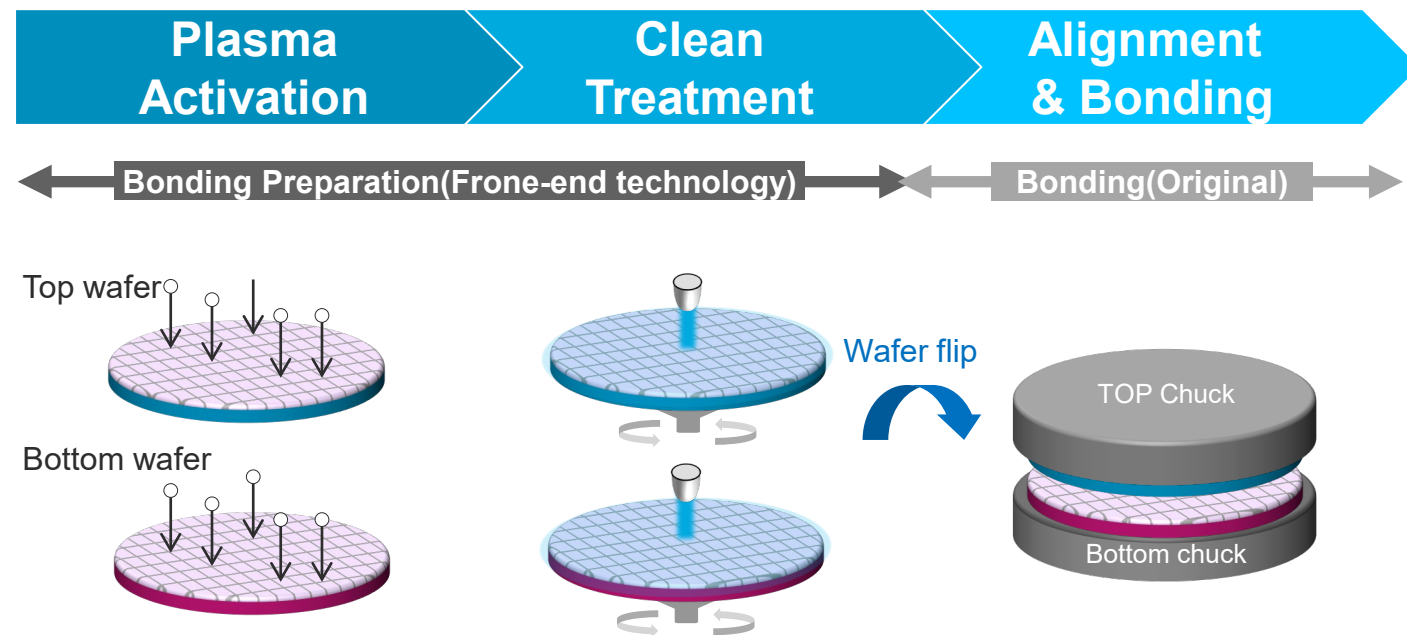


Anticipating a TAM CAGR of 24% from CY2025 to CY2030

- Projected to achieve 300 billion yen by CY2030
- Encompassing both frontend processes and advanced packaging equipment
- Addressing bonding/debonding, slicing, and thinning process equipment utilizing various technologies

* TAM : Total Available Market

Wafer-to-Wafer Permanent Bonder Synapse™ Si



- TEL's existing broad technology and business contributing effective product development/CIPs
- Making good progress with major memory, logic customers towards high volume manufacturing
- Leading W2W Fusion/Cu hybrid bonding technology for next generation device manufacturing

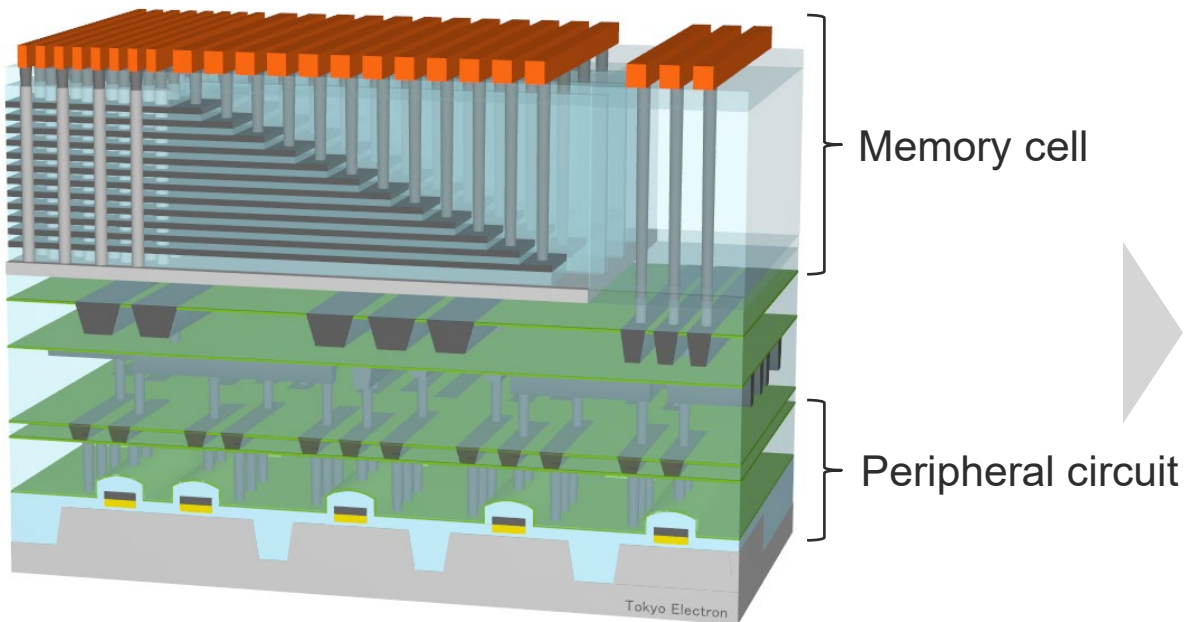
Broad Applications and Expansion of Bonding Technology

Application	Frontend Process					
	CIS* ¹	NAND		DRAM		Logic
Stacking Device	BSI* ² 	3D NAND 		VCT* ⁵ DRAM 	3D DRAM 	BSPDN BSPDN & CFET
Bonding	Wafer to Wafer (CHB* ³ /Fusion)	Wafer to Wafer (CHB)		Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (HB* ⁶ /Fusion)
Structure						
Status	HVM* ⁴	R&D~HVM	R&D	R&D	R&D	R&D~HVM R&D

The design of future devices is transitioning from single bonding to multi-bonding structures

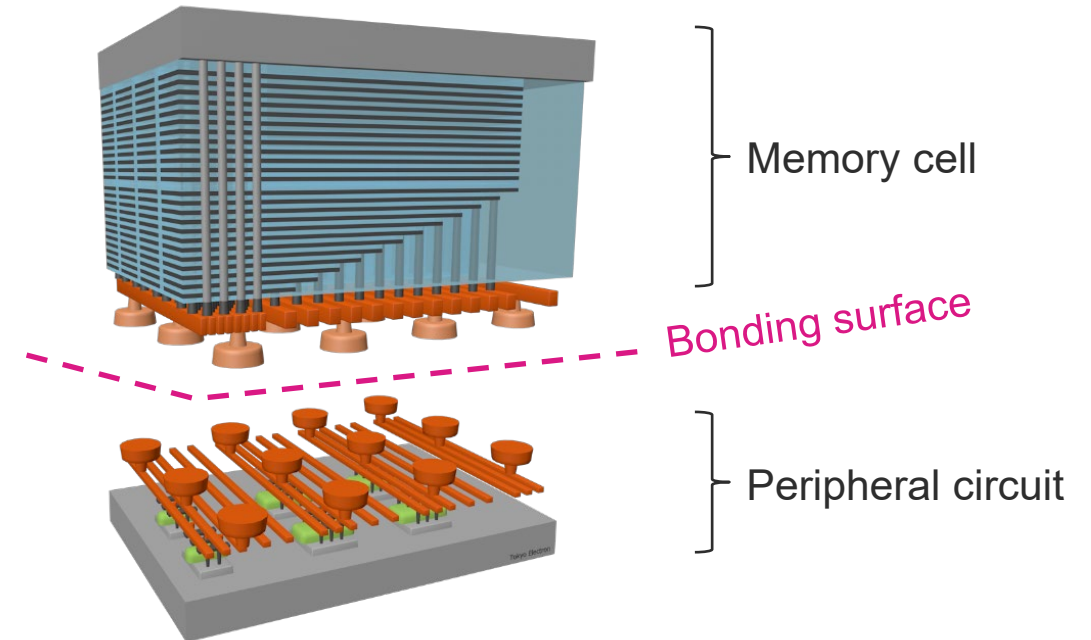
Wafer Bonding Application for 3D NAND

Current structure



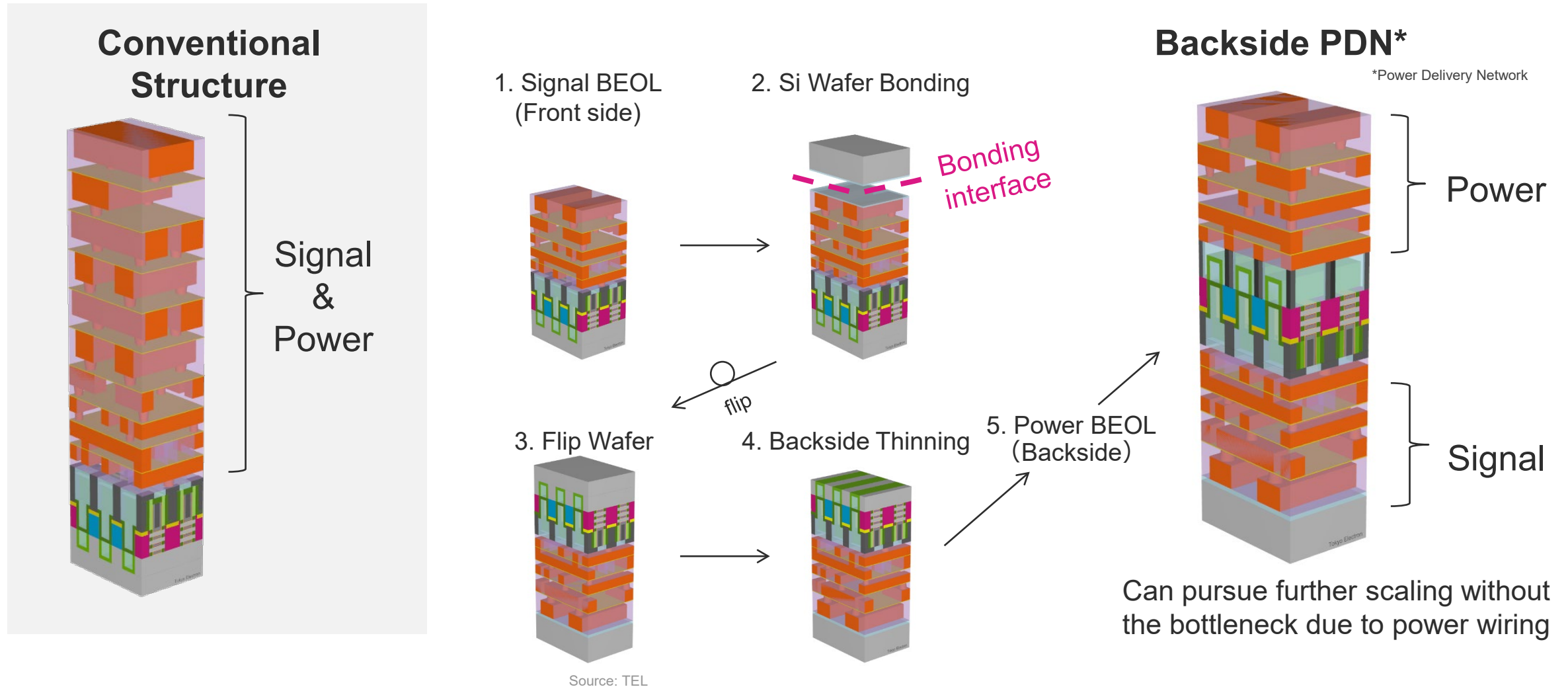
- ✓ Peripheral circuit performance deteriorates due to exposure to high temperature during memory cell manufacturing
- ✓ Long interconnects wiring

New structure



- ✓ Peripheral circuit is manufactured on the separate wafer and bond to the memory cell wafer
 - higher peripheral circuit performance
 - shorter TAT* process
- ✓ Shorter interconnects wiring

Wafer Bonding Application for Logic Backside PDN



Broad Applications and Expansion of Bonding Technology

Application	Advanced Package		
	Stack Memory / HBM	3DIC	
Stacking Device			
Bonding	Wafer to Wafer / Die to Wafer (CHB/Fusion)	Wafer to Wafer / Die to Wafer (CHB)	Wafer to Wafer (Fusion)
Structure	• Thinner die / more stacks • High density connection • Better thermal conductance	• Small formfactor (3D stack vs. 2D) • Higher speed (shorter wiring, no bump) • Lower power (shorter wiring, no bump) • Lower cost (higher yields, easy to mix processes) • Shorter time to market (matured IP block reuse)	• Better thermal conductance
Status	R&D	R&D ~ HVM	HVM

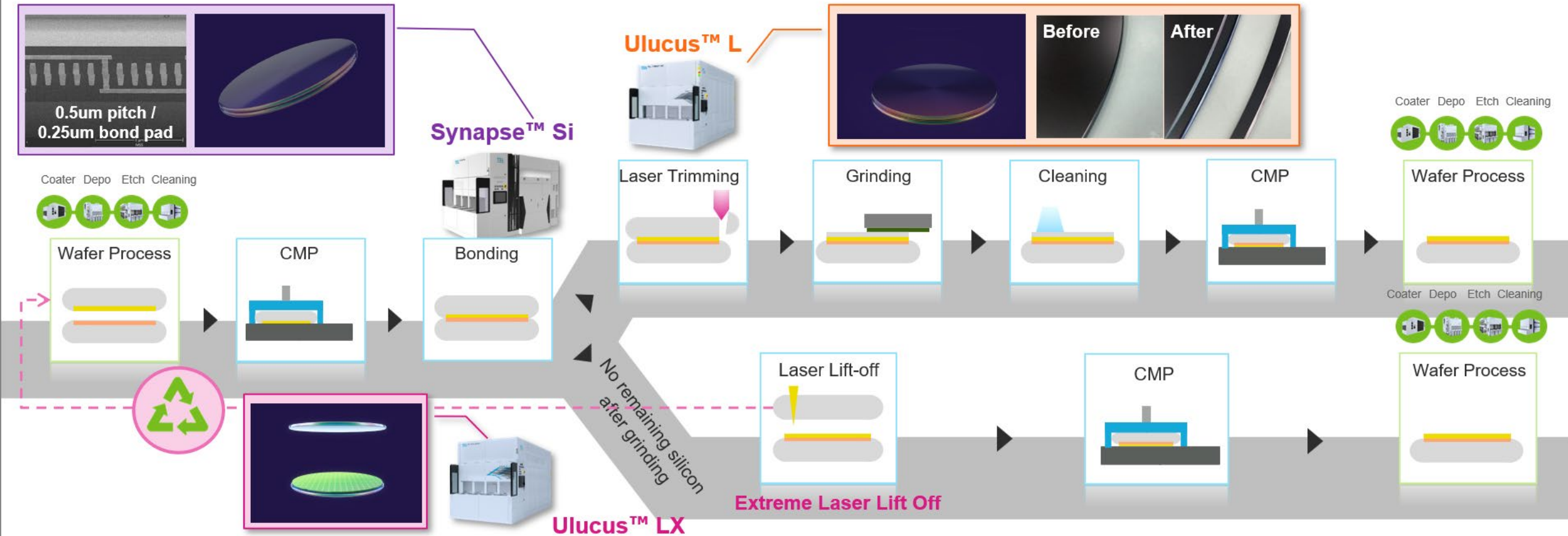
The opportunity for CHB/fusion bonding is growing to encompass advanced packaging

Frontend Wafer Bonding Process and TEL Products

Pre-bond

Example of Wafer Bonding Process

Post-bond



Integrating various TEL equipment enables next generation wafer bonding processes that deliver high performance and process efficiency

Laser Trimming System: Ulucus™ L

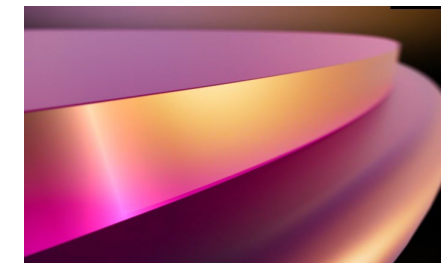
Source of all drawings: TEL

■ Concept

- Edge trimming of bonded wafer with laser
- Latest platform utilizing super clean technology from frontend process, with the integration of laser control technology

■ Features

- High accuracy: enabling narrower trimming width and smooth sidewall with less damage and good yield
- High-productivity, high-reliability process
- Environmentally-friendly process by reducing DIW usage by 70% or more

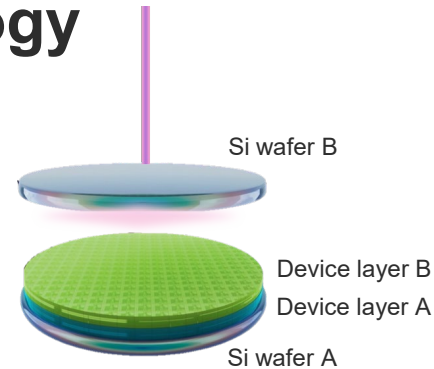


High-accuracy and high-quality laser trimming process -
environmentally-friendly and innovative approach for wafer-level bonding

Introducing Ulucus™ LX for Post-Wafer Bonding Process

■ Extreme laser lift-off (XLO) technology

- Advanced thinning and critical technology for post-wafer bonding process
- Unique laser technology enables separation of the Si-substrate from the device layer



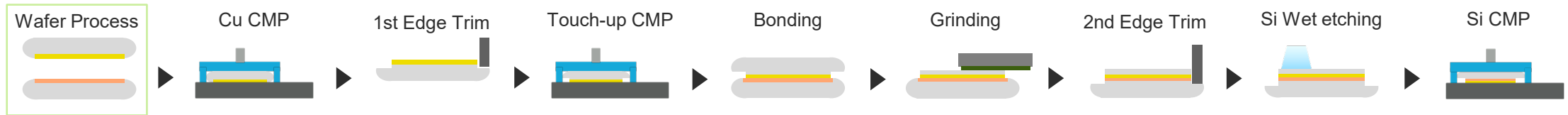
■ Advantages for process and environment

- Enhanced efficiency in silicon active areas
- Fewer process steps required
- Reduced need for DI water usage and CO₂ emission
- Opportunity for wafer reuse

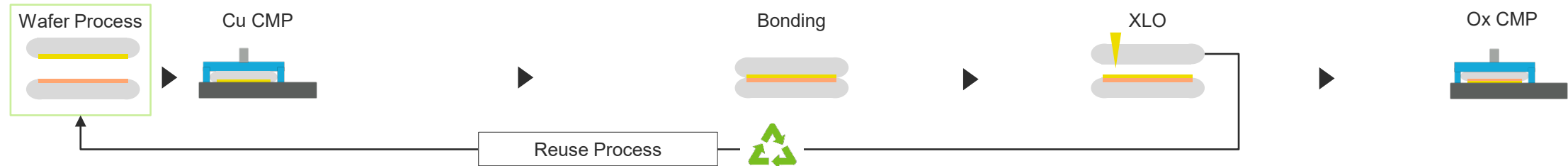


Ulucus™ LX Advantages

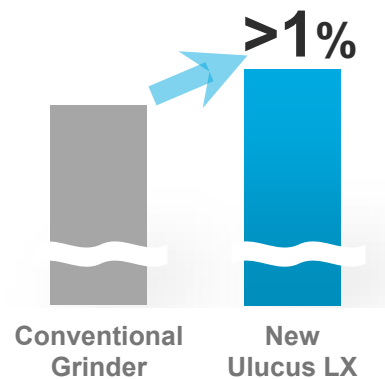
Permanent Bonding Process with Grinding & Blade Edge Trimming (Conventional)



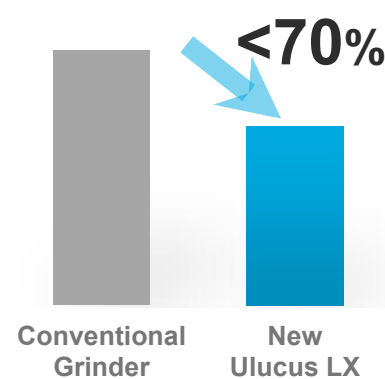
Permanent Bonding Process with XLO (Extreme Laser Lift Off)



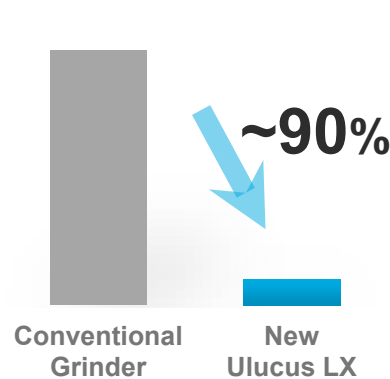
Active Silicon Area



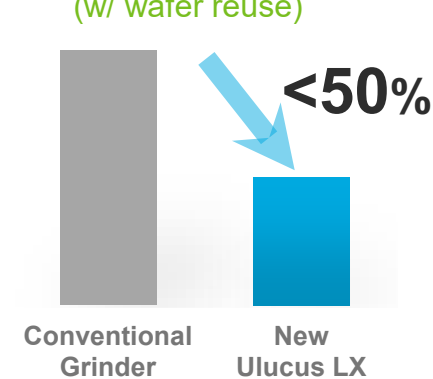
of Process Steps



DIW* Usage



CO₂ Emission (w/ wafer reuse)



No Silicon Sludge → Advantage Over Grinder



Source: TEL

8. MAGIC Market and Field Solutions Business Initiatives

MAGIC market

- Expected market growth of 2x
(approximately \$25B in 2023, projected \$50B in 2030)
- Developing and supplying equipment for MAGIC
- Demo line ready for 200mm MAGIC
 - Yamanashi, Kumamoto, Miyagi
 - Massachusetts, Minnesota, Florida



Source: TEL, Licensed Image

Equipment for Mature Generations

- Reengineered equipment for 200mm wafer
 - Thermal deposition systems, coater/developer, etch systems, etc.
 - Sales expansions not only for replacement demand of existing customers, for emerging customers and for emerging applications
- Equipment for power devices
 - Equipment for SiC wafer, 300mm etch system
 - Respond to the demand for power devices, such as for representative automotive, expanding usage across various fields.



SiC epitaxial CVD system

By integrating our technological assets with new technologies,
improve productivity and reduce impact on the environment

Providing Diverse Systems and Solutions for Diverse Needs

Evolution of Leading-edge Devices

Heterogenous Integration

Layering

Miniaturization

Diversification of devices



PLP



μOLED



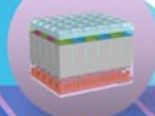
Smart Glass



Power



RF Filter



CIS



Si Photonics

Diversification of substrates/ materials

Square substrates, glass, SiC, GaN, LT/LN, 150/200/300mm

Bonder

Test

Cleaning

Etch

Litho

Dep

GCB

TEL's coverage

Support > 100,000 units

Maximize Customer's Productivity

Field Solutions

Source: Licensed Image
Source of all drawings: TEL



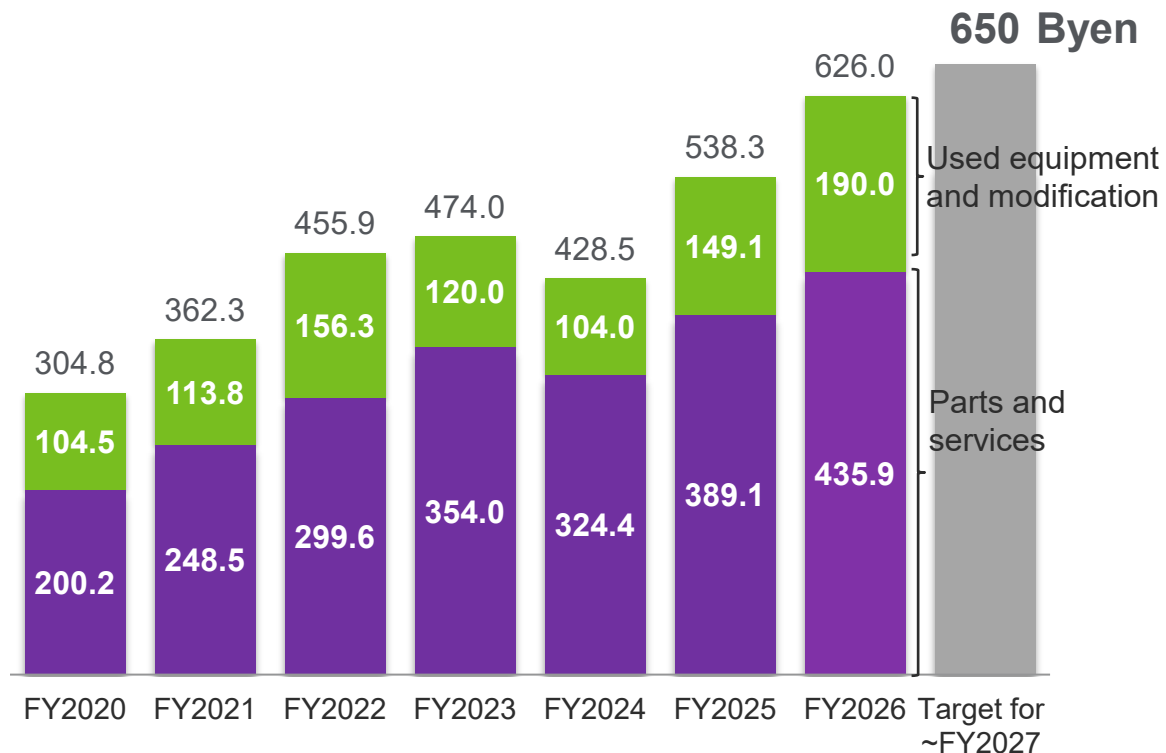
Basic Strategy for Field Solutions (FS)

- Deploying solution business based on installed base
- Development and promotion of advanced Field Solutions
 - Providing leading-edge and sustainable support that utilizes the latest technology, such as DX
 - Development of remote maintenance support and training tools
- Enhancing the front-lines engineers and capabilities
 - Continuous skill improvement for field engineers

Support customers to maximize their business operations
through services with high added value

Field Solutions (FS) Sales Results and Business Contents

FS Sales



■ Parts and repair

- Predictive maintenance for parts deterioration
- Appropriate parts inventory management and prompt delivery

■ Services

- Providing “comprehensive contract type” services that encompass everything from equipment delivery to after-care maintenance
- Proposing solutions that address customer demands and maximizing equipment utilization rates

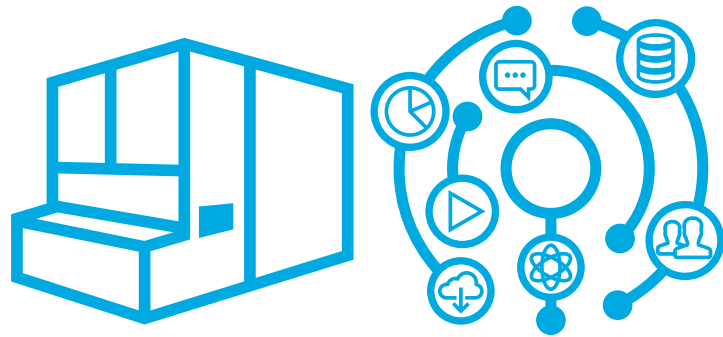
■ Modification

- Productivity improvement
- Yield improvement

SAM is expanding with over 100,000* installed base currently and increasing by approx. 4,000 to 6,000 units each year

Advanced Field Solutions

TELeMetrics™



- Monitoring data on individual equipment
- Knowledge management and accumulation of problem case studies

Remote Support

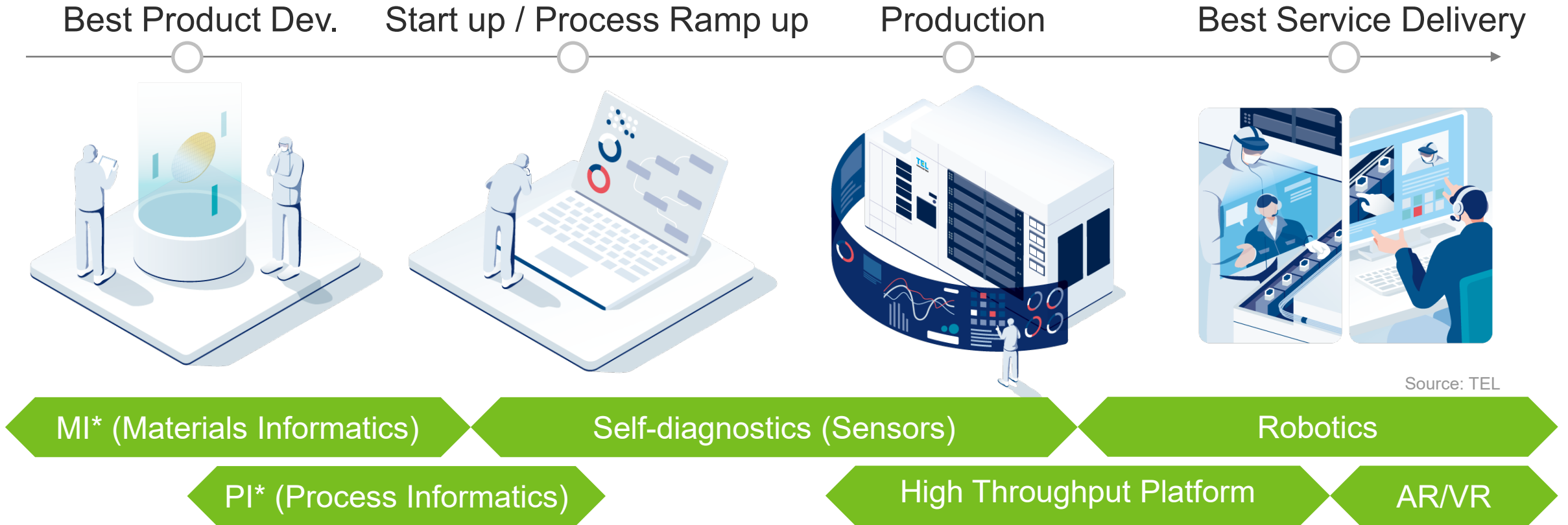


- Minimization of downtime through predictive maintenance of equipment
- Remote support that enables prompt response even under travel restrictions

Proposing solutions with high added value
centered around “TELeMetrics™” that utilize DX

9. Digital Transformation (DX) Initiatives

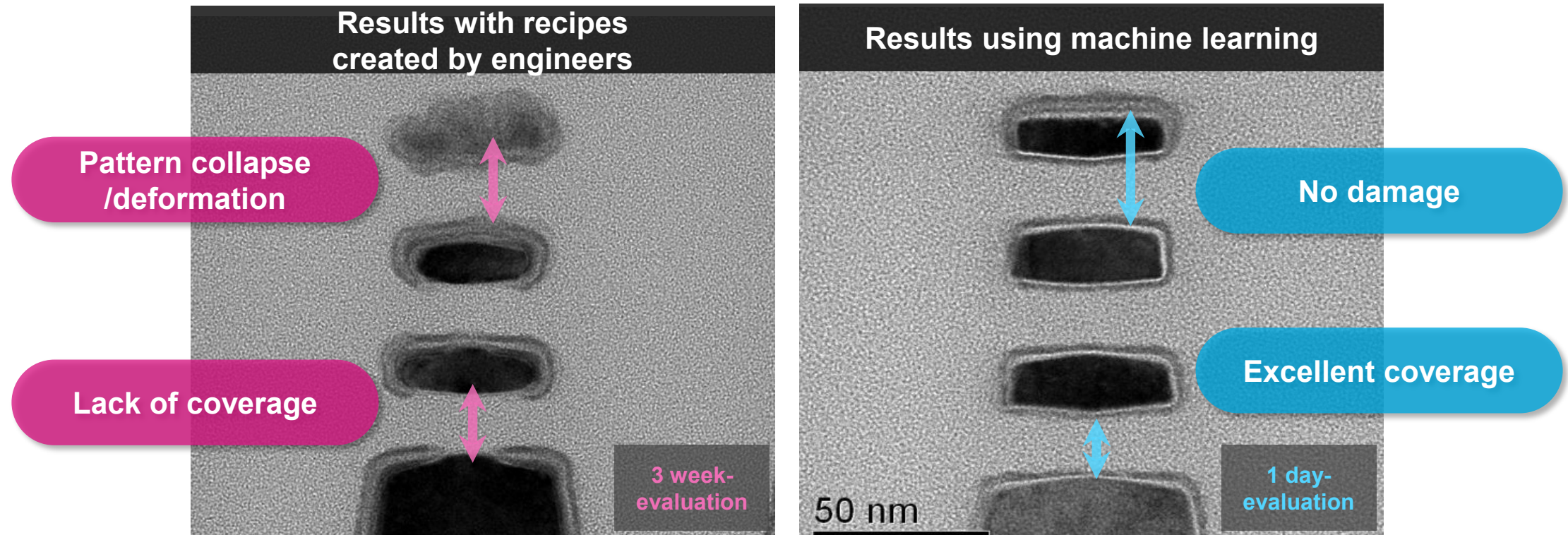
Leveraging DX in each step of Product Lifecycle



Developing digital enablers for use throughout Product Lifecycle (PLC)
to leverage productivity and profitability

Example Activity 1: Increasing Productivity of R&D

Process Informatics



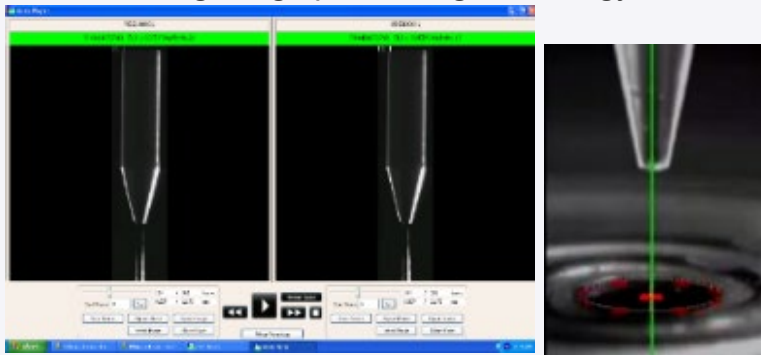
Source: Tokyo Electron Technology Solutions Limited / Tokyo Electron Limited

Achieved good step coverage with no pattern deformation
in the ALD process by machine learning

Example Activity 2: Increasing Operation Cost of Equipment

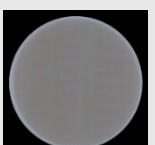
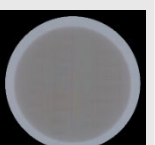
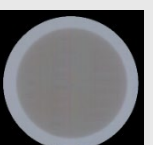
Reducing Chemicals of Coater/Developer

Monitoring of chemical discharge status
using image processing technology



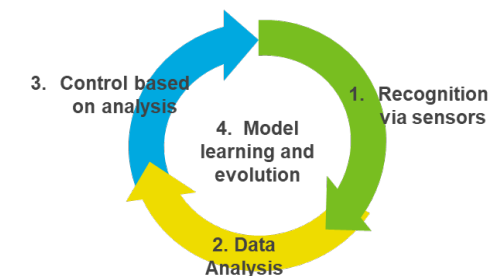
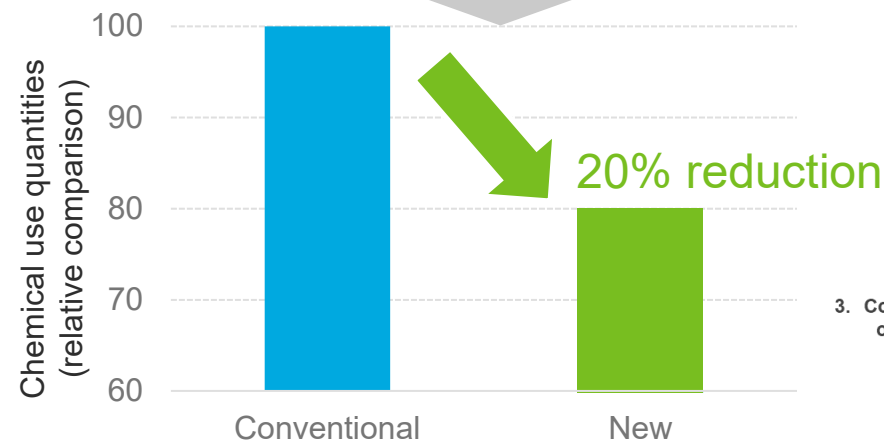
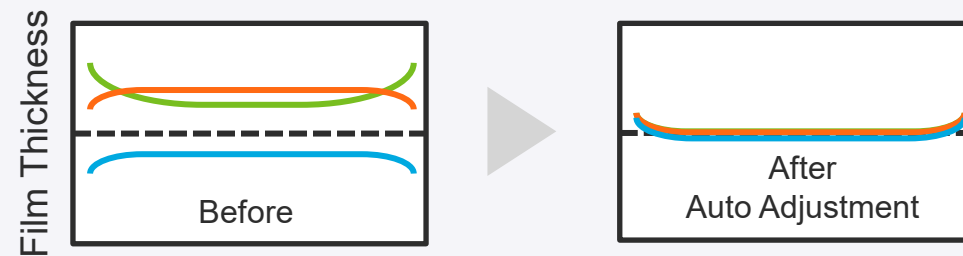
Source: TEL

Monitoring of chemical coverage of interior of surfaces
using image processing technology

Dispense Volume	X ml	Y ml	Z ml	A ml
Judgement	Passed	Passed	Failed	Failed
Wafer image				

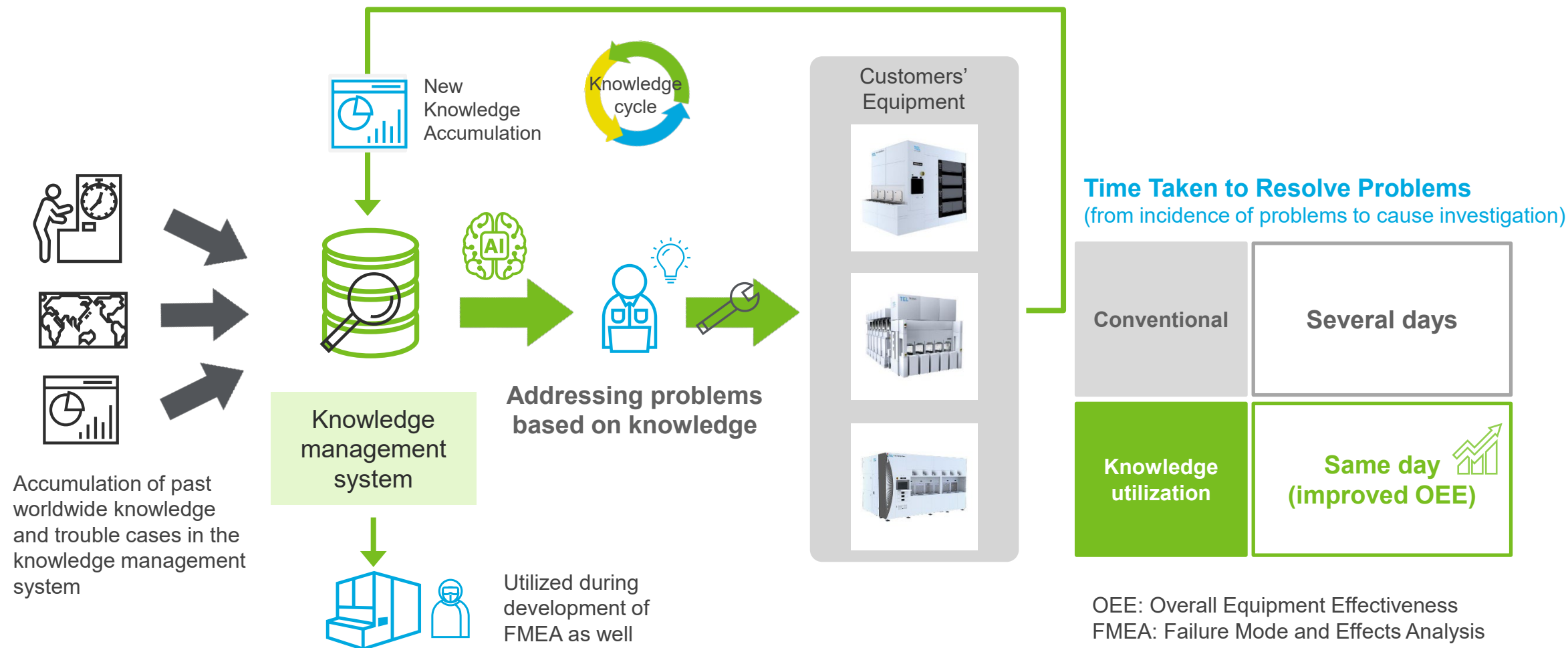
Source: TEL

Automatic film thickness adjustment function



Contributed to customer operation costs
and the environment by using machine learning

Example Activity 3: Improving Overall Equipment Effectiveness



Using the Knowledge Management System to reduce the time taken to resolve problems and improve equipment operation rates

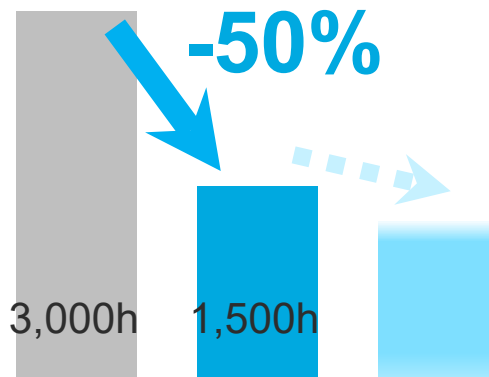
10. Procurement and Manufacturing Strategy

Continuous Production Innovation in Pursuit of Safety, High Quality and High Reliability

- Build a production system able to quickly respond to market changes
- Shorten time from new product development to mass production
- Shorten production lead times: Achieve 100% module shipment
- Utilize DX and automation in manufacturing, and expand automated warehouse
- **Significantly reduce equipment start-up time (One-touch start-up)**
 - Reduce start-up time up to 75% (primary target), One-touch (final target)



Shorten start-up time



Conventional → after production innovation

Expected outcome from shorten start-up time

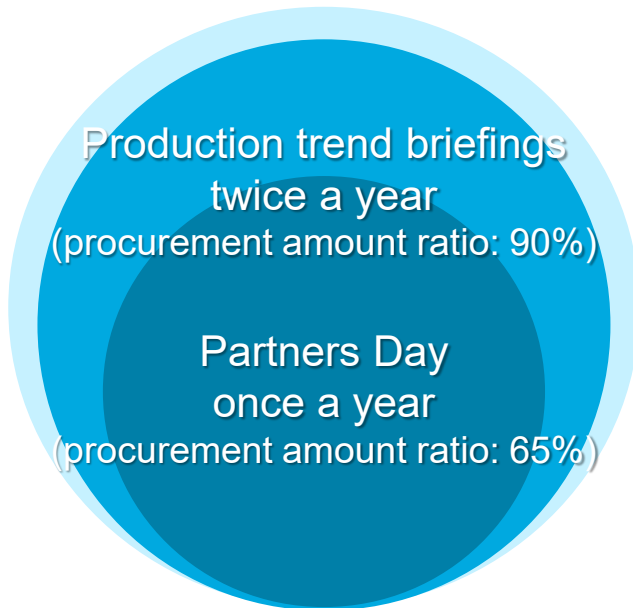
- Enhance productivity and start-up quality
- Reduce accident risks
- Optimize resources and the work-life balance

Build a Sustainable Supply Chain

- Fair and transparent relationships and reliable trust relationship with our business partners
 - Implement CSR/BCP assessments based on industry codes of conduct
 - Share knowledge in such areas as safety, quality, the environment and compliance



Source: United Nations Information Centre (<https://www.unice.or.jp/>)



E-COMPASS

Applaud environmental impact reduction activities, adding environmentally related items to assessment studies

- ✓ Reduce CO₂ emissions and the amount of energy usage
- ✓ Introduce renewable energy
- ✓ Promote resource conservation
- ✓ Promote waste reduction and recycling
- ✓ Promote activities for reducing the environmental impact of logistics



Procurement BCP and Proactive Procurement Activities

Mid- and long-term forecast
Promote “Shift Left” procurement strategy
Build BCP system resilient to procurement difficulty

Oversee whole supply chain from upstream to downstream
Visualize and grasp risks

Supply chain responsive to any kind of risks
(Raw materials, parts, processing and assembly)
Strong and reliable supply chain

**Safety stock
Inventory liquidity**

**Visualize
supply chain**

**Risk management on
business partners
Strengthen partnership**

Measures for procurement BCP

Early procurement of parts

- Early procurement for long term
- Ensure inventory exchange flexibility among factories
- Inventory reductions in total

Secure semiconductor devices

- Secure semiconductor devices for our equipment
 - Visualize and streamline distribution channel
 - Collaborate with semiconductor makers
- = TEL can be a customer of our customers

Parts and Suppliers

- Identify and analyze risk parts
- Multi sourcing of producing countries
- Standardization, centralization and decentralization of parts
- Measures to secure capacity for us

Smart Manufacturing to Achieve High Quality and Productivity

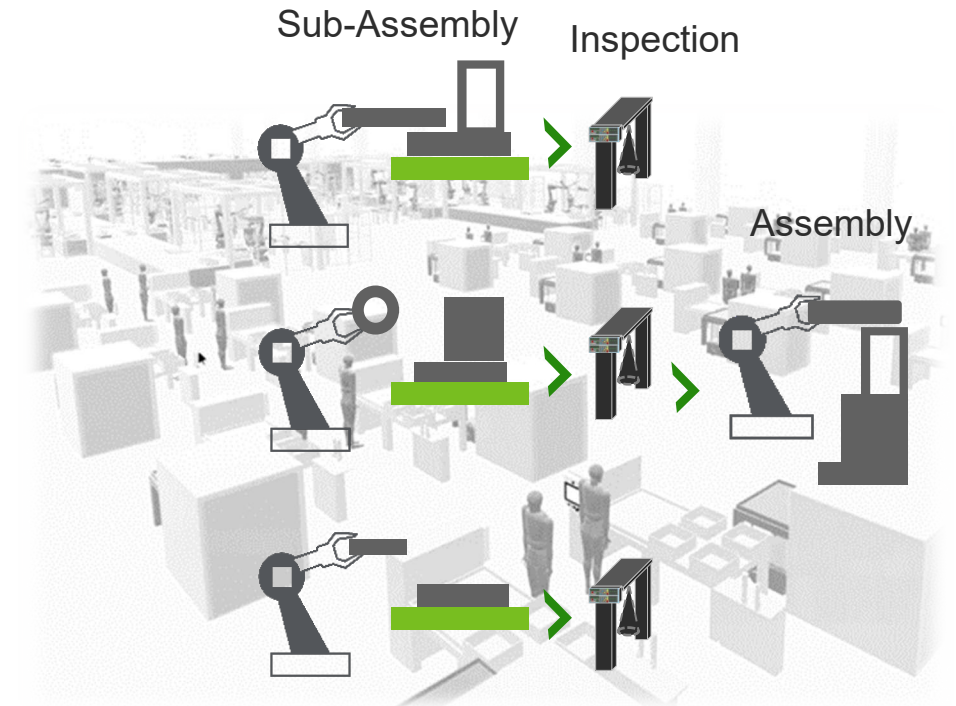
Development & Design



Feed Forward

Feedback

Smart Manufacturing



By centralizing development and production in TEL Miyagi,
we ensure continuous concurrent engineering and advanced manufacturing capabilities

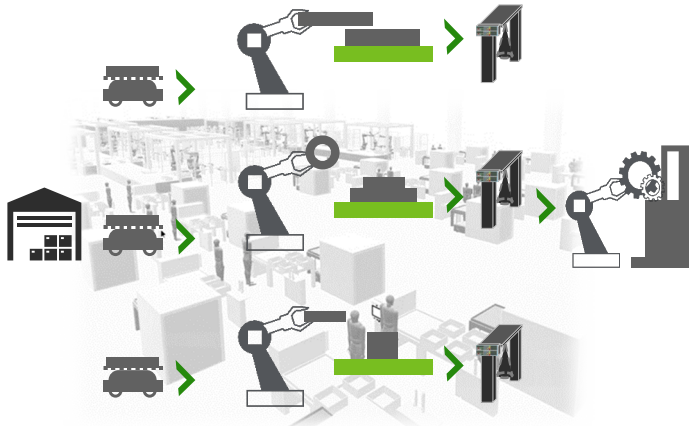
Source: TEL

Vision for Smart Production

- Achieve sustainable manufacturing for the future

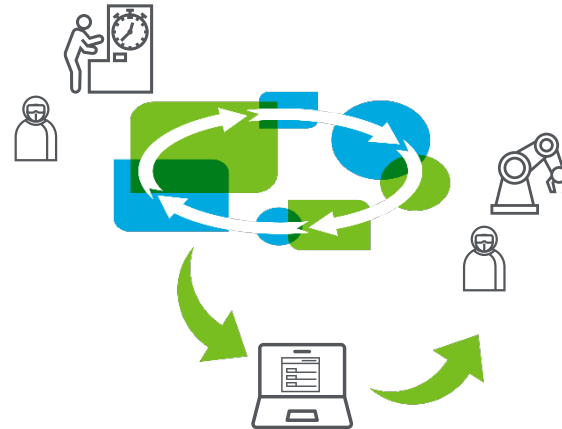
Overwhelming Efficiency

through automation
and standardization



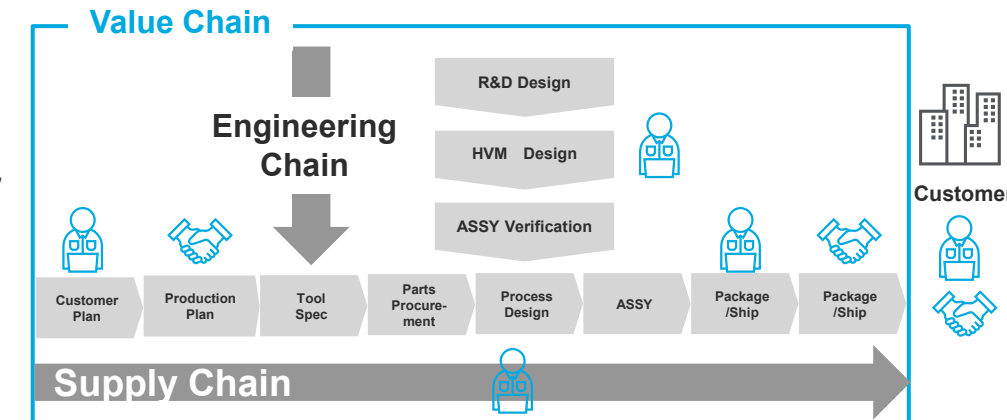
Enhancing Adaptability

to internal and external
environmental changes

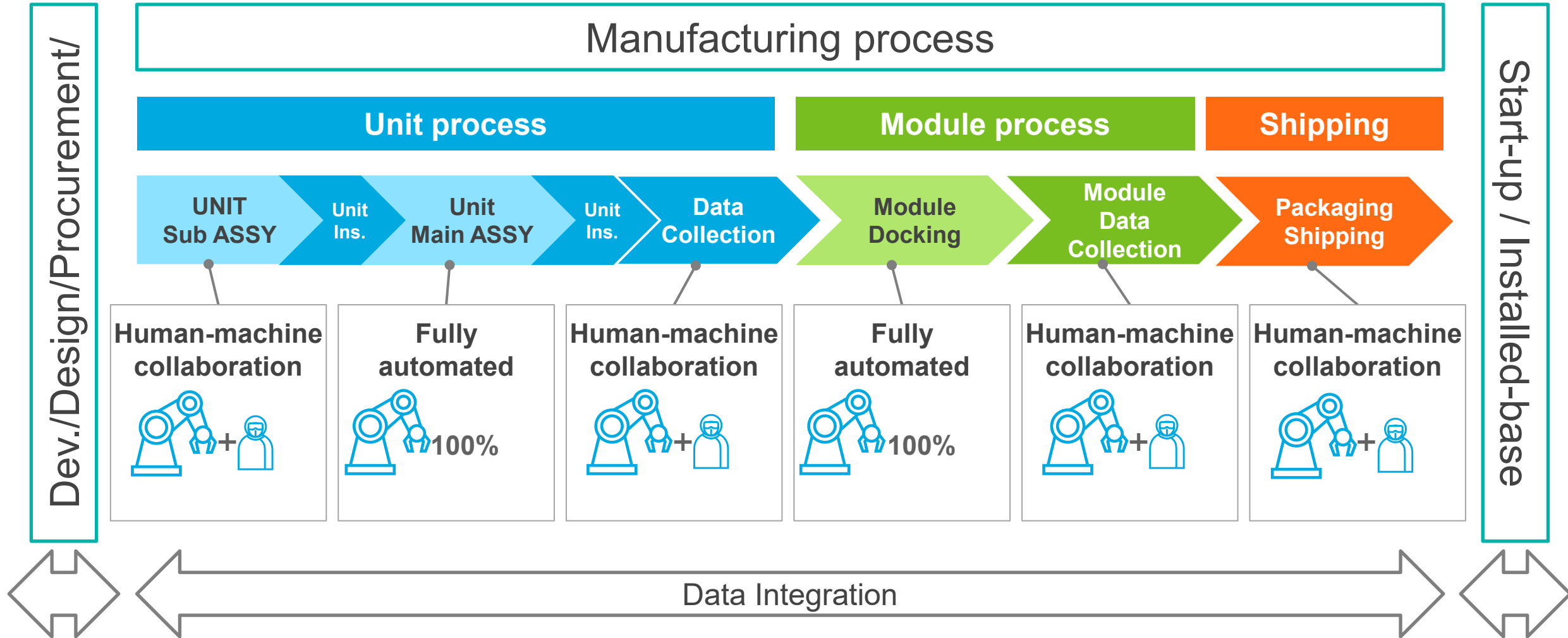


Product & Service Quality Improvement

through enhanced
value chain



Concept of Smart Production



Appendix: Data Section

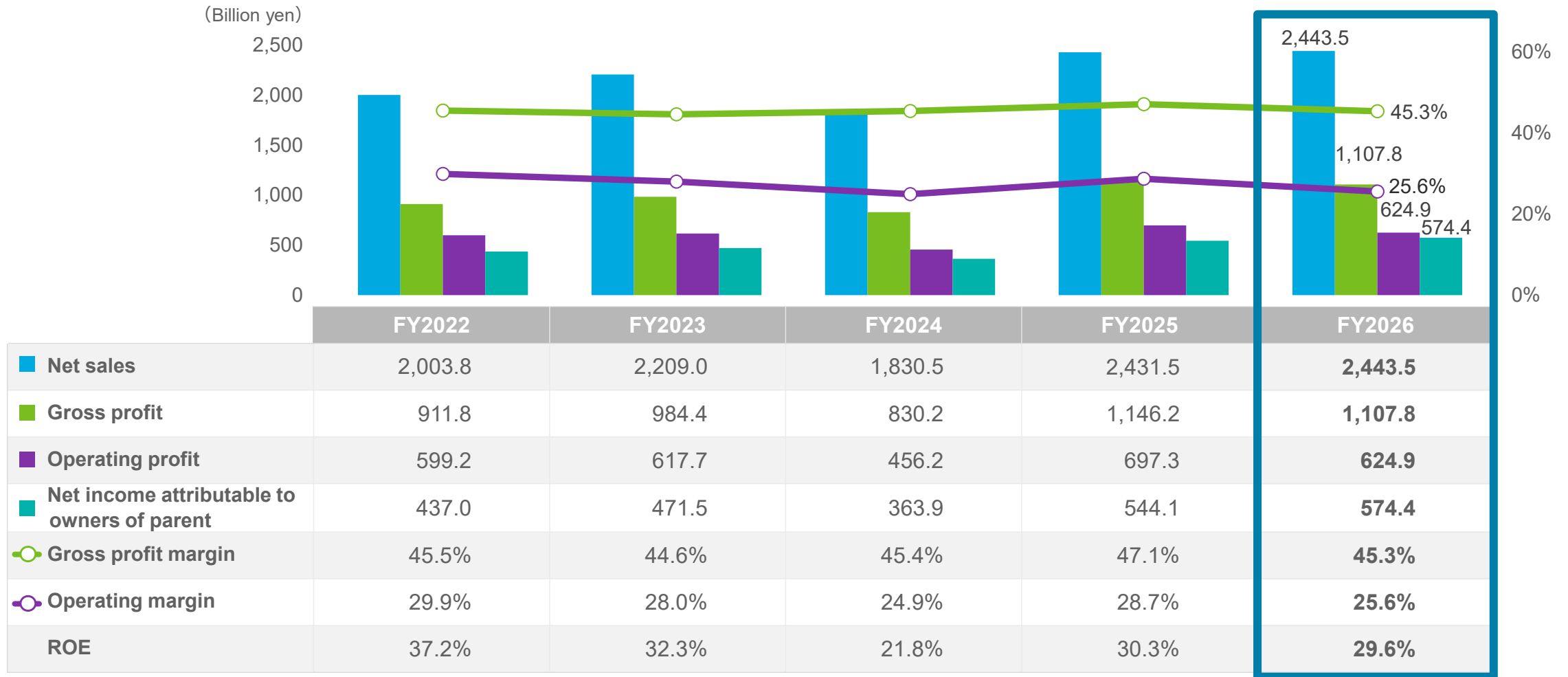
Financial Summary

	FY2025	FY2026	FY2026 vs FY2025	(Billion yen) Reference: FY2026 estimates announced on February 6, 2026
Net sales	2,431.5	2,443.5	+0.5%	2,410.0
Gross profit	1,146.2	1,107.8	-3.4%	1,092.0
Gross profit margin	47.1%	45.3%	-1.8pts	45.3%
SG&A expenses	448.9	482.9	+7.6%	499.0
Operating income	697.3	624.9	-10.4%	593.0
Operating margin	28.7%	25.6%	-3.1pts	24.6%
Income before income taxes	706.1	748.1	+6.0%	714.0
Net income attributable to owners of parent	544.1	574.4	+5.6%	550.0
EPS (Yen)	1,182.40	1,254.57	+6.1%	1,200.05
R&D expenses	250.0	277.8	+11.1%	290.0
Capital expenditures	162.1	216.0	+33.2%	240.0
Depreciation and amortization	62.1	80.9	+30.3%	86.0

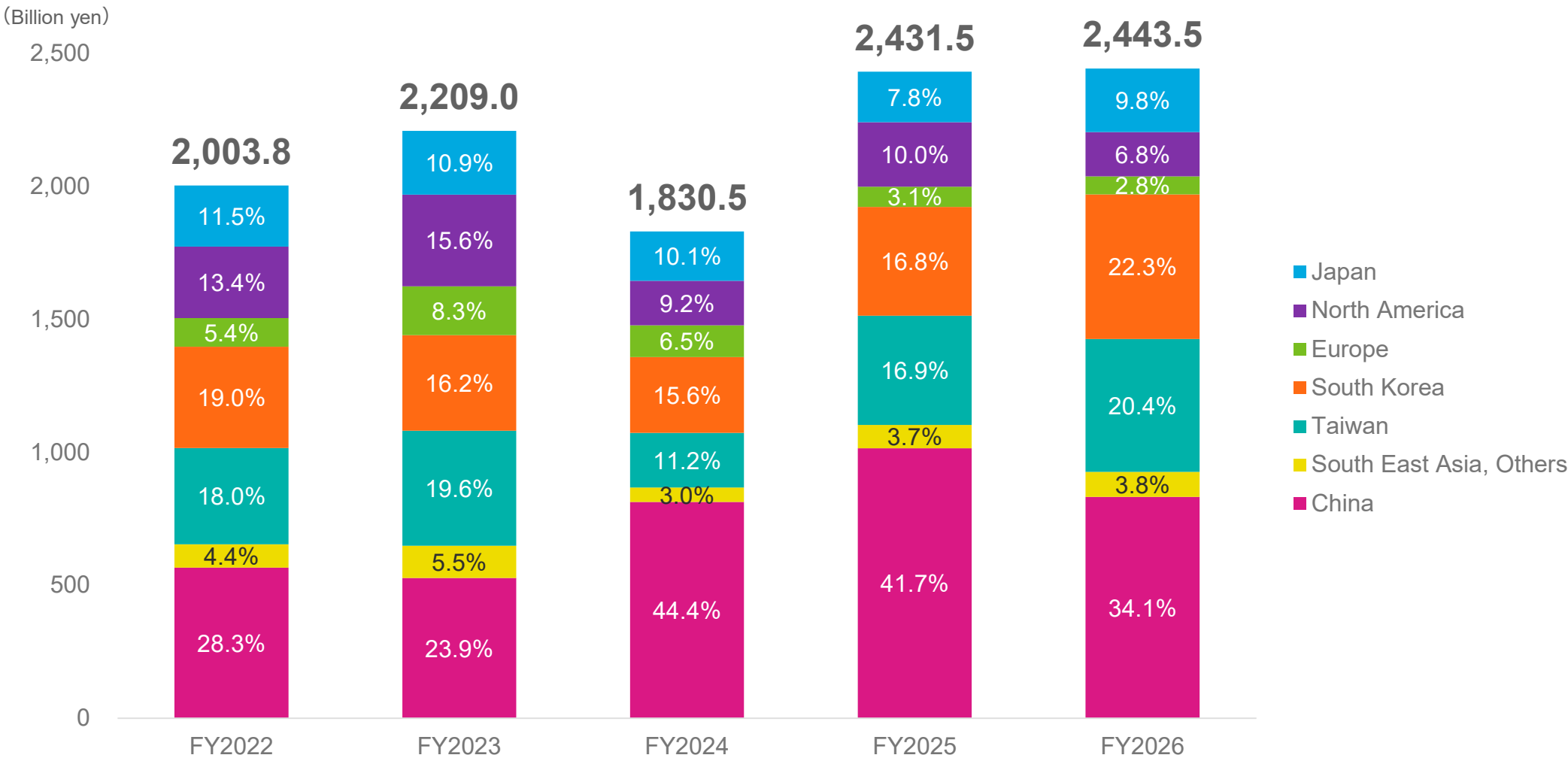
1. In principle, export sales of Tokyo Electron's products are denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of foreign exchange rate fluctuations on profits is negligible, unless extreme fluctuations occur.

2. Profit ratios are calculated using full amounts, before rounding.

Financial Trend



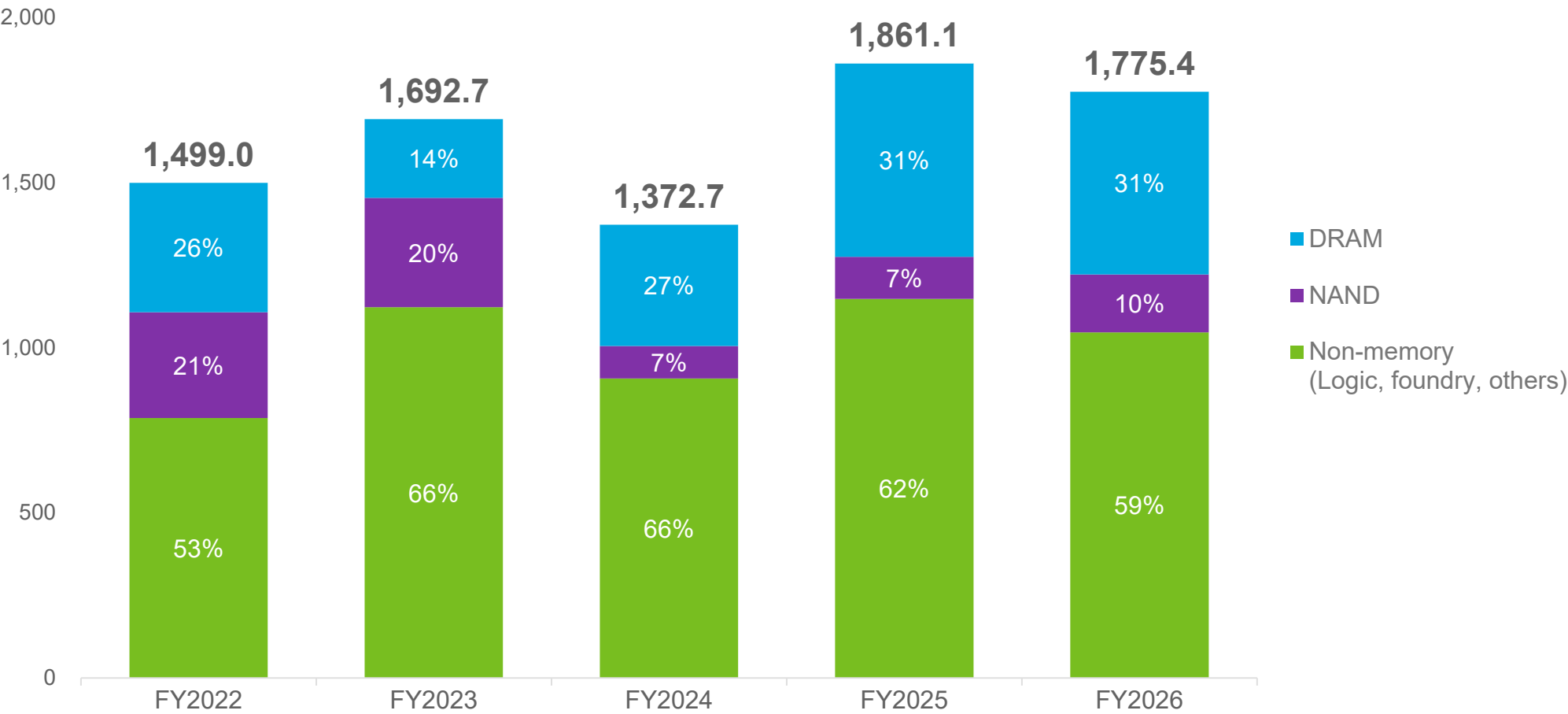
Sales by Region



1. SPE: Semiconductor Production Equipment
2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

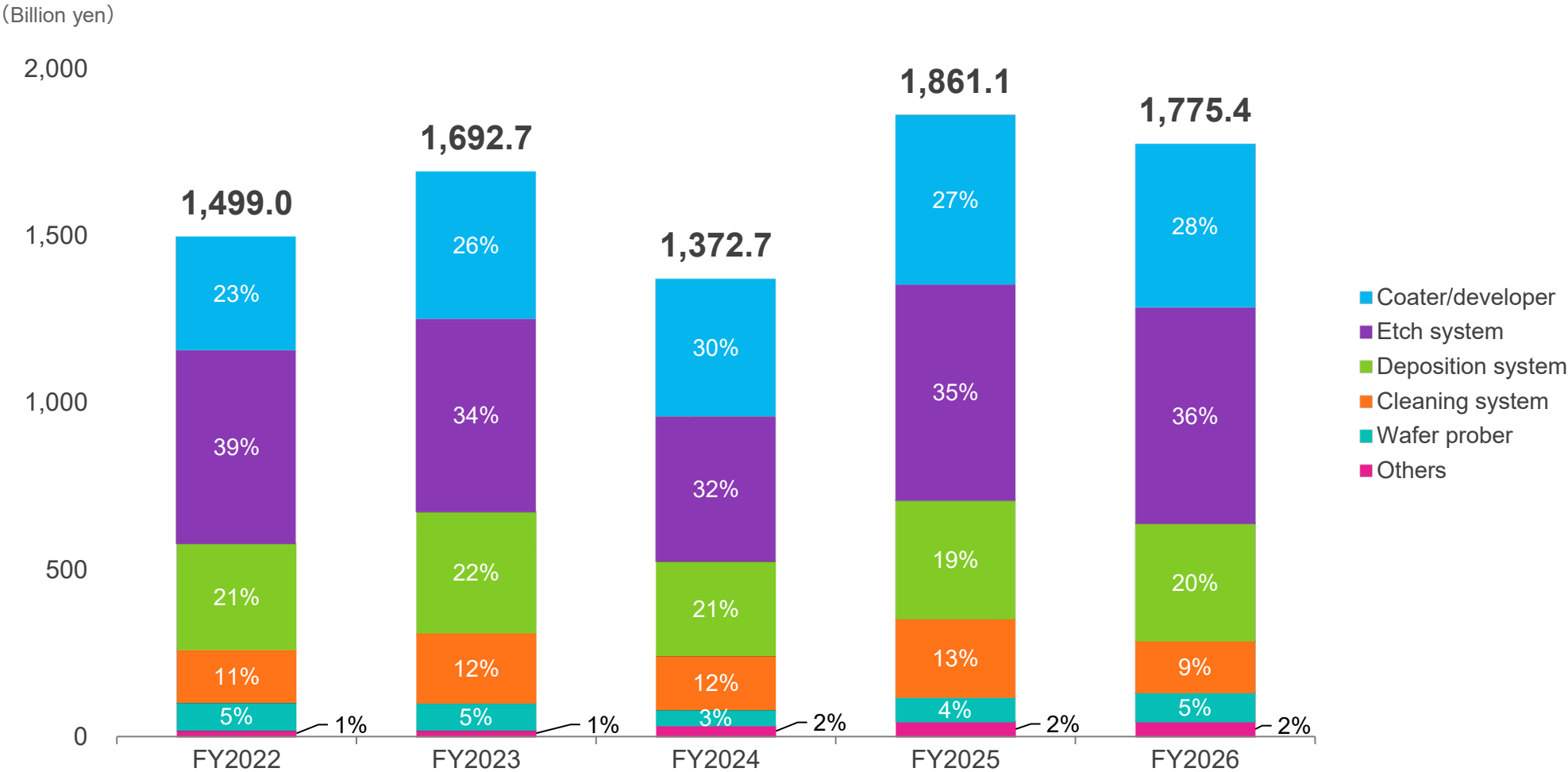
SPE New Equipment Sales by Application

(Billion yen)



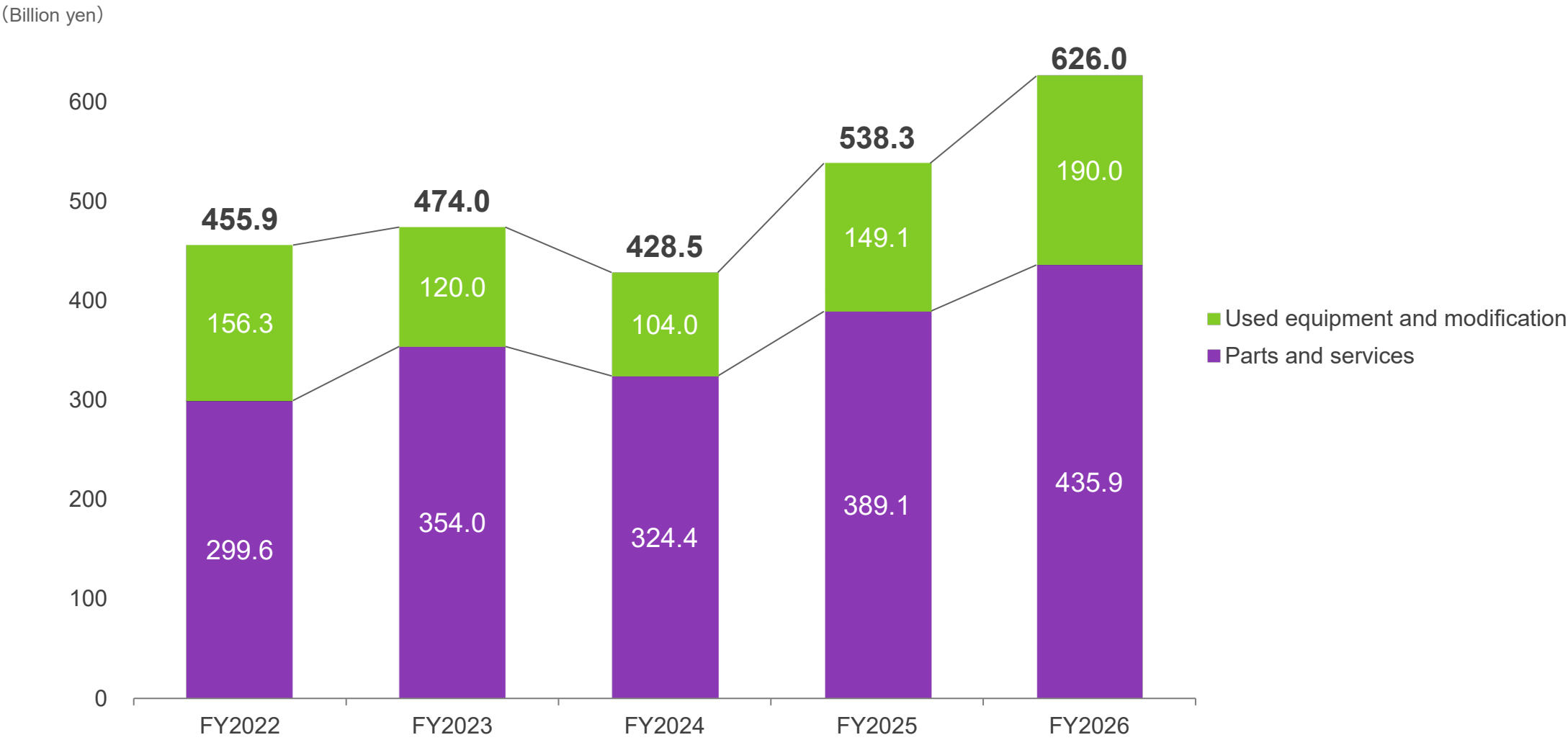
1. SPE: Semiconductor Production Equipment
 2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

SPE New Equipment Sales by Product



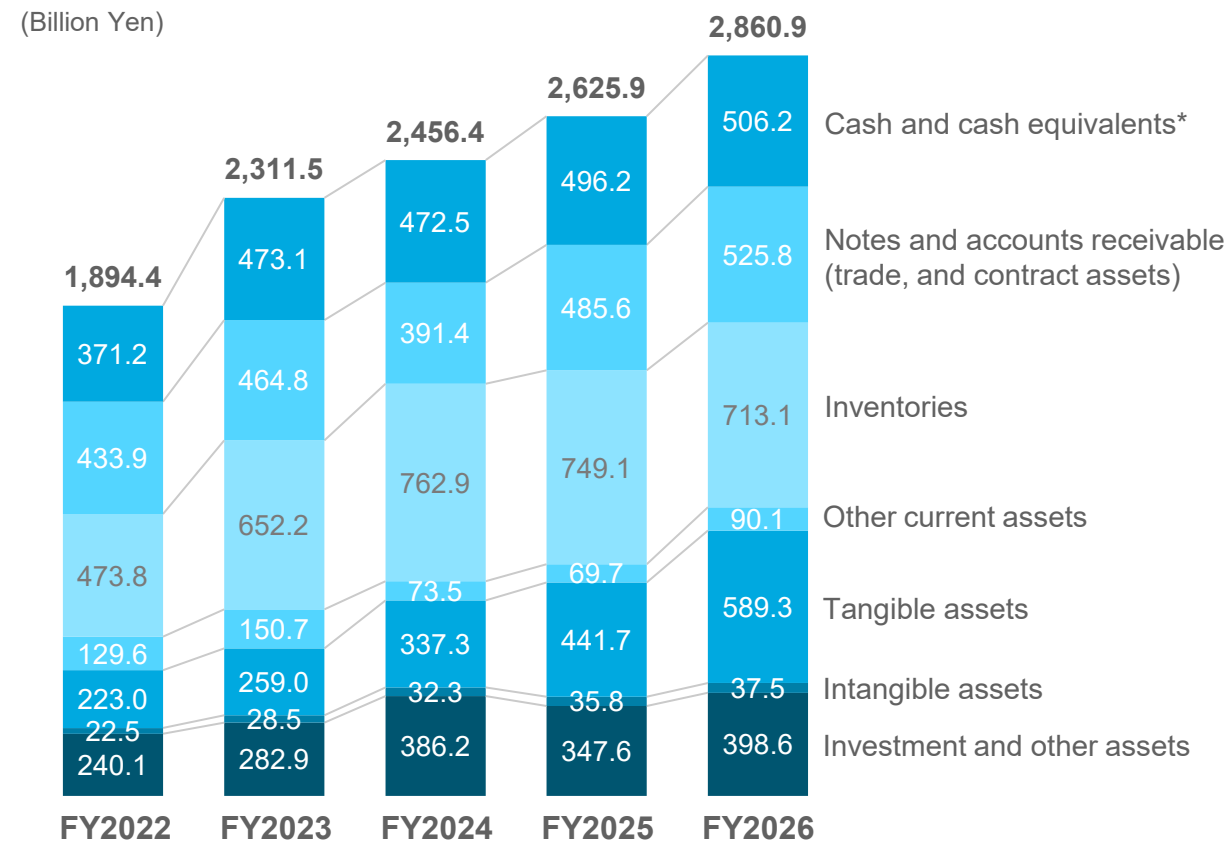
1. SPE: Semiconductor Production Equipment
 2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

Field Solutions Sales

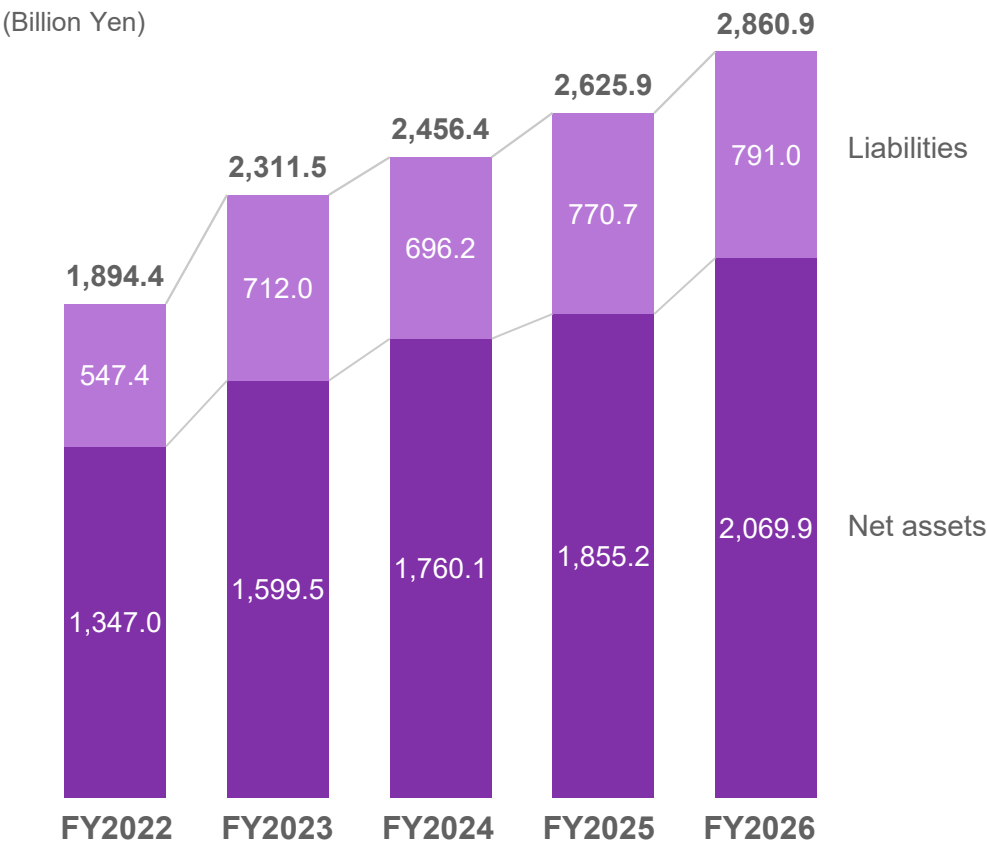


Balance Sheet

Assets

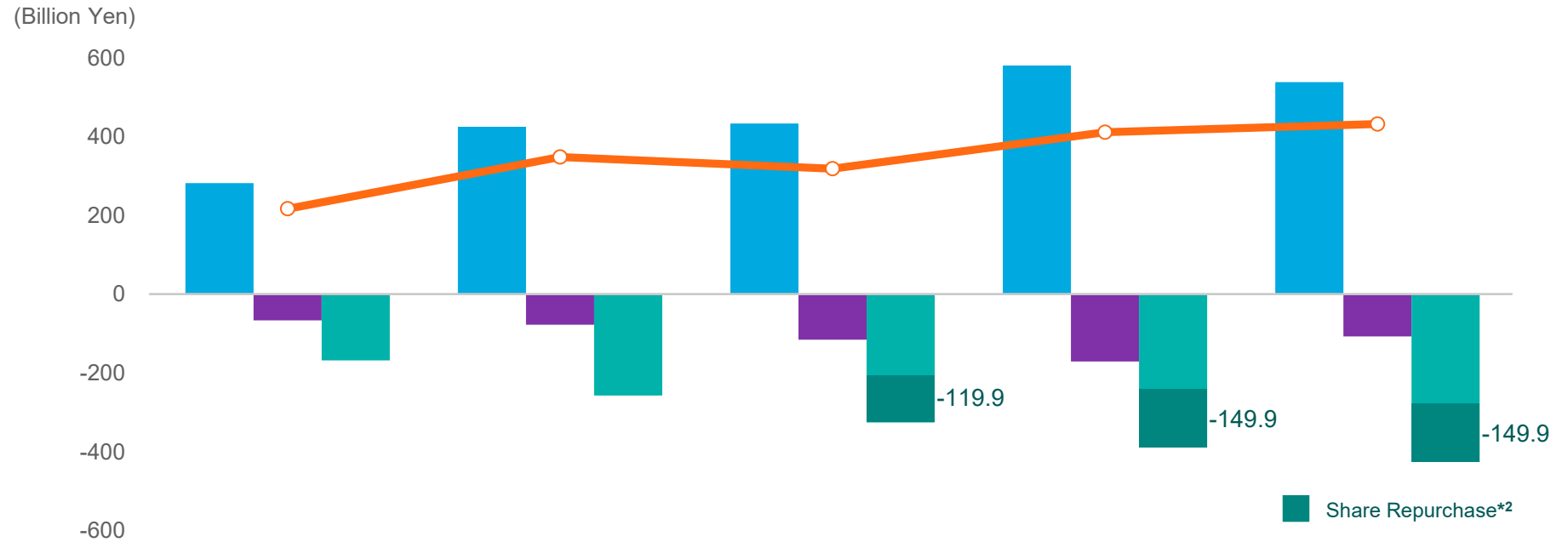


Liabilities and Net Assets



*Cash and cash equivalents: "Cash and deposits" + "Short-term investments", etc. ("Securities" in Balance Sheet).

Cash Flow



	FY2022	FY2023	FY2024	FY2025	FY2026
■ Cash flow from operating activities	283.3	426.2	434.7	582.1	539.7
■ Cash flow from investing activities*1	-65.6	-76.7	-115.0	-169.7	-106.4
■ Cash flow from financing activities	-167.2	-256.5	-325.0	-388.8	-425.3
○ Free cash flow*3	217.7	349.4	319.6	412.4	433.2
Cash on hand*4	371.2	473.1	472.5	496.2	506.2

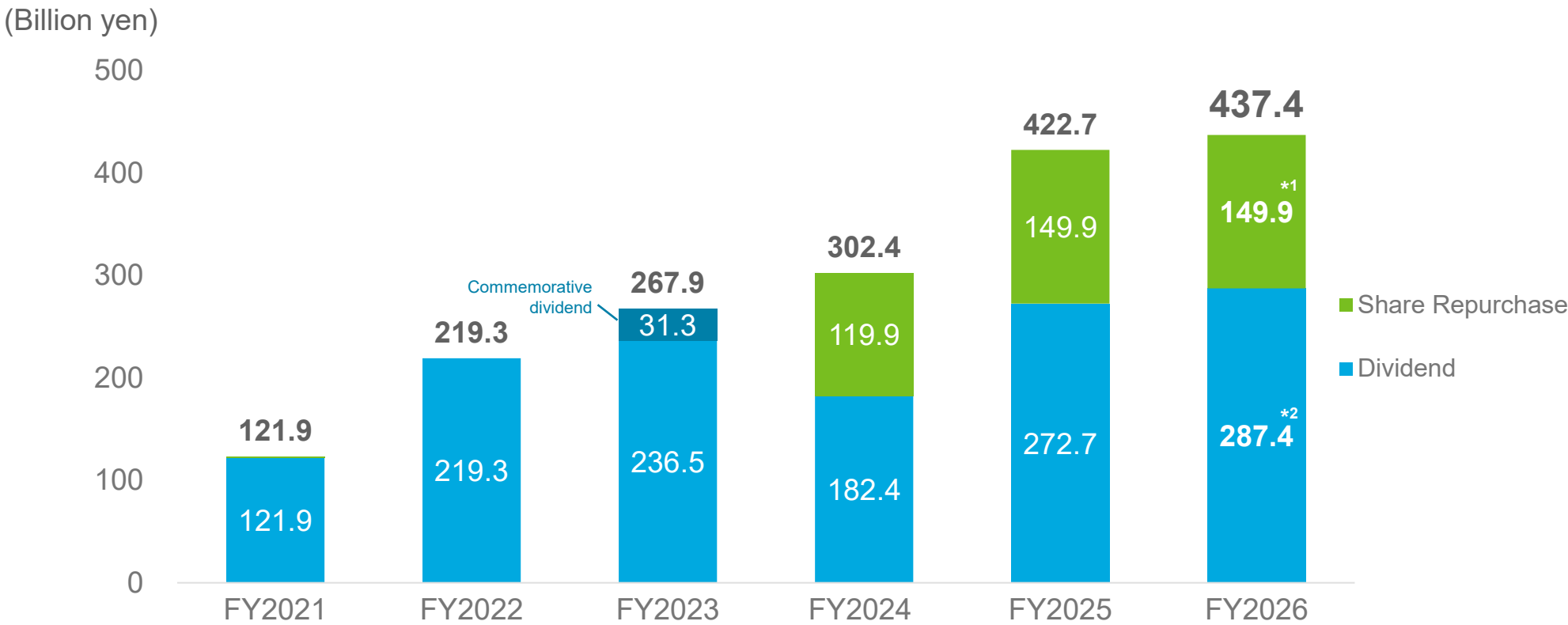
*1 Cash flow from investing activities excludes changes in time deposits and short-term investments.

*2 The amount for share repurchase excludes the cost incurred to purchase odd-lot shares.

*3 Free cash flow = "Cash flow from operating activities" + "Cash flow from investing activities" (excluding changes in "Time deposits" and "Short-term investments").

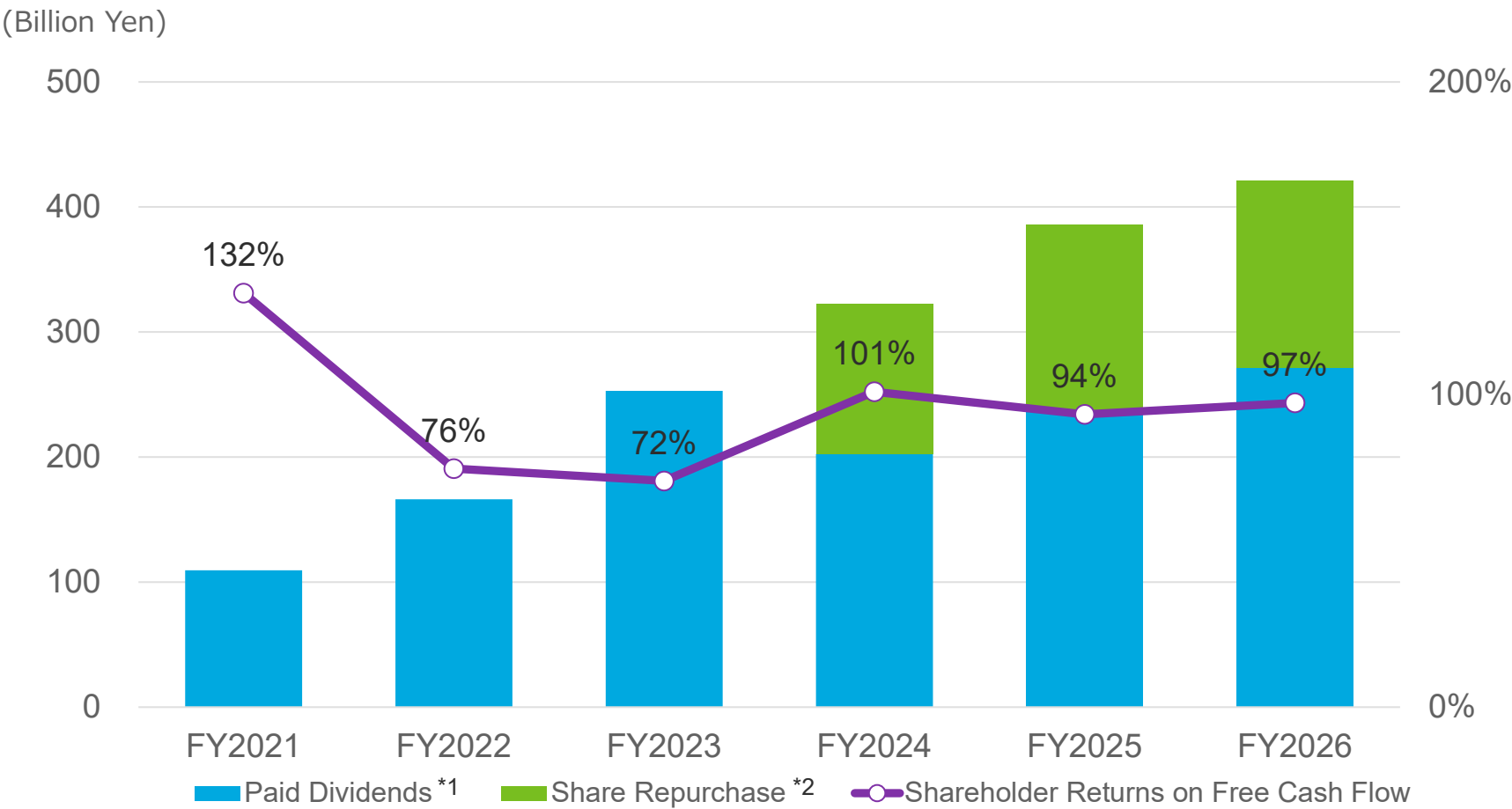
*4 Cash on hand includes "Cash and cash equivalents" + "Time deposits and short-term investments" with original maturities of more than three months.

Total Return Amount



^{*1} https://www.tel.com/news/ir/2026/kn008f00000000ho-att/20260327_002_e.pdf
^{*2} The year-end dividend for FY2026 is provisional and pending approval by the Board of Directors.

Shareholder Returns Trend



*1 Paid dividends are shown based on their payment date.
*2 The amount for share repurchase excludes the cost incurred to purchase odd-lot shares.

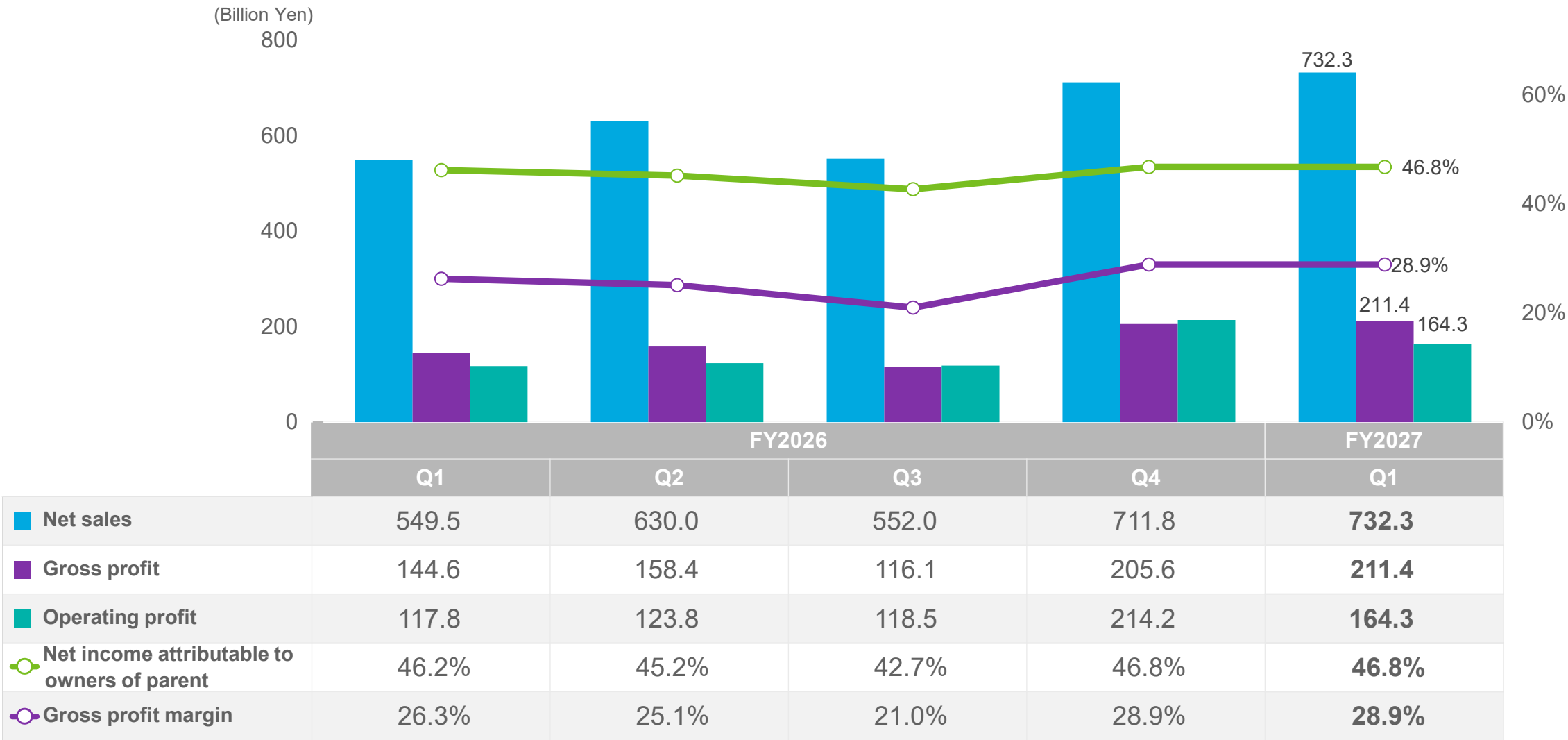
Financial Summary

(Billion yen)

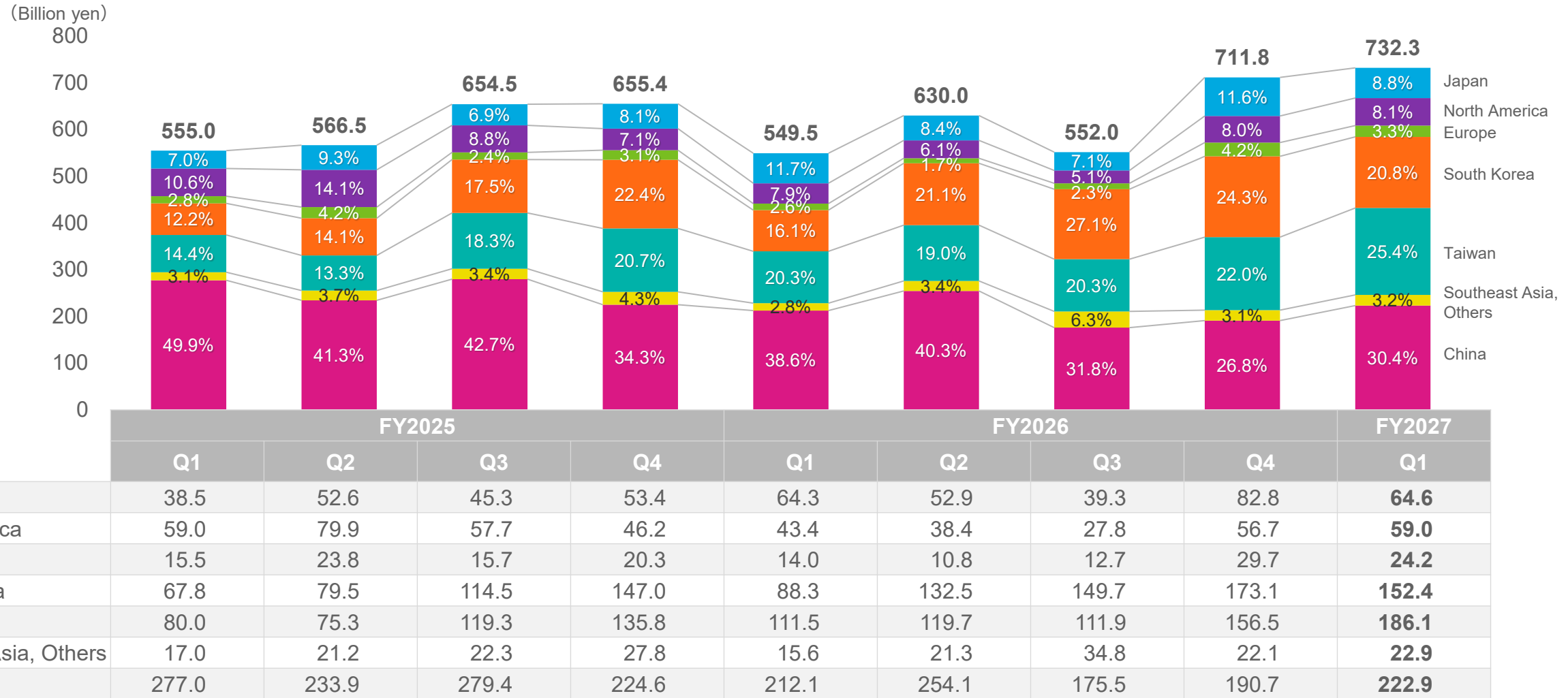
	FY2026				FY2027	vs. FY2026 Q4	vs. FY2026 Q1
	Q1	Q2	Q3	Q4	Q1		
Net sales	549.5	630.0	552.0	711.8	732.3	+2.9%	+33.3%
Gross profit	253.9	284.8	235.8	333.1	342.7	+2.9%	+34.9%
Gross profit margin	46.2%	45.2%	42.7%	46.8%	46.8%	±0.0pts	+0.6pts
SG&A expenses	109.2	126.4	119.6	127.5	131.3	+2.9%	+20.2%
Operating income	144.6	158.4	116.1	205.6	211.4	+2.8%	+46.1%
Operating margin	26.3%	25.1%	21.0%	28.9%	28.9%	±0.0pts	+2.6pts
Income before income taxes	151.9	161.0	153.3	281.8	215.4	-23.5%	+41.8%
Net income attributable to owners of parent	117.8	123.8	118.5	214.2	164.3	-23.3%	+39.5%
R&D expenses	62.1	72.6	66.2	76.7	72.0	-6.2%	+15.9%
Capital expenditures	52.8	91.2	30.3	41.6	39.9	-4.1%	-24.4%
Depreciation and amortization	17.1	19.1	21.1	23.5	22.5	-4.4%	+31.2%

1. In principle, export sales of Tokyo Electron's products are denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of foreign exchange rate fluctuations on profits is negligible, unless extreme fluctuations occur.
2. Profit ratios are calculated using full amounts, before rounding.
3. FY20xx refers to the financial year ending in March 20xx.

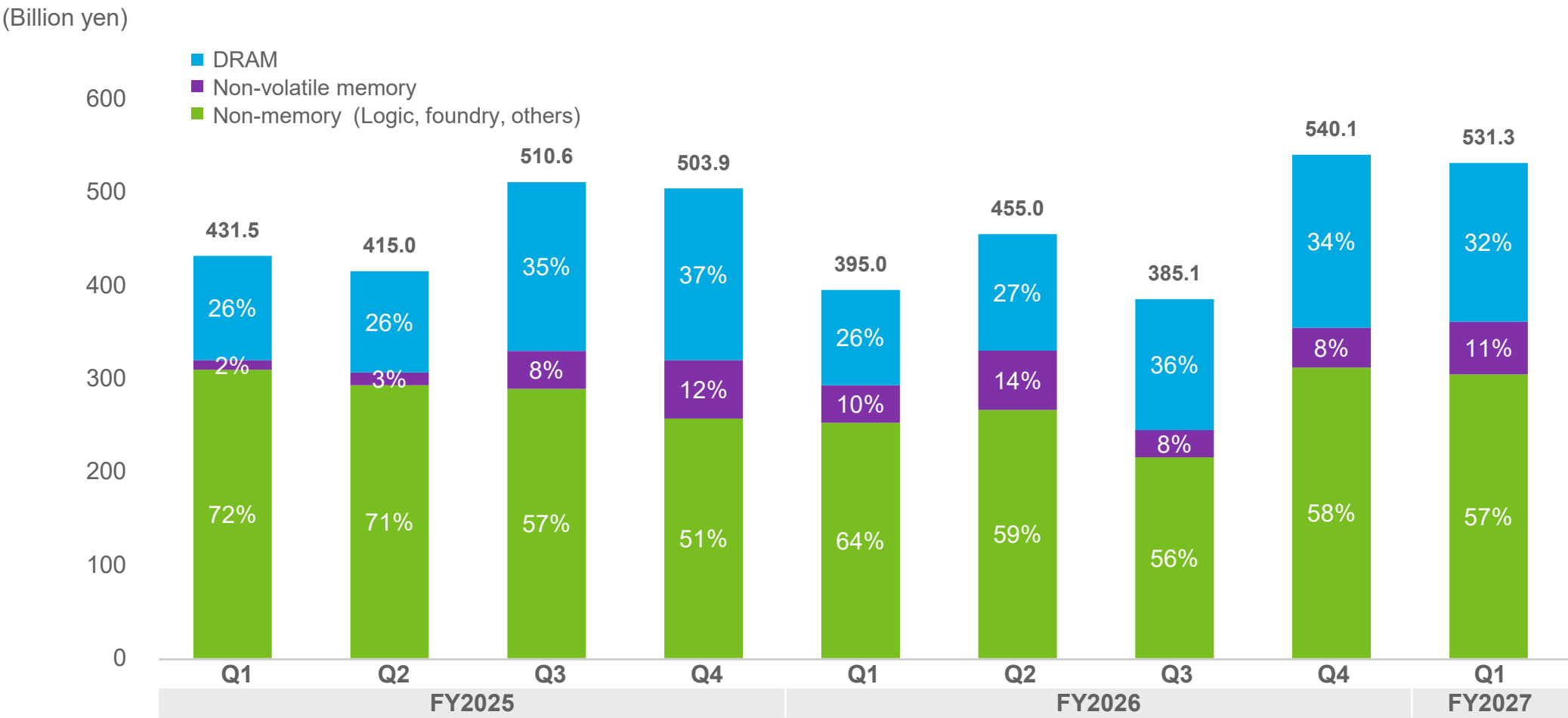
Financial Performance



Composition of Net Sales by Region

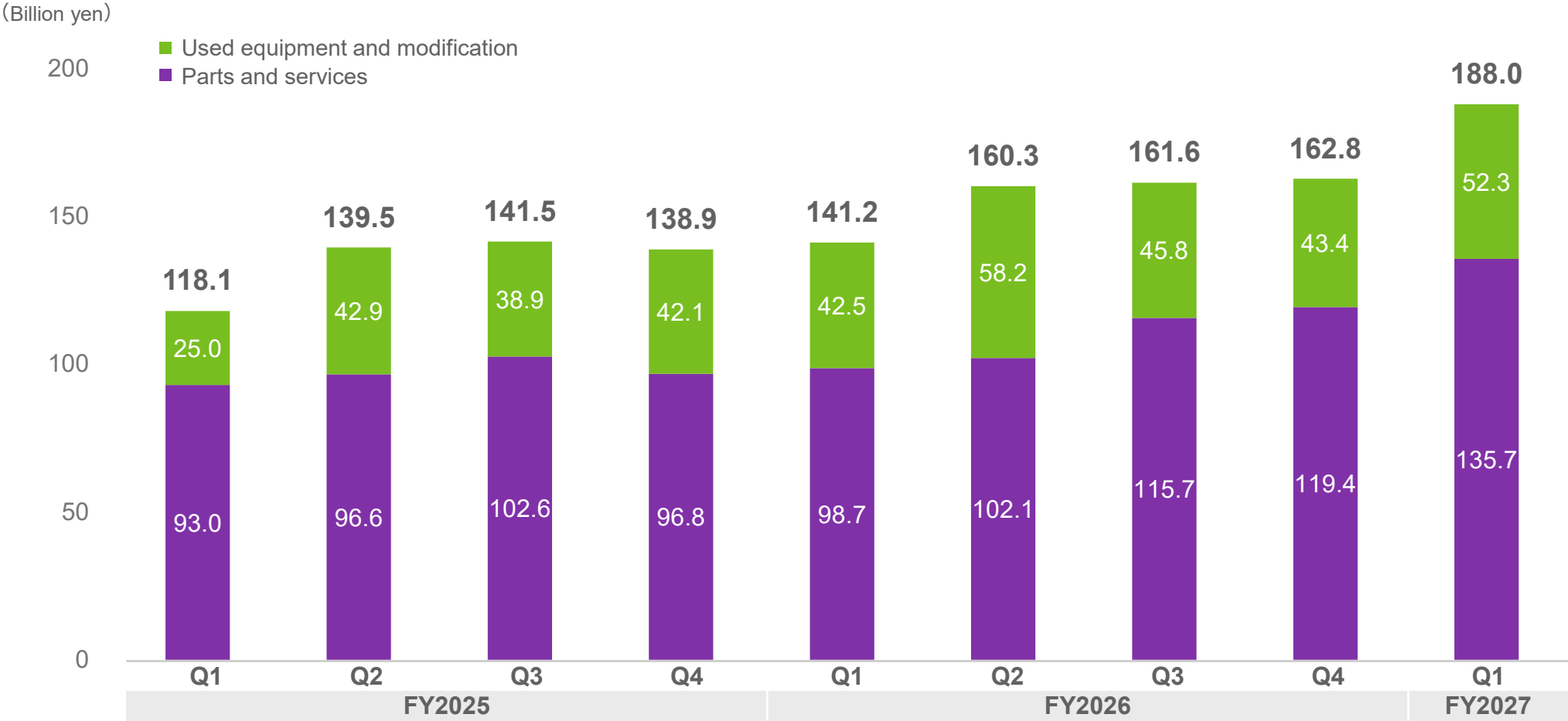


SPE New Equipment Sales by Application

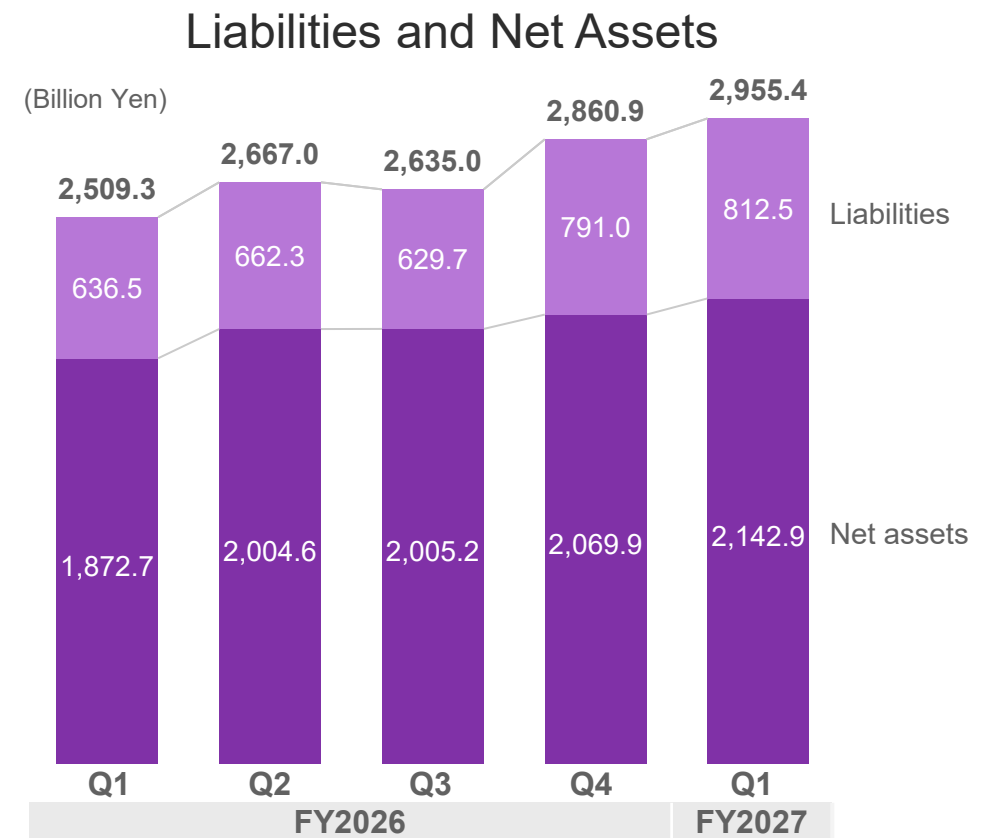
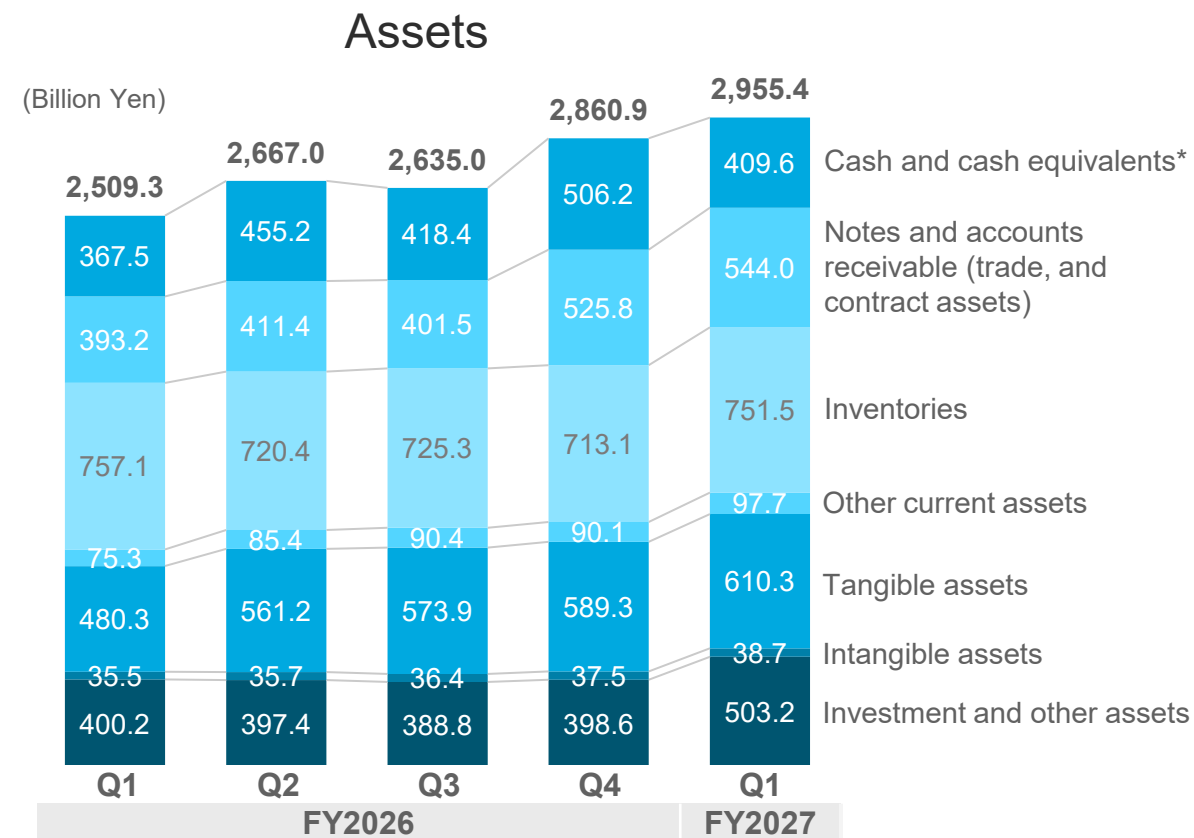


1. SPE: Semiconductor Production Equipment
2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

Field Solutions Sales

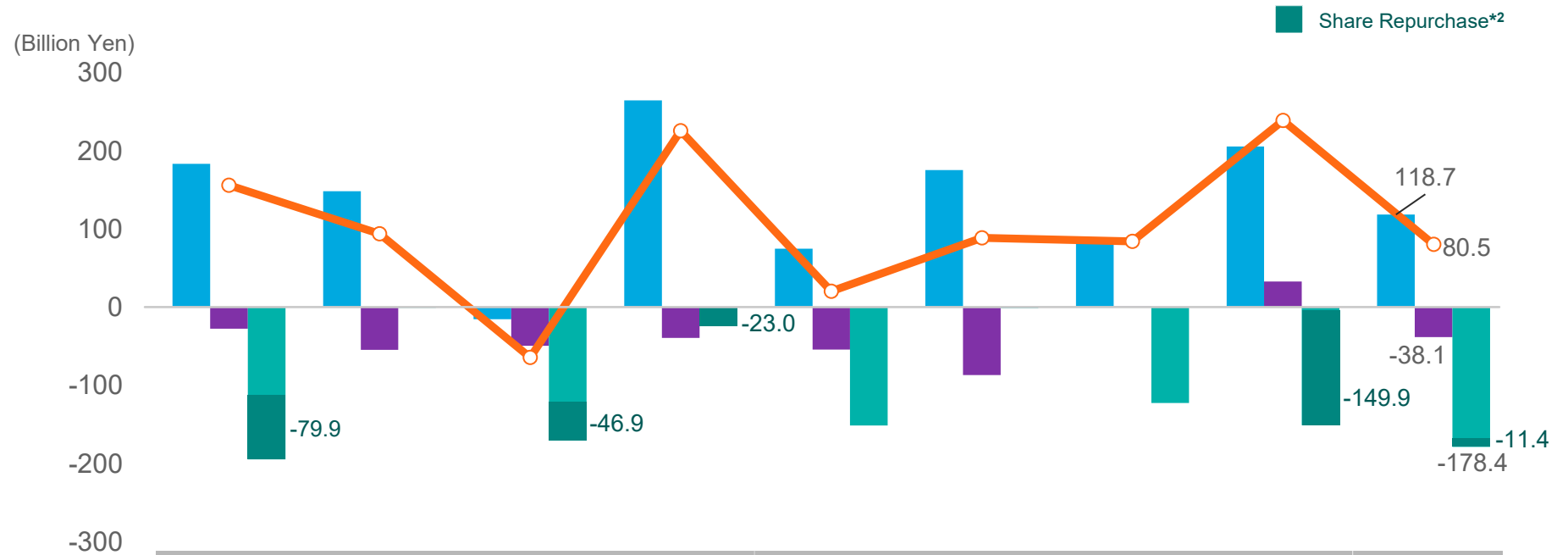


Balance Sheet



*Cash and cash equivalents: "Cash and deposits" + "Short-term investments", etc. ("Securities" in Balance Sheet).

Cash Flow



	FY2025				FY2026				FY2027
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1
■ Cash flow from operating activities	183.7	148.6	-15.0	264.8	74.9	175.8	83.1	205.7	118.7
■ Cash flow from investing activities*1	-27.3	-54.4	-49.0	-38.9	-54.1	-86.7	1.2	33.2	-38.1
■ Cash flow from financing activities	-194.4	-0.6	-170.1	-23.5	-151.1	-1.0	-122.3	-150.8	-178.4
○ Free cash flow*3	156.4	94.1	-64.1	225.8	20.7	89.1	84.3	239.0	80.5
Cash on hand*4	438.5	525.5	295.5	496.2	367.5	455.2	418.4	506.2	409.6

*1 Cash flow from investing activities excludes changes in time deposits and short-term investments.

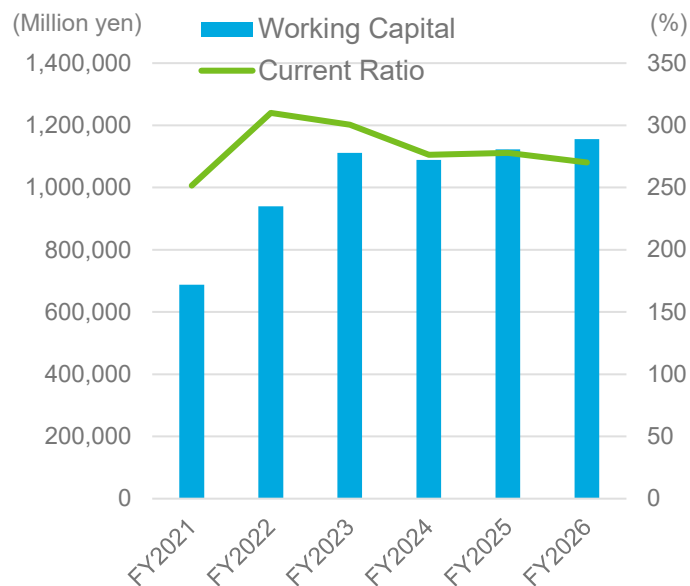
*2 The amount for share repurchase excludes the cost incurred to purchase odd-lot shares.

*3 Free cash flow = "Cash flow from operating activities" + "Cash flow from investing activities" (excluding changes in "Time deposits" and "Short-term investments").

*4 Cash on hand includes "Cash and cash equivalents" + "Time deposits and short-term investments" with original maturities of more than three months.

Asset Related Indices

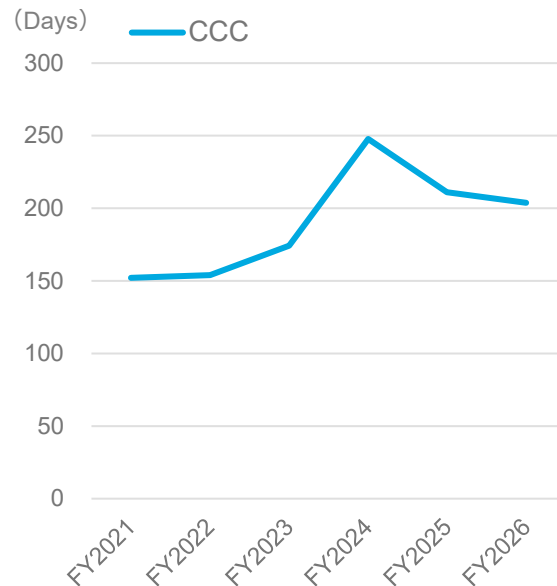
Working Capital and Current Ratio



	Working Capital (Million yen)	Current Ratio (%)
FY2021	688,035	310.0
FY2022	940,124	300.6
FY2023	1,111,065	276.4
FY2024	1,088,552	277.9
FY2025	1,122,830	265.6
FY2026	1,156,224	270.2

Working capital = Current assets - Current liabilities
Current ratio = Current assets / Current liabilities × 100

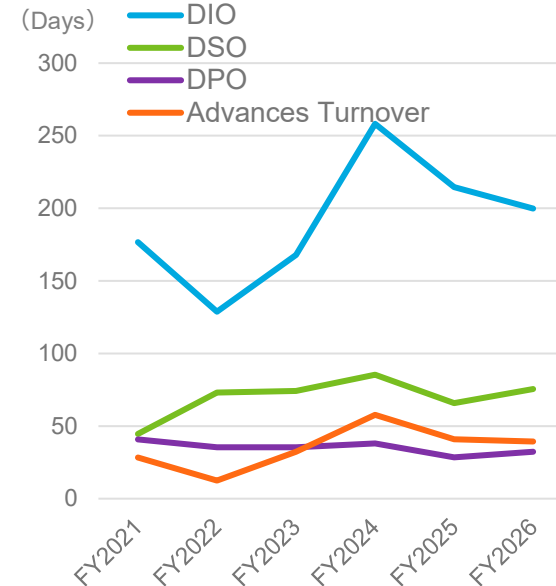
Cash Conversion Cycle (CCC)



	CCC (Days)
FY2021	152
FY2022	154
FY2023	174
FY2024	248
FY2025	211
FY2026	204

Cash conversion cycle
= DIO + DSO - Advances turnover - DPO

Inventory (DIO) / Receivable (DSO) / Payable (DPO) / Advances Turnover



	DIO (Days)	DSO (Days)	DPO (Days)	Advances (Days)
FY2021	177	45	41	28
FY2022	129	73	35	12
FY2023	168	74	35	32
FY2024	258	85	38	58
FY2025	215	66	28	41
FY2026	200	76	32	39

DIO = Average inventories / Cost of goods sold *365
DSO = Average accounts receivable* / Revenue *365
*Accounts receivable includes contract assets
DPO = Accounts payable / Cost of goods sold *365
Advances turnover = Average advances received / Revenue *365

*From the beginning of FY2022, the Company applies "Accounting Standard for Revenue Recognition" (ASBJ Statement No. 29).

Consolidated 10-year Financial Summary

(Millions of yen)

	FY2017	FY2018	FY2019	FY2020	FY2021	FY2022	FY2023	FY2024	FY2025	FY2026
Net sales	799,719	1,130,728	1,278,240	1,127,286	1,399,102	2,003,805	2,209,025	1,830,527	2,431,568	2,443,533
Gross profit	322,291	475,032	526,183	451,941	564,945	911,822	984,408	830,269	1,146,287	1,107,880
Gross profit margin	40.3%	42.0%	41.2%	40.1%	40.4%	45.5%	44.6%	45.4%	47.1%	45.3%
SG&A expenses	166,594	193,860	215,612	214,649	244,259	312,551	366,684	374,006	448,967	482,944
Operating income	155,697	281,172	310,571	237,292	320,685	599,271	617,723	456,263	697,319	624,936
Operating margin	19.5%	24.9%	24.3%	21.0%	22.9%	29.9%	28.0%	24.9%	28.7%	25.6%
Ordinary income	157,549	280,737	321,662	244,979	322,103	601,724	625,185	463,185	707,727	630,338
Income before income taxes	149,116	275,242	321,508	244,626	317,038	596,698	624,856	473,439	706,114	748,180
Net income attributable to owners of parent	115,208	204,371	248,228	185,206	242,941	437,076	471,584	363,963	544,133	574,454
R&D expenses	83,800	97,103	113,980	120,268	136,648	158,256	191,196	202,873	250,017	277,866
Capital expenditures	20,697	45,603	49,754	54,666	53,868	57,288	74,432	121,841	162,171	216,063
Depreciation and amortization	17,872	20,619	24,323	29,107	33,843	36,727	42,927	52,339	62,148	80,982
Interest-bearing debt	-	-	-	-	-	-	-	-	-	-
Equity	643,094	767,146	880,748	819,301	1,012,977	1,335,152	1,587,595	1,746,835	1,839,929	2,046,298
Total assets	957,447	1,202,796	1,257,627	1,278,495	1,425,364	1,894,457	2,311,594	2,456,462	2,625,981	2,860,997
Debt-to-equity ratio	-	-	-	-	-	-	-	-	-	-
Equity ratio	67.2%	63.8%	70.0%	64.1%	71.1%	70.5%	68.7%	71.1%	70.1%	71.5%
ROE	19.1%	29.0%	30.1%	21.8%	26.5%	37.2%	32.3%	21.8%	30.3%	29.6%
Cash flow from operating activities	136,948	186,582	189,572	253,117	145,888	283,387	426,270	434,720	582,174	539,732
Cash flow from investing activities	-28,893	-11,833	-84,033	15,951	-18,274	-55,632	-41,756	-125,148	-169,609	-96,492
Cash flow from financing activities	-39,380	-82,549	-129,761	-250,374	-114,525	-167,256	-256,534	-325,012	-388,836	-425,359
Net income per share (Yen)	234.09	415.16	504.53	390.19	520.73	935.95	1,007.82	783.75	1,182.40	1,254.57
Cash dividends per share (Yen)	117.00	208.00	253.00	196.00	260.00	468.00	570.00	393.00	592.00	628.00
Number of employees	11,241	11,946	12,742	13,837	14,479	15,634	17,204	17,702	19,573	20,236

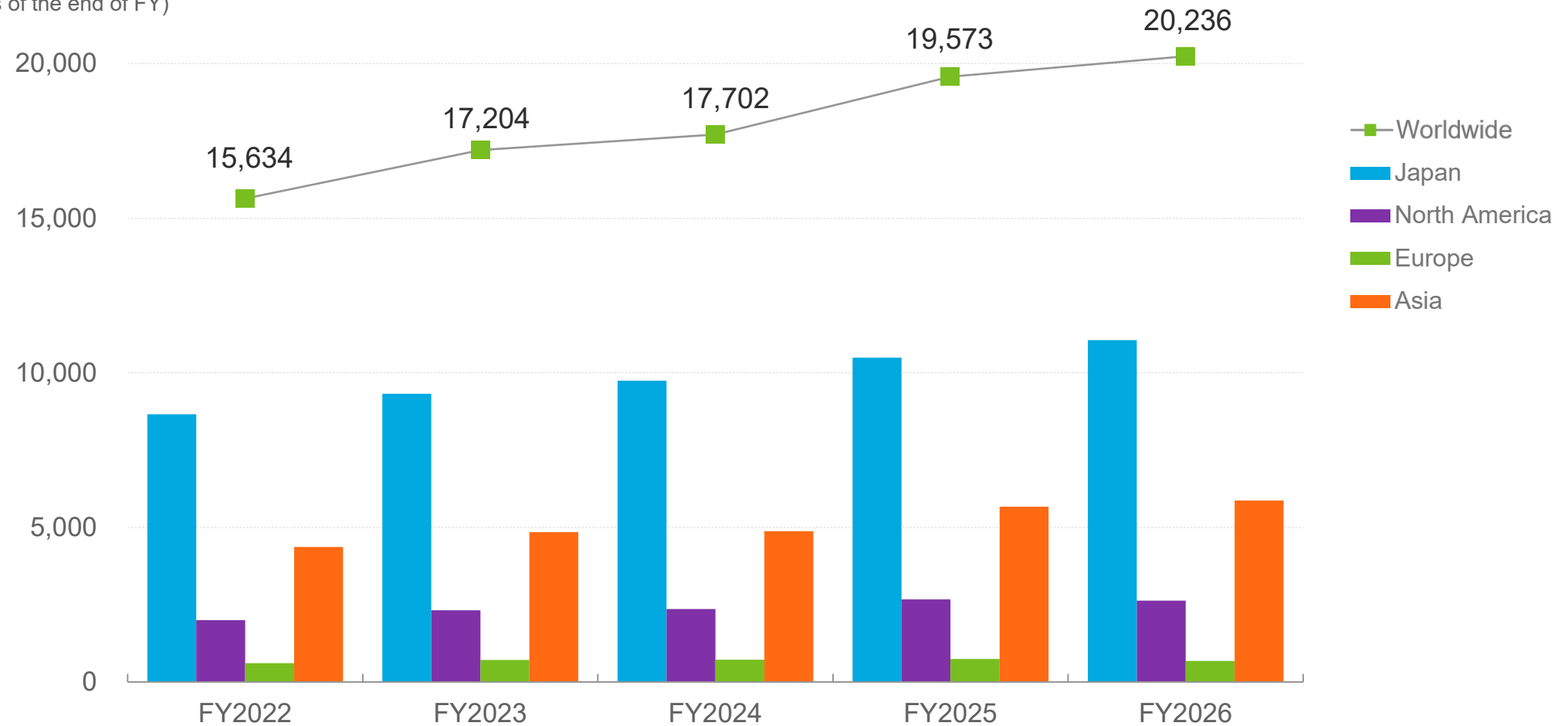
1. From FY2019, the Company adopts "Partial Amendments to Accounting Standard for Tax Effect Accounting" (ASBJ Statement No. 28, revision on February 16, 2018). "Total assets" and "equity ratio" for FY2018 have been restated in the table in accordance with the revised accounting standard.

2. From the beginning of FY2022, the Company applies "Accounting Standard for Revenue Recognition" (ASBJ Statement No. 29).

3. The Company implemented a 3-for-1 common stock split on April 1, 2023. Net income per share and dividend per share (yen) are the figures after the stock split.

Worldwide Employees

(Number of Employees
as of the end of FY)



- Disclaimer regarding forward-looking statements

Forward-looking statements with respect to TEL's business plan, prospects and other such information are based on information available at the time of publication. Actual performance and results may differ significantly from the business plan described here due to changes in various external and internal factors, including political and economic situations, semiconductor market conditions, intensification of sales competition, safety and product quality management, intellectual property-related matters and impacts from infectious diseases.

- Processing of numbers

For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.

- Foreign exchange risk

In principle, export sales of Tokyo Electron's products is denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of foreign exchange rate fluctuations on profits is negligible, unless extreme fluctuations occur.

- Disclaimer regarding Gartner data (Page 7, 12)

All statements in this presentation attributable to Gartner represent Tokyo Electron's interpretation of data, research opinion or viewpoints published as part of a syndicated subscription service by Gartner, Inc., and have not been reviewed by Gartner. Each Gartner publication speaks as of its original publication date (and not as of the date of this presentation). The opinions expressed in Gartner publications are not representations of fact, and are subject to change without notice.

Notice

You may not copy or disclose to any third party without prior written consent with TEL.

Tokyo Electron

TEL and “TEL” are trademarks of Tokyo Electron Limited.



TOKYO ELECTRON