Investors’ Guide

May 9, 2025

Tokyo Electron Limited

Contents

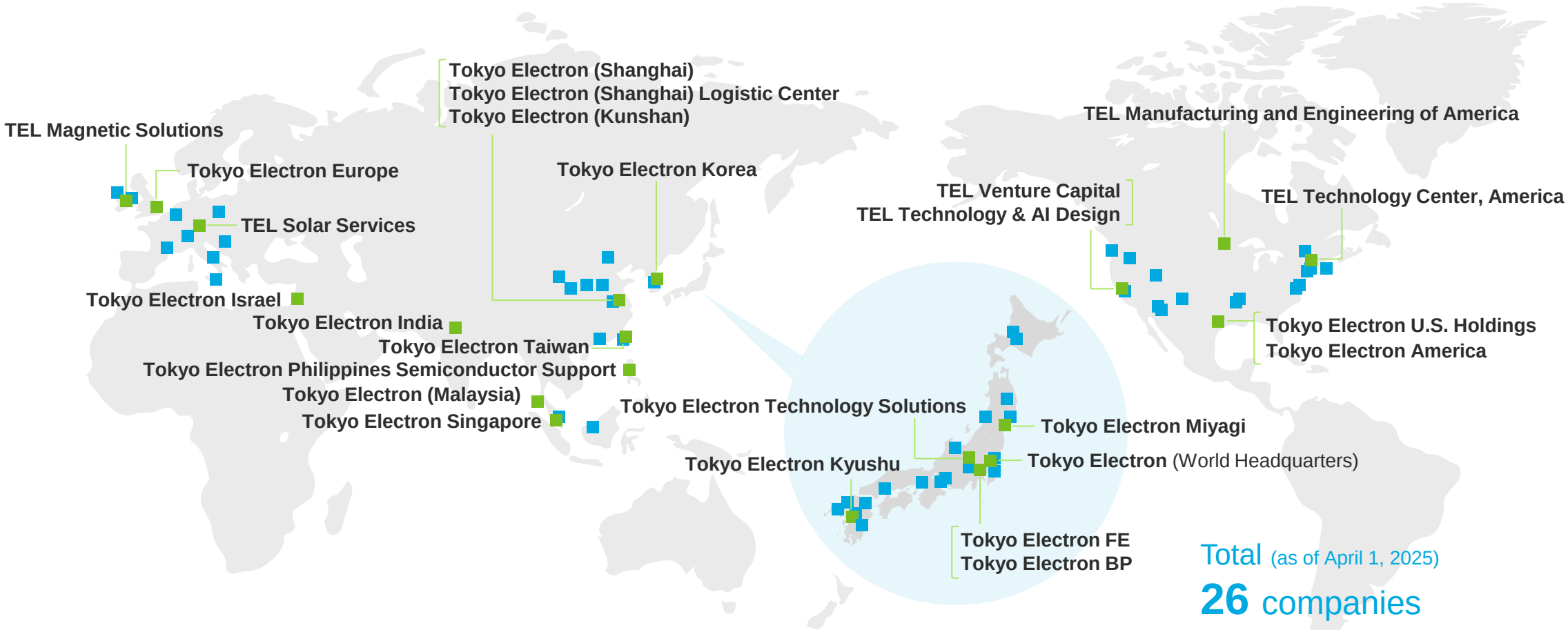
1. TEL Overview

Company Profile

Established	November 11, 1963
Major Products and Services	Semiconductor Production Equipment
Capital	54.9 Billion Yen
Sales/Profit	Net sales 2,431.5 Billion Yen / Operating income 697.3 Billion Yen / Operating margin 28.7% (Fiscal 2025)
Number of Employees	2,347 (non-consolidated) 20,273 (consolidated)
Global Network	Japan: 6 companies / 30 sites Overseas: 20 companies / 17 countries and regions / 65 sites Total: 26 companies / 18 countries and regions / 95 sites (consolidated) (as of April 1, 2025)

Worldwide Operations

(As of Apr. 1, 2025)



Head Office

Branch, Office (including Field Service), Sales Office

*Group companies in the process of being wound up are not shown on the map.

Total (as of April 1, 2025)

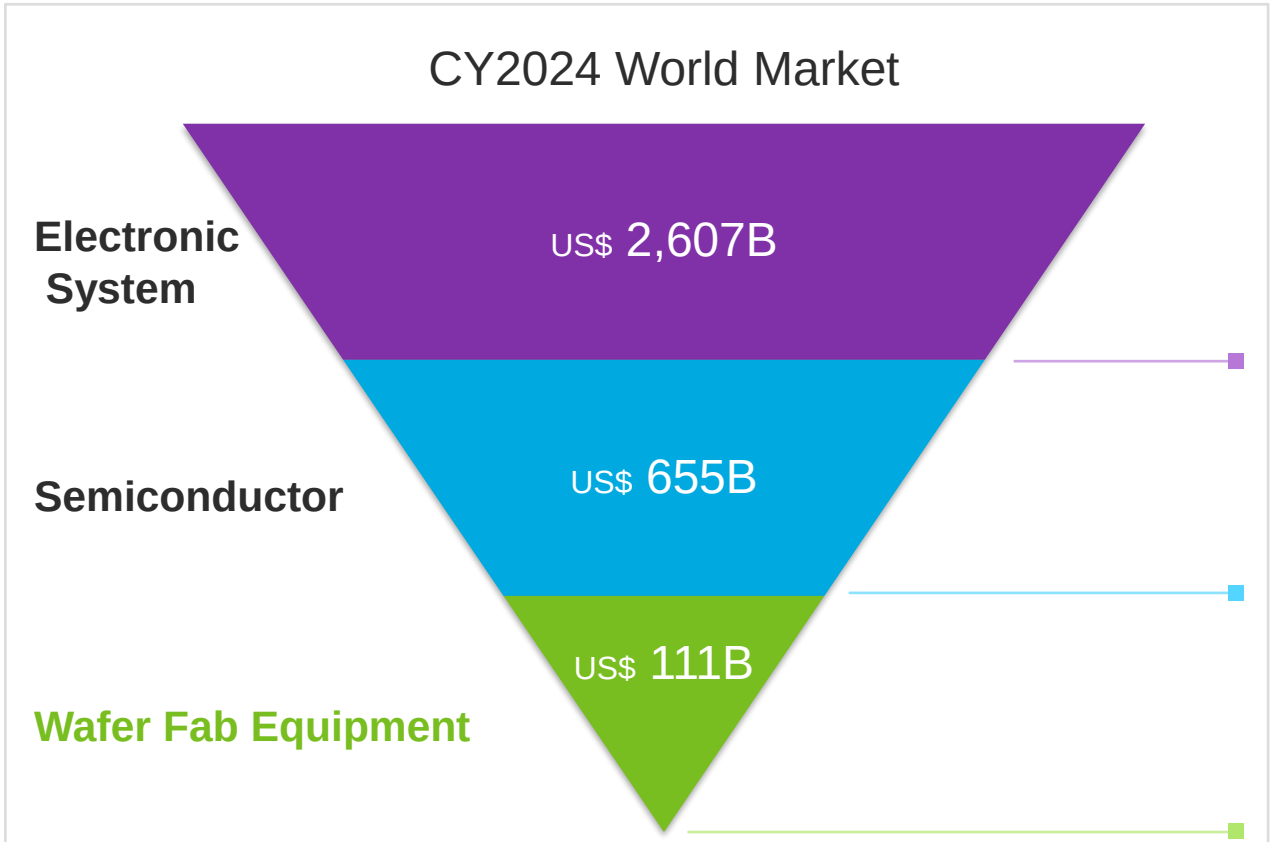
26 companies

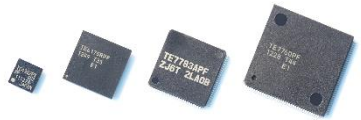
18 countries and regions

95 sites

The Market TEL Participates in

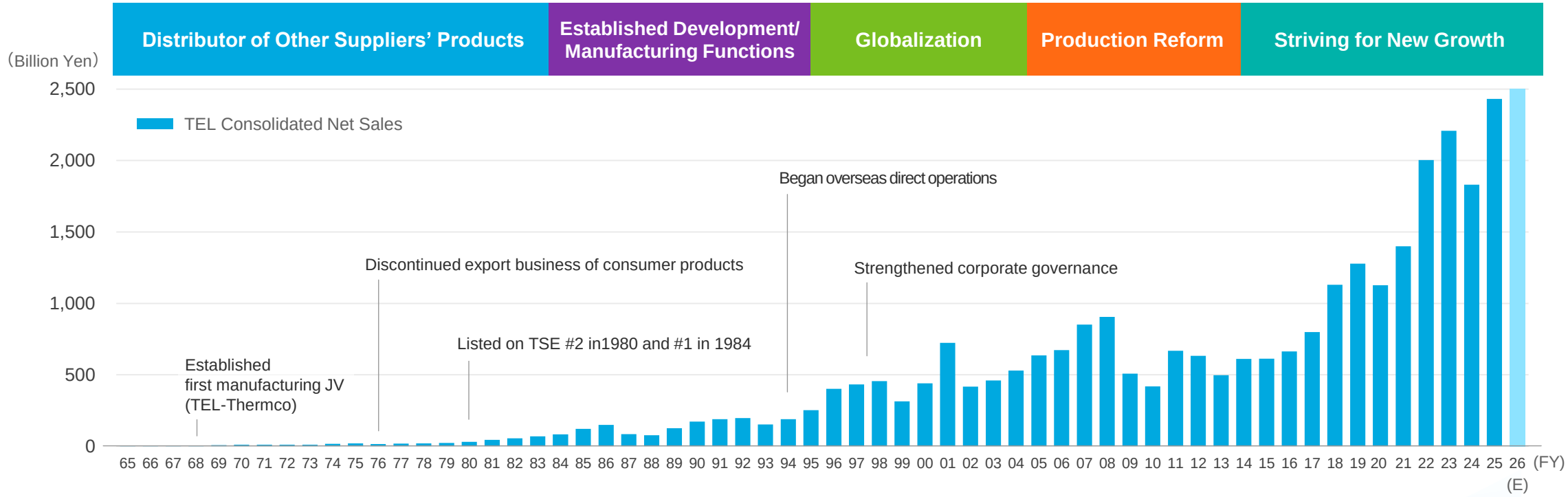
The market TEL participates in





Charts created by Tokyo Electron based on Gartner research.
Source: Gartner®, "Forecast: Semiconductor Capital Spending, Wafer Fab Equipment and Capacity, Worldwide, 1Q25 Update", Bob Johnson et al., 30 April 2025
Electronic System＝Electronic Equipment Production/Semiconductor＝Semiconductor Revenue /Wafer Fab Equipment ＝Total Wafer Fab Equipment Revenue Basis.

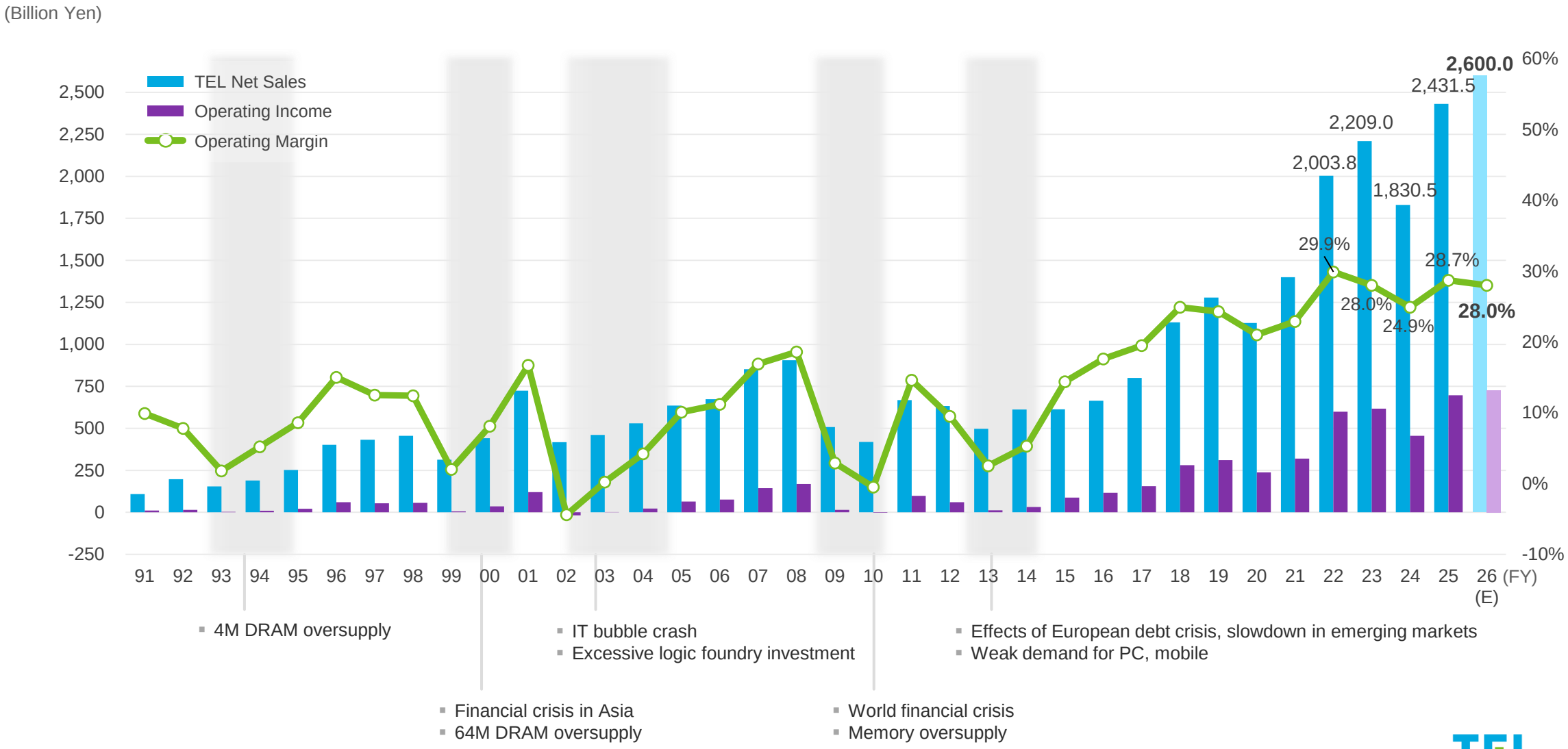
TEL's Growth



Expansion of Semiconductor Applications*

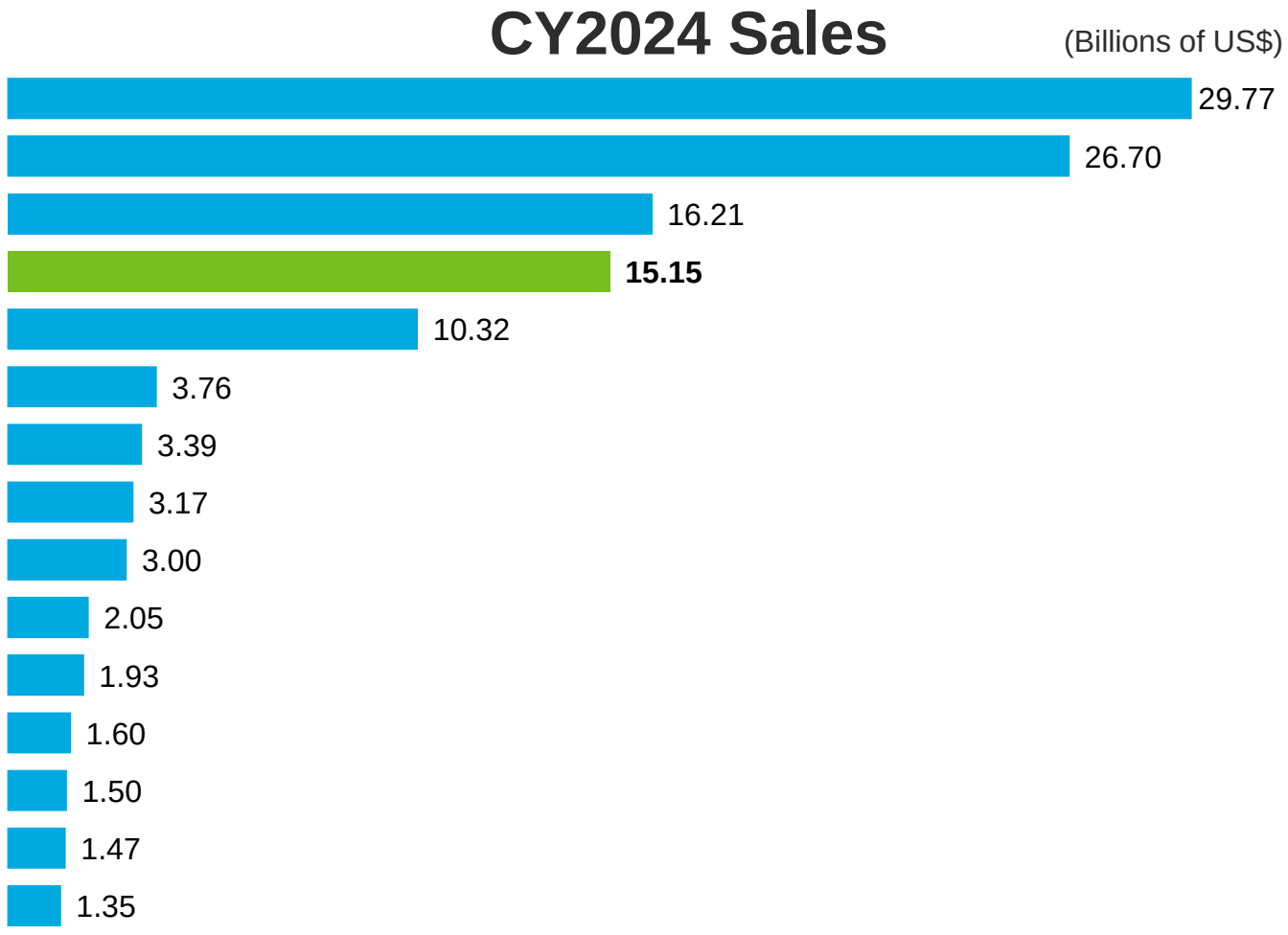
*The diagram is an image of the expanding use of semiconductors and does not indicate the actual number of semiconductors used.

Financial Performance: Sales and Operating Margin



CY2024 SPE Makers Top 15

1	ASML	29.77
2	Applied Materials	26.70
3	Lam Research	16.21
4	**Tokyo Electron**	**15.15**
5	KLA	10.32
6	Advantest	3.76
7	SCREEN	3.39
8	ASM International	3.17
9	NAURA	3.00
10	Teradyne	2.05
11	DISCO	1.93
12	SEMES	1.60
13	Hitachi High-Tech	1.50
14	KOKUSAI ELECTRIC	1.47
15	Lasertec	1.35



Source：TechInsights Inc., May 2025

Semiconductor Manufacturing Process

TELCC-SMP-003

Wafer Process (Front-end)
Assembly and Test process (Back-end)

Deposition

TELINDY PLUS™ NT333™ Episode™1

Lithography
(Photoresist coating, Development)

CLEAN TRACK™ LITHIUS Pro™ Z

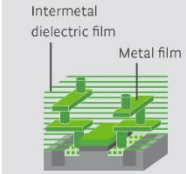
Etching

Tactras™ Episode™ UL Certas LEAGA™

Cleaning

CELLESTA™-i

Film deposition | Photoresist coating | Exposure | Development | Etching | Ashing / Cleaning



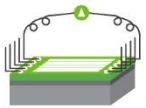
Completed Transistor and Wiring

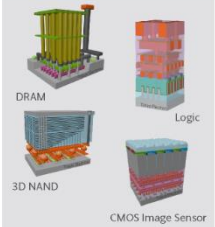
Bonding

Synapse™ Si Ulucus™ L / Ulucus™ LX

Wafer Probe Testing

Prexa™ Cellcia™





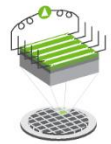
Completed Integrated Circuit

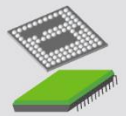
Wafer Bonding / Debonding

Synapse™ V / Synapse™ Z Plus

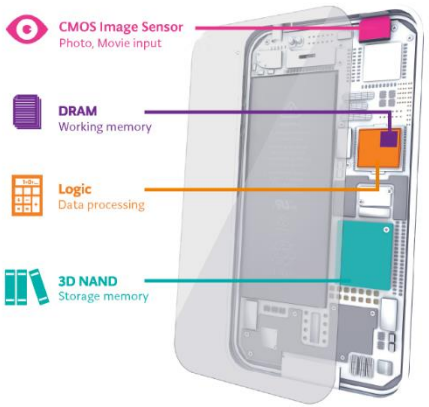
Inspection

WDF™ 12DP+

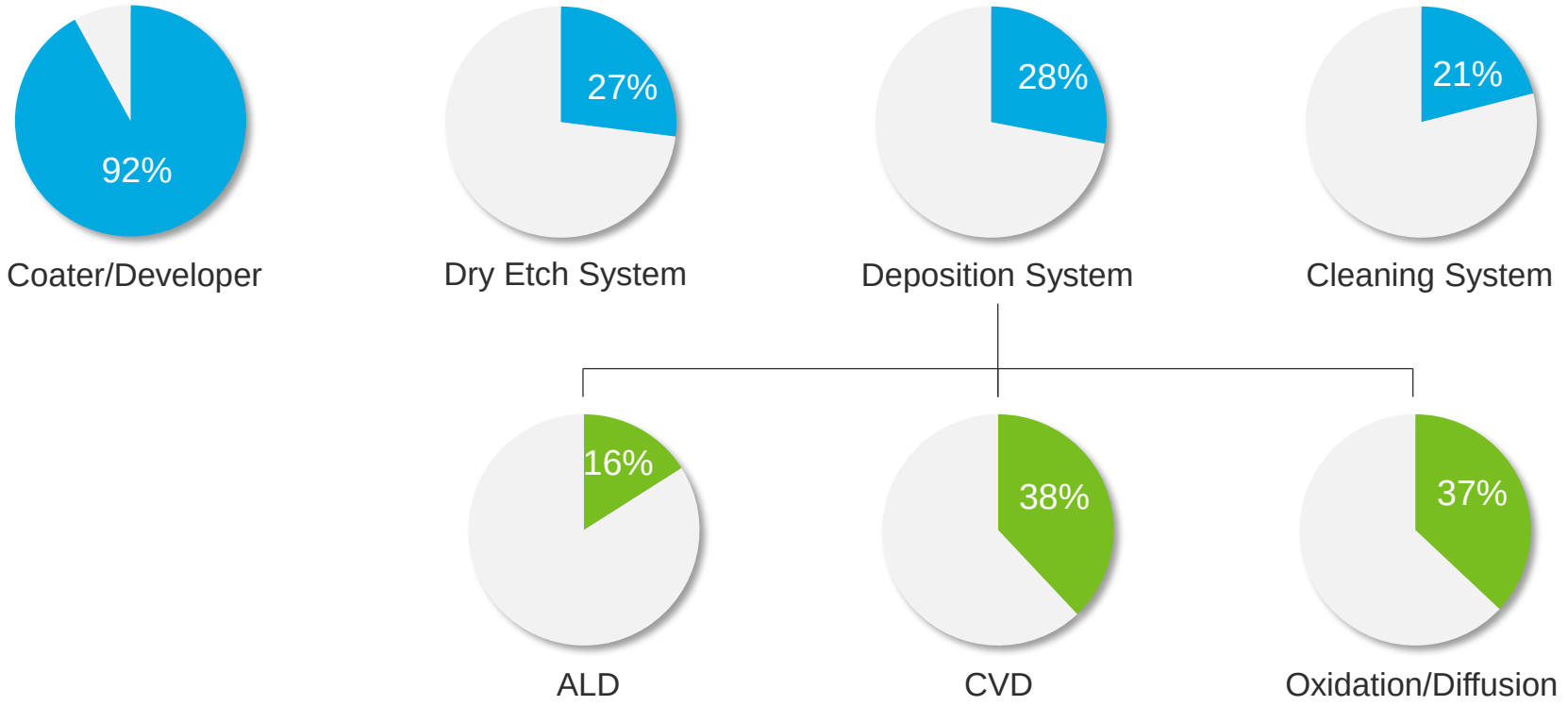


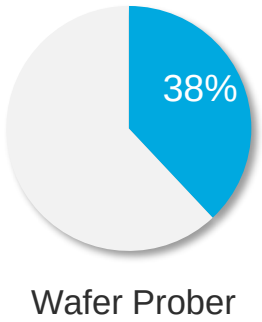


Completed Semiconductor Packaging



World Market Share of Major Products（CY2024）





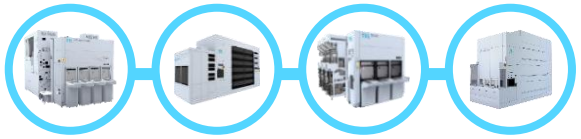
Source
SPE (excluding Wafer Prober) : Gartner®, Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2024, Bob Johnson and Menglin Cao, 21 April 2025, Revenue from Shipments basis. Chart created by TEL based on Gartner research. Gartner research. Calculations performed by TEL.
Coater/Developer: Photoresist Processing (Track), Dry Etch System: Dry Etch, Deposition System: Tube CVD + Atomic Layer Deposition Tools + Oxidation/Diffusion Furnaces + Nontube LPCVD, ALD: Atomic Layer Deposition Tools, CVD: Tube CVD + Nontube LPCVD, Oxidation/Diffusion: Oxidation/diffusion Furnaces, Cleaning System: Single Wafer Processors + Wet Stations + Batch Spray Processors + Scrubbers + Other Clean Equipment, Wafer Bonder: Wafer Bonder.

Source
SPE (Wafer Prober) : Auto Probers, TechInsights Inc., April 2025
Charts/graphics created by Tokyo Electron based on : TechInsights Inc.

TEL's Strengths

Only One

Have products in 4 sequential processes



Deposition | Coater/ Developer | Etch | Cleaning

No.1/No.2

Products with the world's No. 1 or No.2 market share

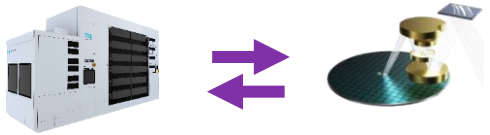
Major Products & Market Position*

#1	#2	#2	#1	#1	#1	#2	#1	#2
Coater/ Developer	Cleaning	Plasma Etch	Gas Chemical Etch	Diffusion Furnace	Batch Deposition	Metal Deposition	Prober	Bonding

*TEL estimate

100%

Market share of coater/developer for EUVL



Coater/ Developer | EUV Lithography

No.1

Worldwide installed base

Annual increase by about 4,000～6,000 units*1

Industry's largest installed base 96,000 units*2

*1 As of March 2024
*2 As of December 2024

R&D Map

(As of May 10, 2024)

TEL Magnetic Solutions (Ireland)

imec (Belgium)

CEA-Leti (France)

TEL Technology Center Korea (Korea)

TEL Technology Center, Taiwan (Taiwan)

IME (Singapore)

TEL Digital Design Square
Tokyo Electron Technology Solutions
Tokyo Electron Miyagi
Tokyo Electron Kyushu
(Japan)

National Institute of Advanced Industrial Science and Technology
(Japan)

TEL Manufacturing and Engineering of America (U.S.)

TEL Technology Center, America (U.S.)

SUNY Poly/NY CREATES (U.S.)

BRIDG (U.S.)

Tokyo Electron America (U.S.)

TEL R&D base

Consortium

Strengthen R&D Capabilities

Yamanashi R&D building

Deposition system, gas chemical etch system, corporate R&D

(Established in July 2023)

Miyagi R&D building

Etch system

(Completion scheduled for spring 2025)

Kumamoto R&D building

Coater/Developers, surface preparation system, Bonder

(Completion scheduled for autumn 2025)

Miyagi Technology Innovation Center

Etch system

(Established in September 2021)

TEL Digital Design Square

DX, Software

(Began operation in Novenmber 2020)

Continually Pursuing the Best Products and Best Service

Front-loading

Advanced field solutions

- Share roadmap for next several generations with customers
- Promote early engagement
- Realize maximum yield of customer devices and equipment availability from early stage of customers' mass production and reduce burden on the environment
- Further increase investment in human resources/R&D by raising operational efficiency and driving higher per-employee productivity

- Business development leveraging industry's largest installed base of 96,000 units*
- TELeMetrics™ remote maintenance
- Predictive maintenance with machine learning

* As December 2024

Maximize Utilization of TEL's Comprehensive Strengths

Sales

Customer trust

Broad product coverage

Market-ing

Advanced data collection and analysis abilities

FS

- **Largest installed base in industry: over 96,000 units***
- **Advanced FS**

* As of December 2024

R&D

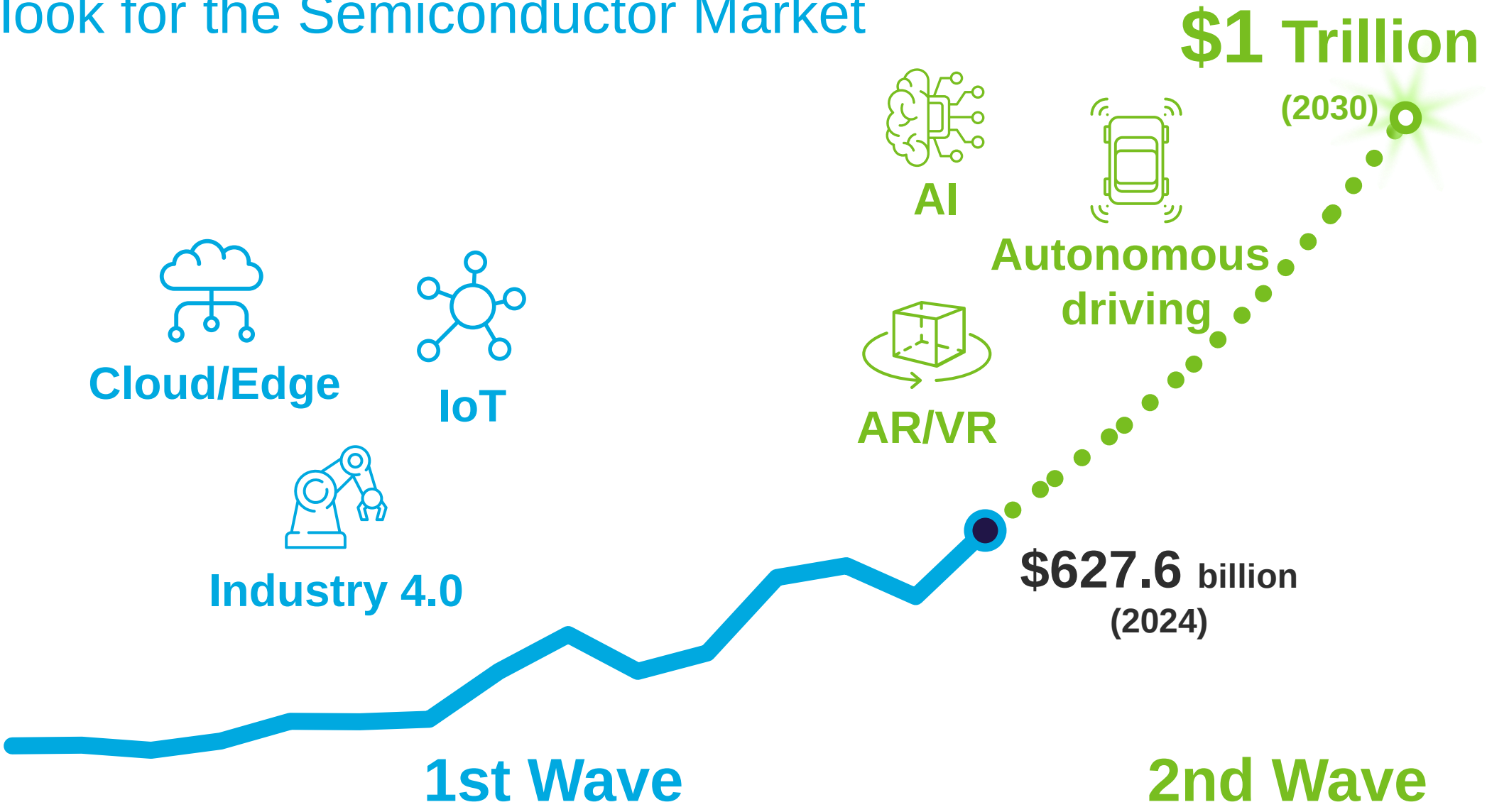
- **Strong next generation product development**
- **Process integration**

Manu-facturing

- **High quality**
- **Robust supply chain**

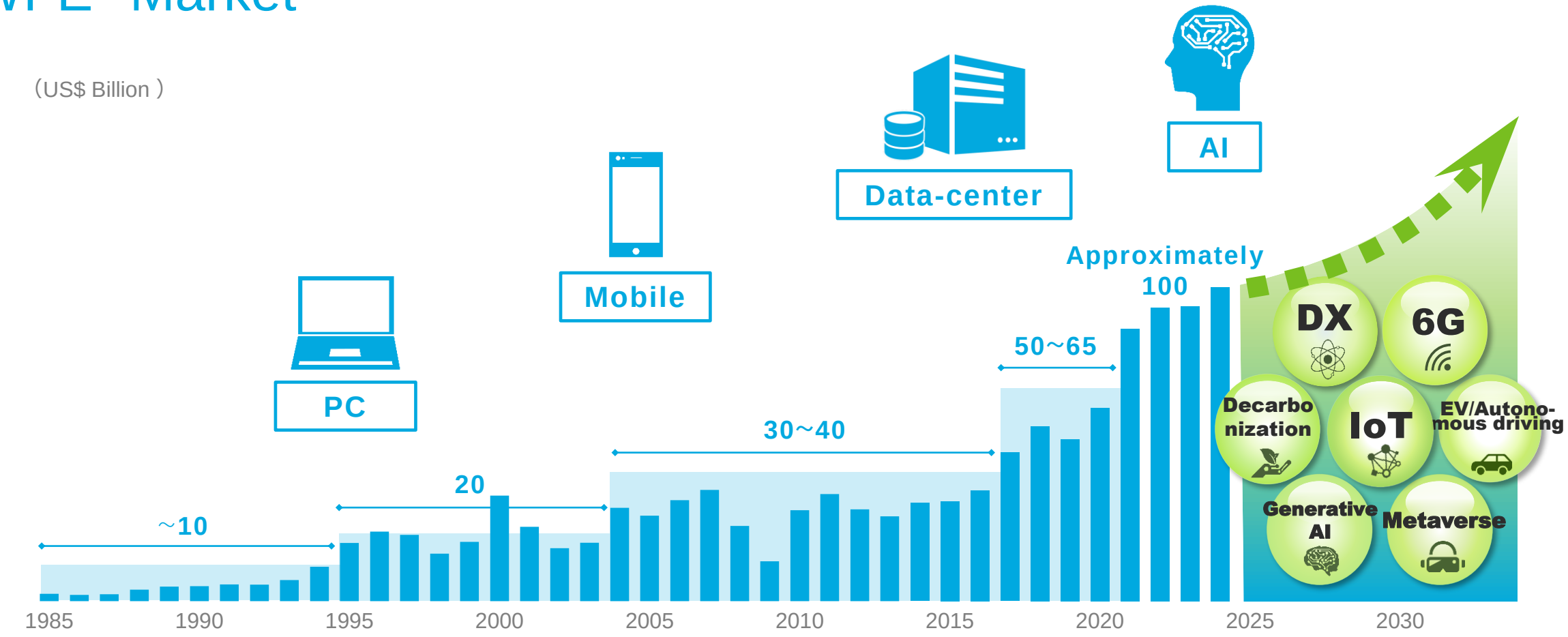
2. Semiconductor and SPE Market Outlook

Outlook for the Semiconductor Market



Source:1990-2024 (WSTS)／2025-2030 (IBS, January 2025)

WFE* Market

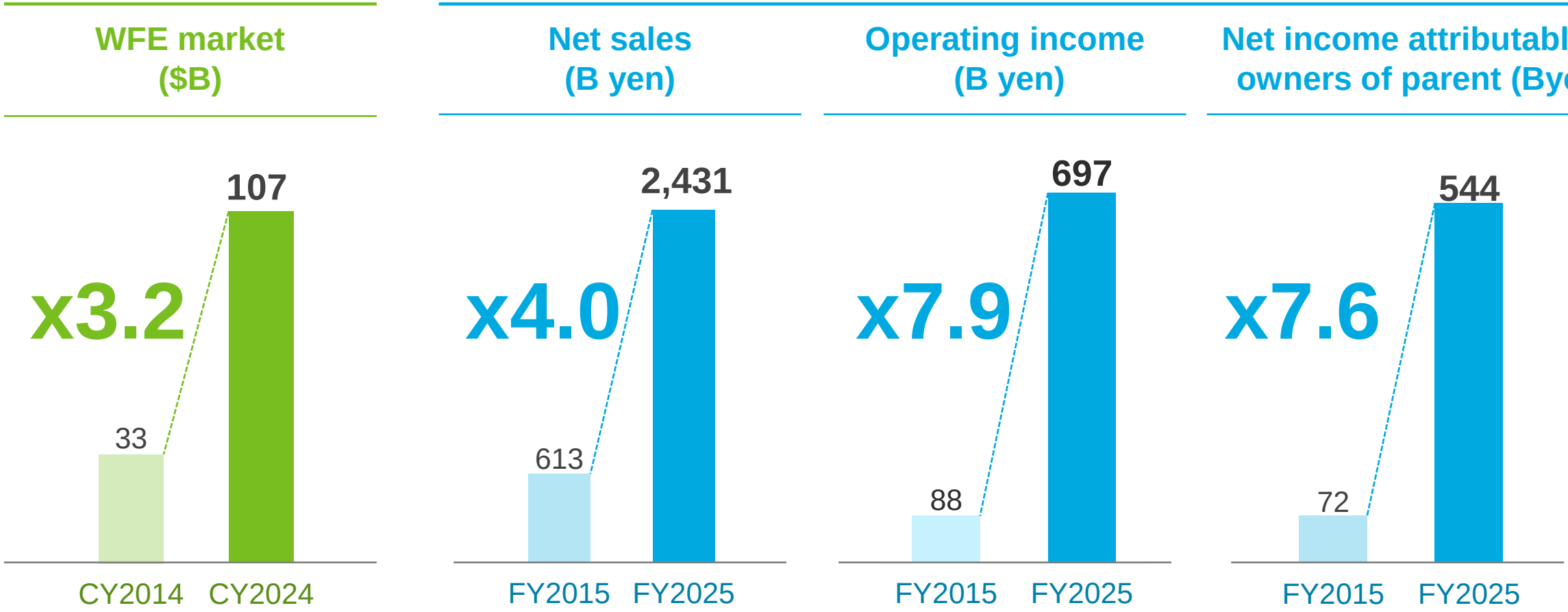


* WFE (Wafer Fab Equipment): The semiconductor production process is divided into front-end production, in which circuits are formed on wafers and inspected, and back-end production, in which wafers are cut into chips, assembled and inspected again. WFE refers to the production equipment used in front-end production and in wafer-level packaging production.

Source : TechInsights Inc. (1985~2024)

WFE Market will grow further with progress of digitalization and evolution of semiconductors

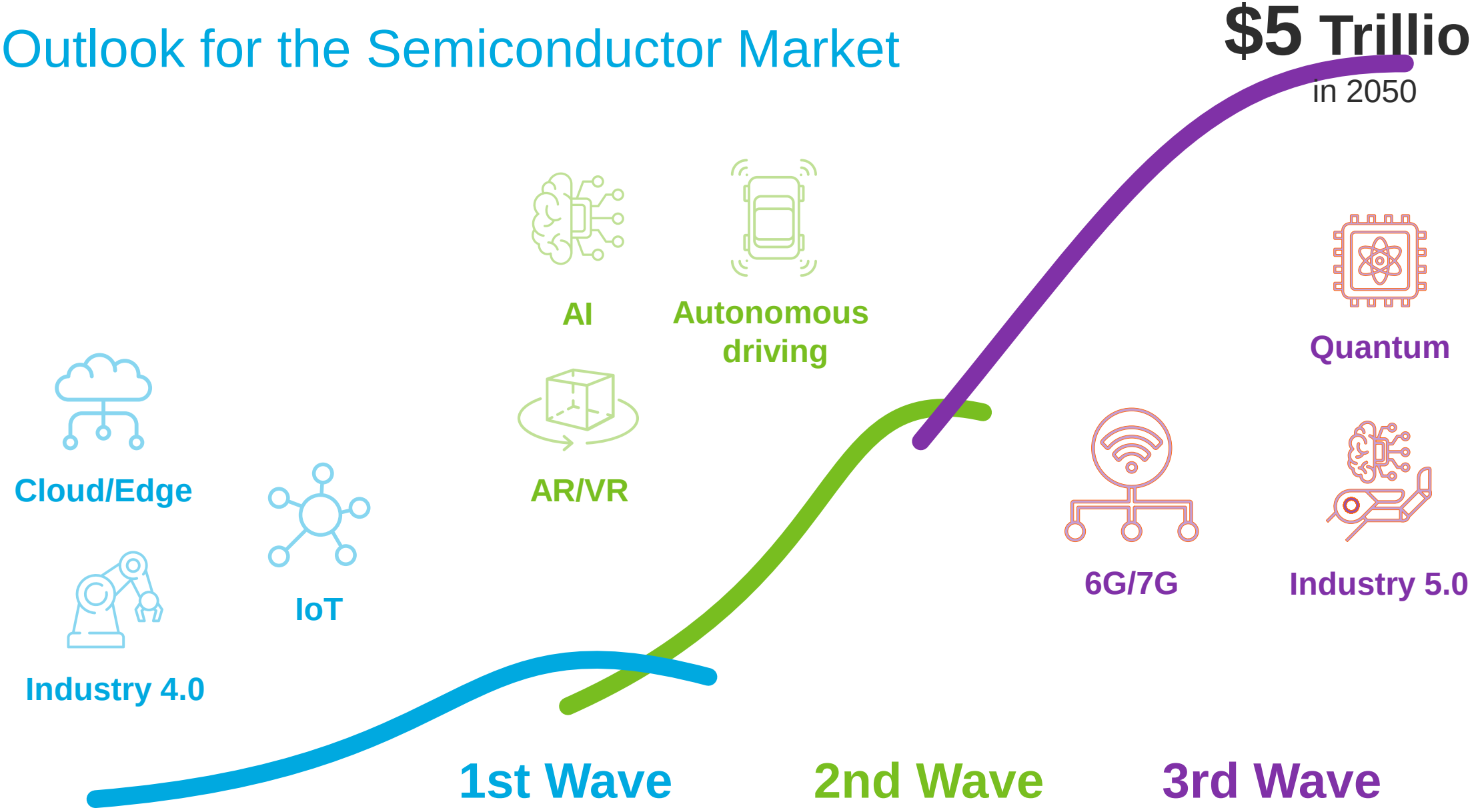
Market and Performance Growth (FY2015 to FY2025)



Significantly outperformed market growth

Source : TechInsights Inc.

Outlook for the Semiconductor Market



Source: SEMI 2024

Green Future Through Semiconductor Evolution

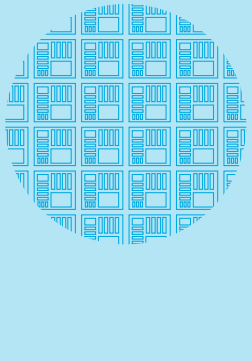
Digital & Green

Higher Speed

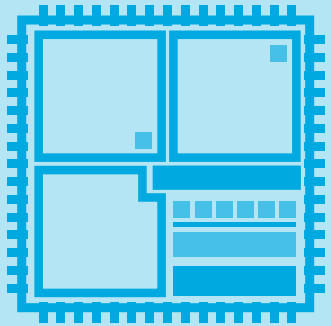
Larger Capacity

Superior Reliability

Lower Power Consumption



Physical Scaling



Heterogeneous Integration

Physical Scaling x Heterogeneous Integration

Frontend

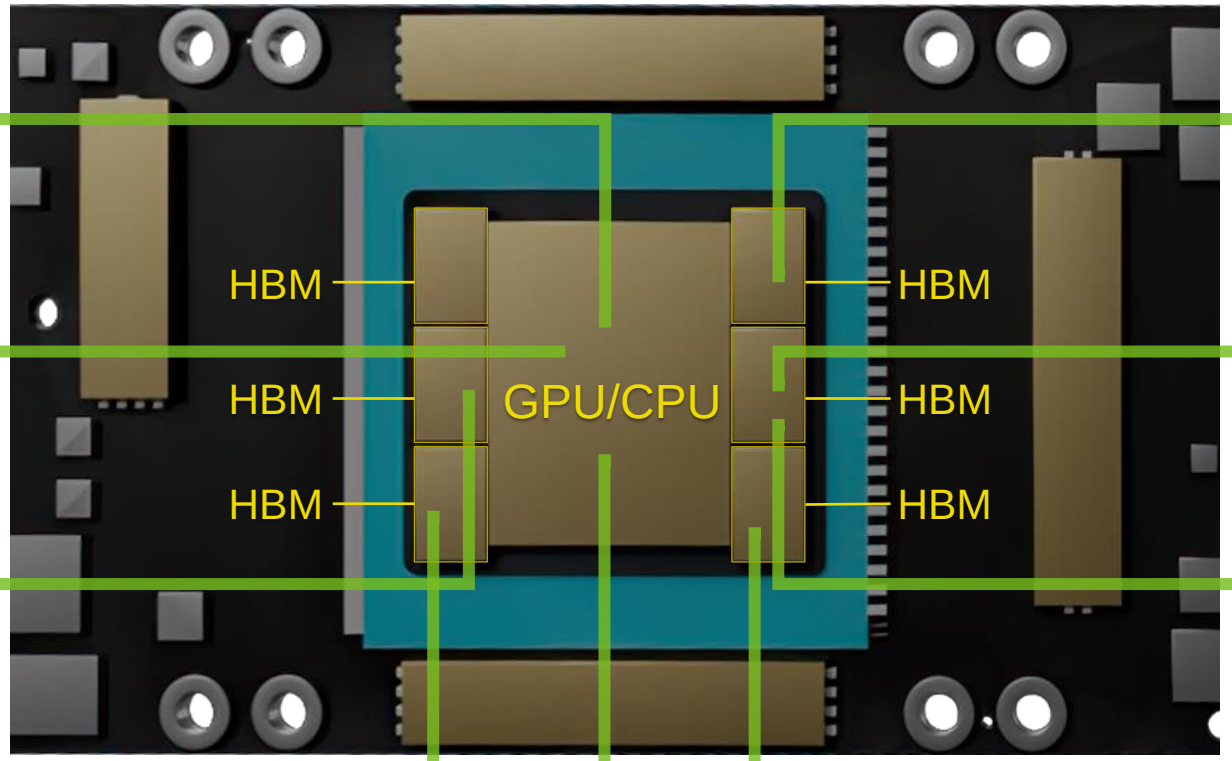
Logic
GAA * / CFET

Logic
Backside PDN *

DRAM
VCT * $4F^2$ / 3D DRAM

Super Flat Wafer

AI Semiconductor



Advanced Packaging

Heat Spreader

3DIC
Chiplet Integration

Stack Memory
HBM, etc.

Known Good Die

* GAA : Gate All Around
* Backside PDN : Backside Power Delivery Network
* VCT : Vertical Channel Transistor

Expanding Opportunities: Wide Product Portfolio

Frontend

Advanced Packaging

Deposition

Lithography

Etch

Cleaning

Testing

Bonding / Debonding

Batch Deposition

Semi-batch Deposition

Single Deposition

Coater/ Developer

Plasma Etch

Gas Chemical Etch

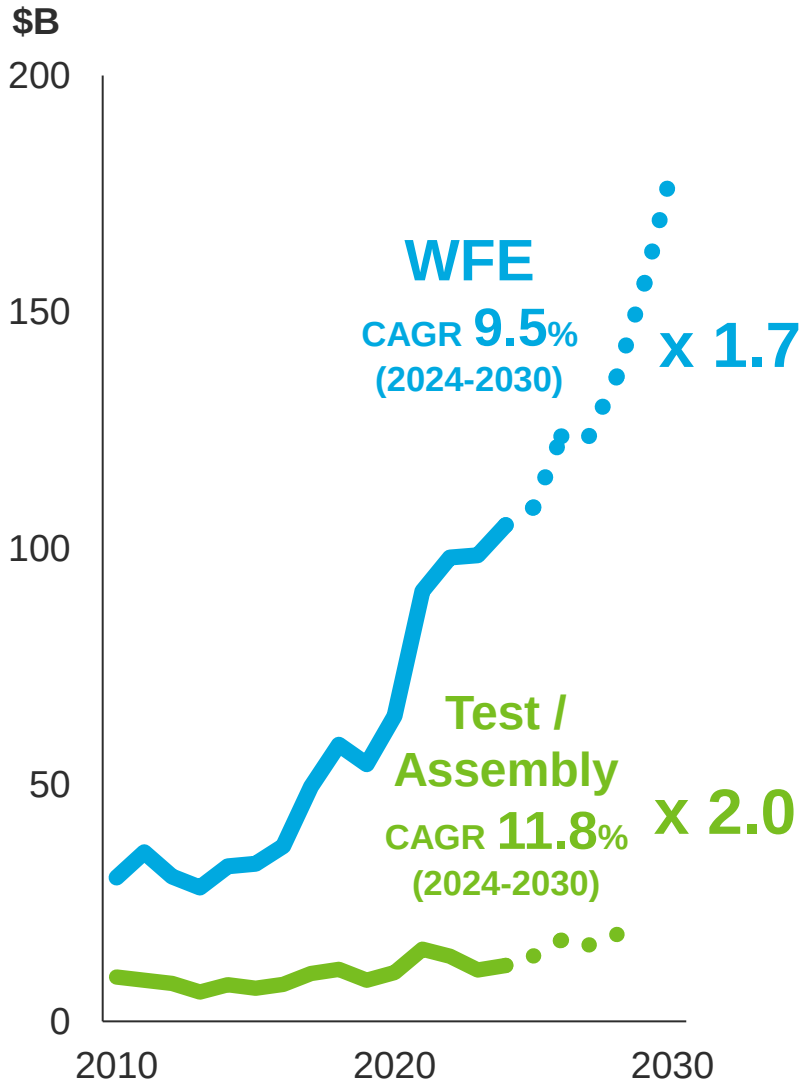
Cleaning

Prober

Wafer Bonder/ Debonder

Wafer Edge Trimming

Strategic Technologies for Future Growth



Source : TechInsights (April 2025)

Frontend

Logic : GAA, BSPDN

- EUV Coater/Developer
- Gas Chemical Etch
- Conductor Etch
- PVD Metal Overburden
- CFET/Inner Spacer Plasma CVD for filling film
- Double-sided scrubber
- Backside/bevel cleaning
- Pattern Shaping
- Wafer Bonder
- Laser Tool

DRAM: 2D & 3D DRAM

- EUV Coater/Developer
- Capacitor Mold Etch
- Batch High-k Capacitor deposition
- PVD Metal Hardmask
- Supercritical Cleaning
- Backside/bevel Cleaning
- Wafer Bonder
- Laser Tool

NAND: Beyond 4xx

- Slit Etch
- Channel Hole Etch (Plug)
- Batch Mo deposition
- Batch Cleaning WL Separation
- Wafer Bonder
- Laser Tool

Advanced Packaging

Logic Packaging

- Interposer, Polyimide & PR Coater/Developer
- TDV Etch
- Batch High-k Capacitor depo
- Wafer Bonder
- Laser Tool

HBM Packaging

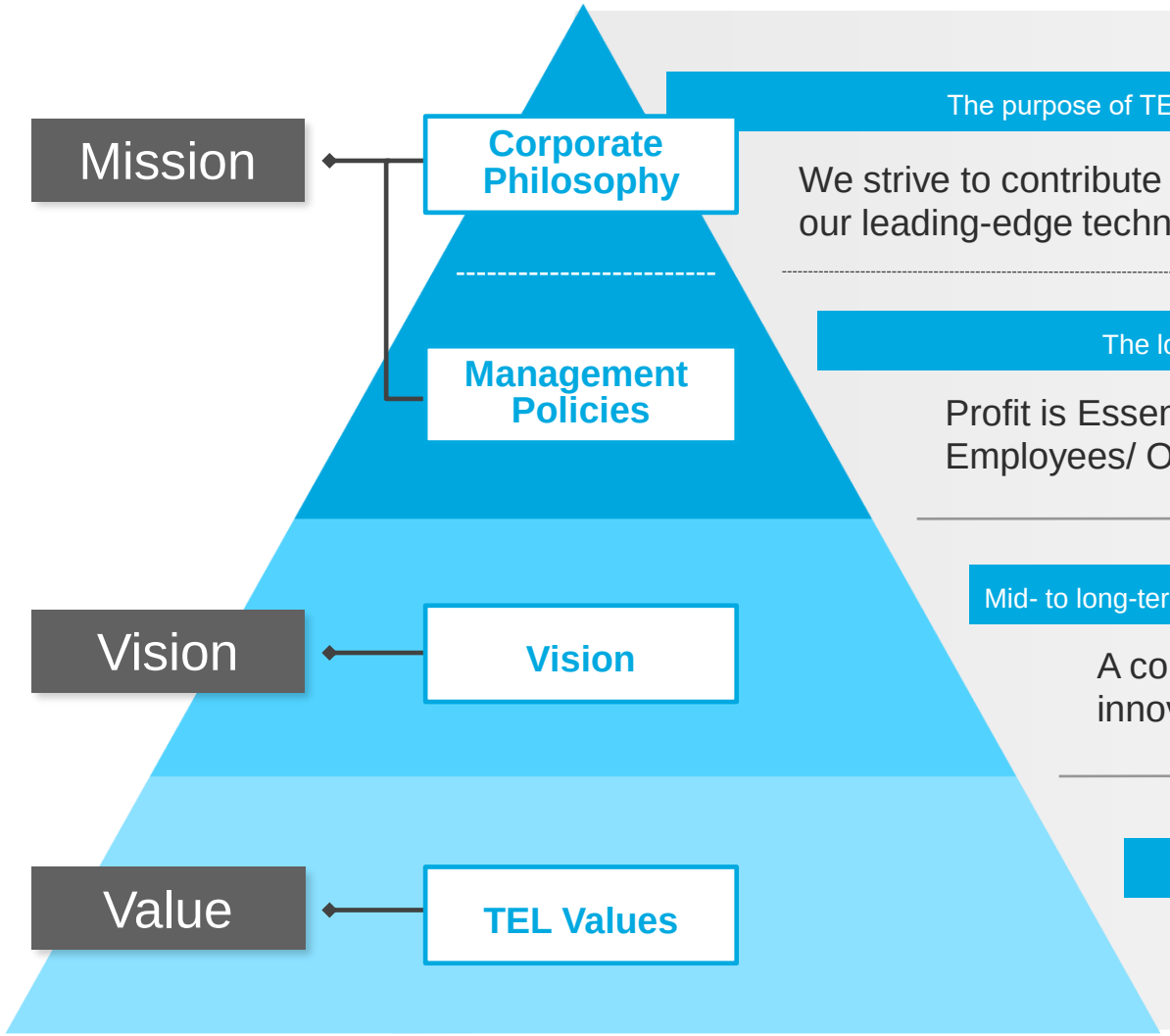
- Polyimide & PR Coater/Developer
- Metal Etch for HBM
- Aerosol Cleaning
- Temporary Bonder/Debonder

Advanced Logic / Memory Test

- Prober

3. Corporate Principles and New Medium-term Management Plan

Corporate Principles System



Corporate Philosophy

The purpose of TEL's existence and its mission in society

We strive to contribute to the development of a dream-inspiring society through our leading-edge technologies and reliable service and support

Management Policies

The logic that underscores general rules of management

Profit is Essential/Scope of Business/Growth Philosophy/Quality and Service/ Employees/ Organizations/Safety, Health, and the Environment/Social Responsibility

Vision

Mid- to long-term business aspirations based on our Corporate Philosophy and Management Policies

A company filled with dreams and vitality that contributes to technological innovation in semiconductors

TEL Values

Attitudes, codes of conduct, and values to be observed by each employee

Pride/Challenge/Ownership/Teamwork/Awareness

Vision

A company filled with dreams and vitality that contributes to technological innovation in semiconductors

Tokyo Electron pursues technological innovation in semiconductors that supports the sustainable development of the world.

We aim for medium- to long-term profit expansion and continuous corporate value enhancement by utilizing our expertise to continuously create high value-added leading-edge equipment and technical services.

Our corporate growth is enabled by people, and our employees both create and fulfill company values. We work to realize this vision through engagement with our stakeholders.

Technology Enabling Life

"Technology Enabling Life" is our corporate message that expresses the Corporate Principles which consist of our Corporate Philosophy, Management Policies, Vision and TEL Values.

CSV
(Creating Shared Value)

The concept is to create social and economic value by leveraging corporate expertise to solve social issues, hereby enhancing corporate value and achieving sustainable growth.

TSV
TEL's Shared Value

=

- Pursue technological innovation in semiconductors that supports the sustainable development of the world
- Continuously create high value-added leading-edge equipment and technical services
- Medium- to long-term profit expansion and continuous corporate value enhancement
- Engagement with our stakeholders

Realization of Vision = Creating Shared Value in TEL

Our Approaches to Social Issues

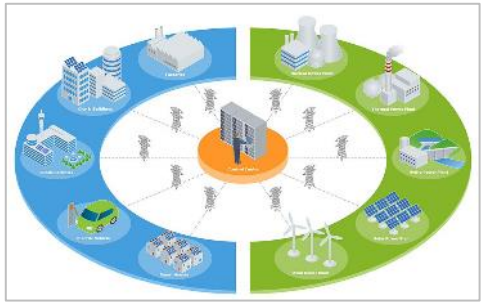
Sustainable development of the world / Diversification of values and happiness

Solutions

Online/Metaverse

AI diagnosis/Prevention/Robots

Smartification



EV/Autonomous driving/MaaS

Technologies

- Higher speed communication (5G/6G)
- Cloud/Edge Computing
- AI
- IoT
- AR/VR/MR

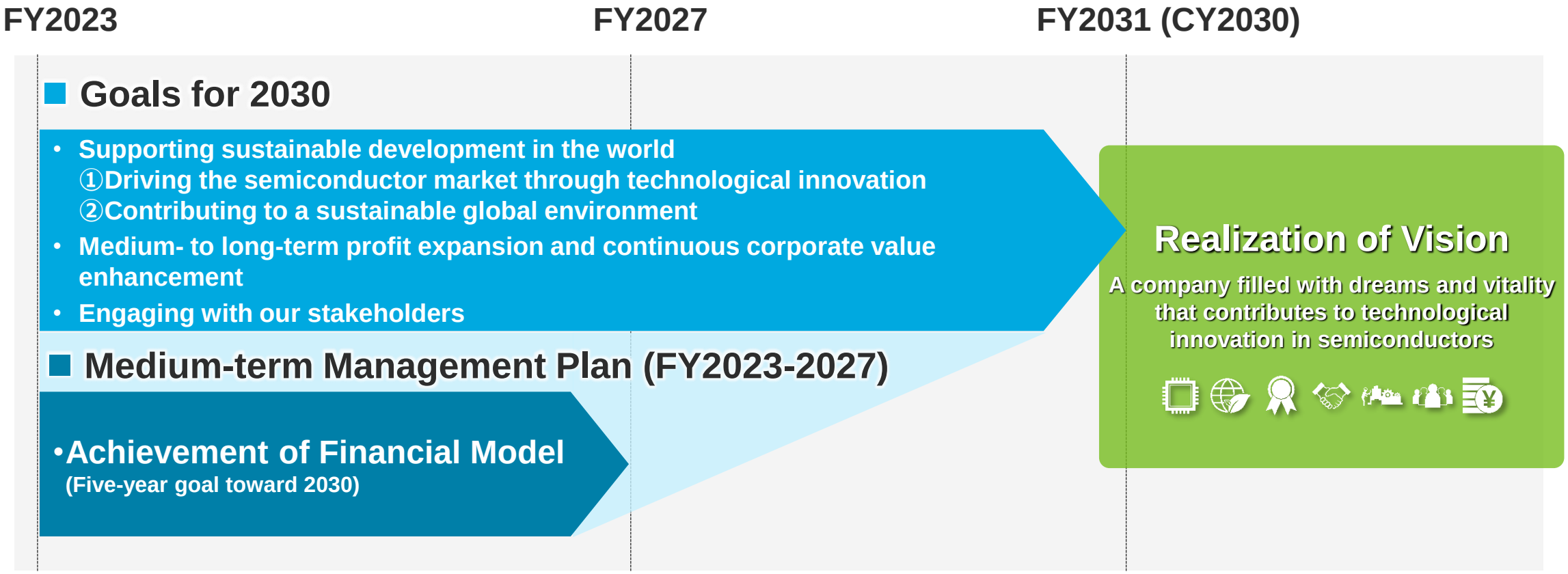
Semiconductors

- Logic
- Memory
- Power
- Analog
- Sensor
- Display

Pursue technological innovation in semiconductors：
Larger capacity/Higher speed/Higher reliability/Lower power consumption

Higher definition/Flexible /Lower power consumption

Vision & Medium-term Management Plan

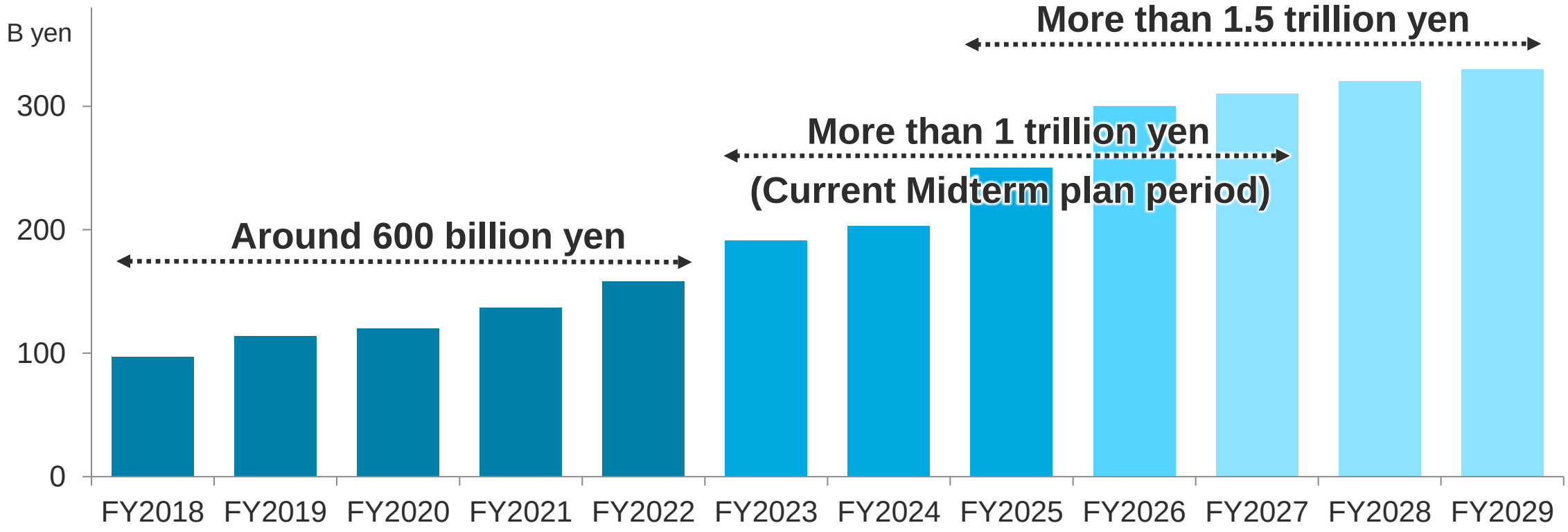


Aiming to achieve the Medium-term Management Plan
by FY2027 with a view to realizing Vision in 2030

The New Medium-term Management Plan : Financial Targets

Financial Targets (FY2023 - FY2027)	
Net sales	≥ 3 trillion yen
OP margin	≥ 35%
ROE	≥ 30%

Aggressive Investment in R&D

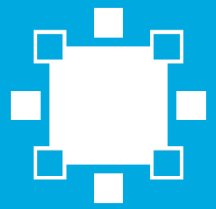


Driving the creation of high-value next-generation products through further growth investments

Investment for Growth Visioning beyond the Midterm Plan (FY2025 to FY2029)

R&D Investment

1.5
trillion yen



Capex

700
billion yen

Recruitment

10,000
people
2,000 people/year

4. Business Environment and Financial Estimates

FY2025 Business Highlights

- Achieved record highs for both net sales and profit.
  Gross profit exceeded 1 trillion yen for the first time
  - Net sales grew +33%. Sales for DRAM grew significantly by +59% with the adoption of a wide range of equipment for HBM*1
- Market share expanded by winning PORs*2 with strategic products
  - **Etch**: DRAM - major monopoly in capacitor etch; NAND - new POR in channel hole etch (cryogenic etch), expansion in slit etch; logic/HBM - adoption in advanced packaging interconnect processes
  - **Wafer bonders**: Significant increase in demand for temporary bonders/debonders for HBM
  - **Probers**: sales rose by leveraging the trend of expanding investments in advanced logic
- Released new products on the expectation that they will support entry into new areas
  - Episode™ 1 single-wafer plasma CVD system; LEXIA™-EX sputtering system; Acrevia™ Gas Cluster Beam system; Ulucus™ LX extreme laser lift off system
- Completed share repurchase of approx. 150 billion yen

*1 HBM: High Bandwidth Memory
*2 POR: Process of Record

Business Environment (WFE Market Outlook as of April 2025)

- **CY2025: Forecasting around $110B, flat YoY**
  - Lull in both automotive and power semiconductor investment, and investment by emerging Chinese manufacturers
  - Demand for AI servers is driving investment in leading-edge logic and HBM
- **CY2026: Double-digit growth is expected**
  - Expect continued and significant demand for AI servers, as well as an acceleration in investment in 2nm mass production
  - Also expect higher semiconductor demand accompanying the increase in on-device AI for PCs and smartphones

Expanding business opportunities for TEL amid progress in technological innovations of both scaling and heterogeneous integration (GAA*1, BSPDN*2, HBM, testing) in order to achieve even higher speed, higher capacity, higher reliability and lower power consumption

*1 GAA (Gate All Around) : A transistor structure where the channel is surrounded by the gate
*2 BSPDN (Backside Power Delivery Network) : Structures that arrange power delivery networks on the backside of wafer

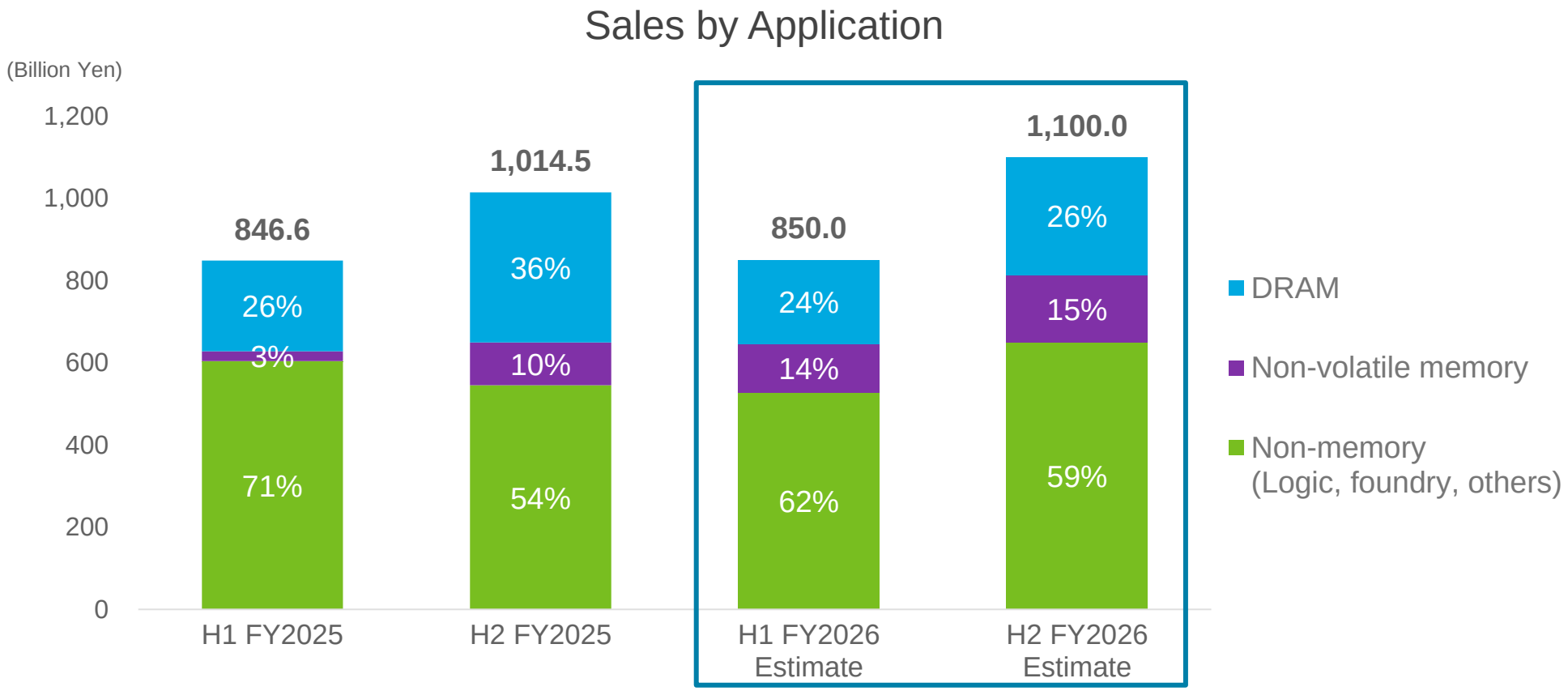
FY2026 Financial Estimates

(Billion Yen)

	FY2025 (Actual)	FY2026 (Estimates)			
		H1	H2	Full Year	Full Year YoY
Net sales	2,431.5	1,150.0	1,450.0	2,600.0	+6.9%
Gross profit Gross profit margin	1,146.2 47.1%	527.0 45.8%	701.0 48.3%	1,228.0 47.2%	+7.1% +0.1pts
SG&A expenses R&D Other than R&D	448.9 250.0 198.9	239.0 140.0 99.0	262.0 160.0 102.0	501.0 300.0 201.0	+11.6% +20.0% +1.1%
Operating income Operating margin	697.3 28.7%	288.0 25.0%	439.0 30.3%	727.0 28.0%	+4.3% -0.7pts
Income before income taxes	706.1	293.0	443.0	736.0	+4.2%
Net income attributable to owners of parent	544.1	224.0	342.0	566.0	+4.0%
Net income per share (Yen)	1,182.40	488.97	-	1,235.51	+53.11

Expect record high revenue and OP again in FY2026
Plan 300B yen R&D investment to maximize future growth opportunities

FY2026 SPE New Equipment Sales Forecast



Percentages on the graph show the composition ratio of new equipment sales. Field solutions sales are not included.

Expect customers to begin preparations in H2 FY2026 in anticipation for market growth in CY2026.
Expect record-high half-year sales in H2 FY2026

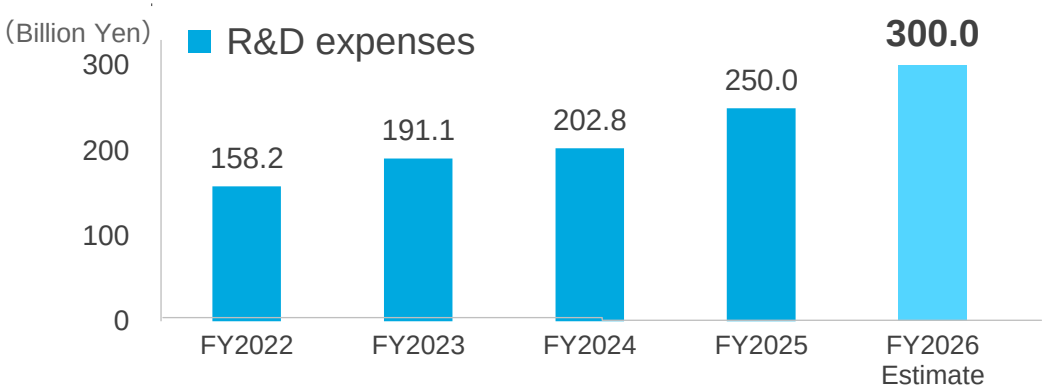
FY2026 R&D Expenses and Capex Plan

New Development Building
Etch system

Kurokawa-gun, Miyagi Prefecture
Established in April 2025

New Development Building
Coater/developer, cleaning system, bonder

Koshi-city, Kumamoto Prefecture
Completion scheduled for autumn 2025

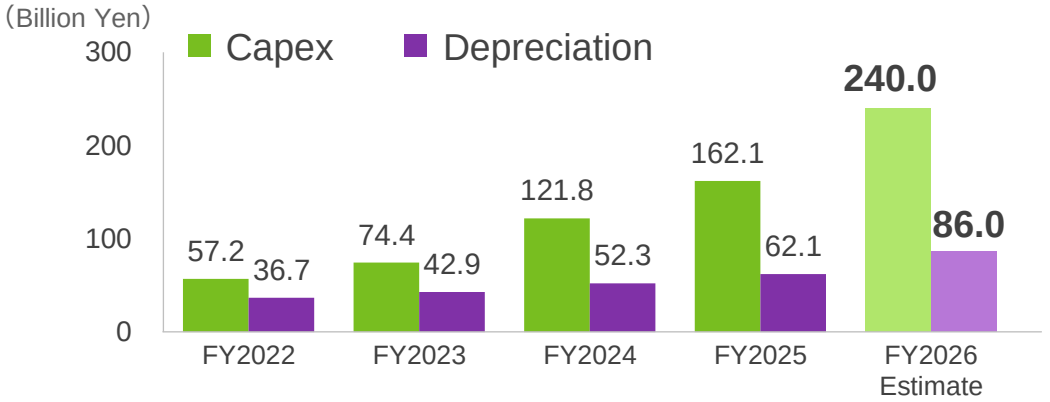


Tohoku Production and Logistics Center
Deposition system

Oshu-city, Iwate Prefecture
Completion scheduled for autumn 2025

New Production Building
Etch system

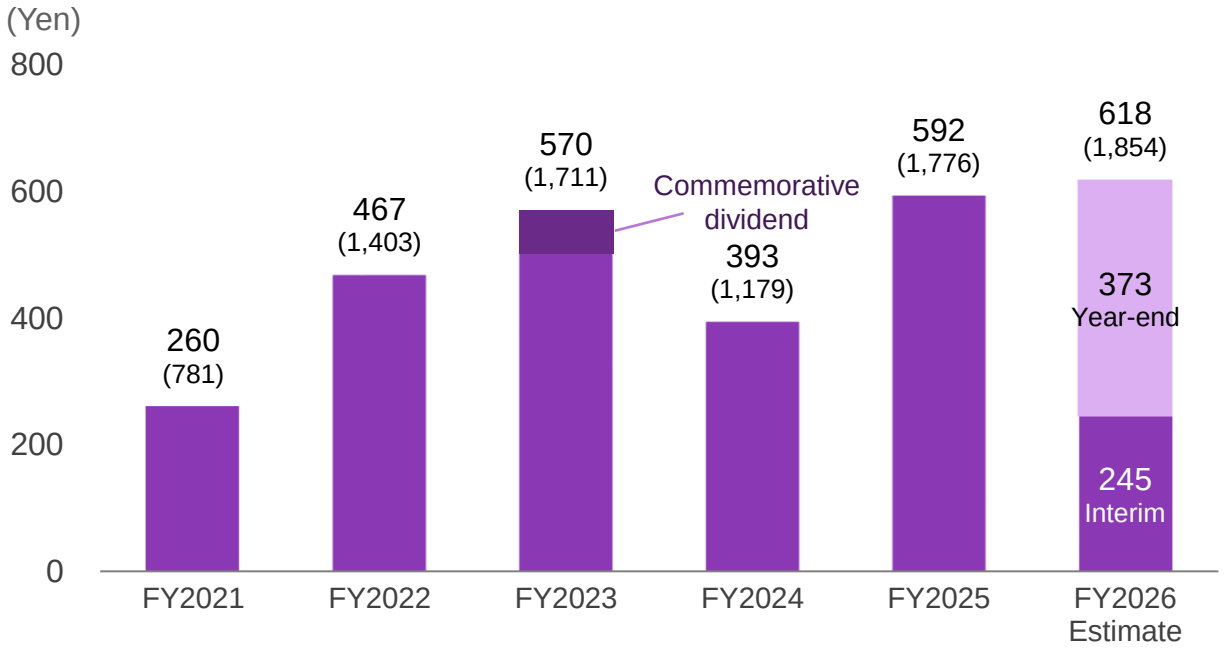
Kurokawa-gun, Miyagi Prefecture
Completion scheduled for summer 2027



Continue aggressive R&D and capital investments for future growth

FY2026 Dividend Forecast

Dividend per Share



TEL shareholder return policy

Dividend payout ratio: 50%

Annual DPS of not less than 50 yen*

We will review our dividend policy if the company does not generate net income for two consecutive fiscal years

We will flexibly consider share buybacks

*Due to the stock split on April 1, 2023, the amount has been changed from 150 yen to 50 yen.

- Dividends per share from FY2020 to FY2023 are calculated on the assumption that the stock split was conducted at the beginning of FY2020.
- FY2023 includes the 60th anniversary commemorative dividends.
- Amounts before the stock split are shown in parentheses.

Implemented a 3-for-1 common stock split on April 1, 2023.
Full-year dividends are expected to be 618 yen per share

5. Sustainability

Sustainability Initiatives

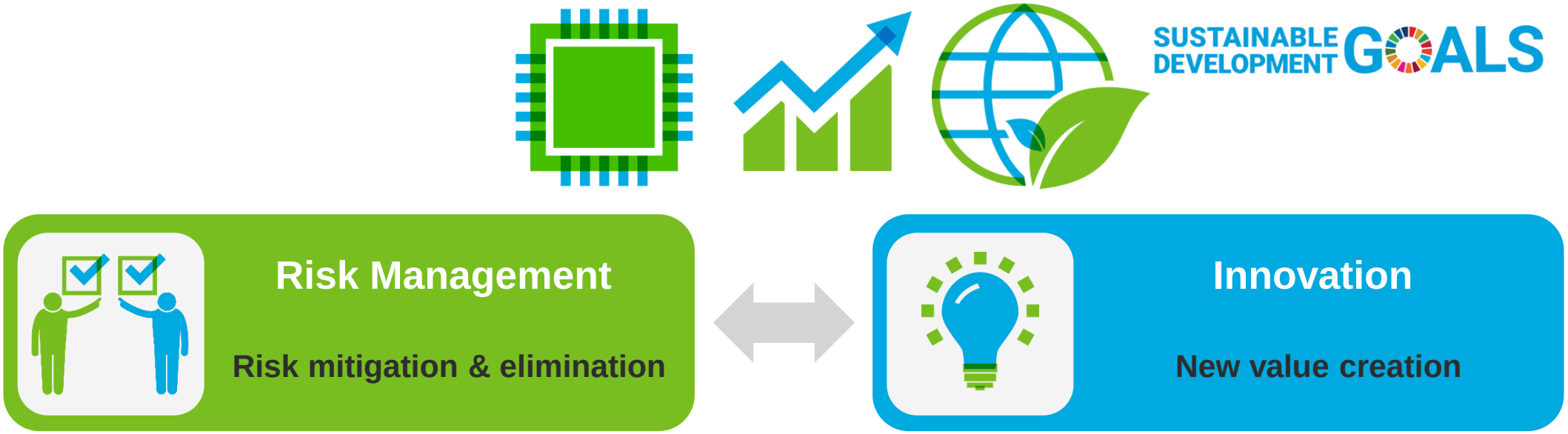
The 14 material issues (key issues) that require prioritized attention and actions are identified to implement sustainability initiatives through our business operation and contribute to the resolution of industrial and social issues.

SUSTAINABLE DEVELOPMENT GOALS

- Respect for Human Rights
- Climate Change and Net Zero
- Product Energy Efficiency
- Best Products with Innovative Technology
- Best Technical Service with High Added Value
- Customer Satisfaction and Trust
- Supplier Relationship

- Employee Engagement
- Safety First Operation
- Quality Management
- Compliance
- Ethical Behavior
- Information Security
- Enterprise Risk Management

Risk Management



TCFD TASK FORCE ON CLIMATE-RELATED FINANCIAL DISCLOSURES

Sustainability-focused management aiming to remain a company that is loved and trusted by all stakeholders. Promotion of technological innovation of semiconductors and reduction of environmental impact in supply chain

Environmental Approaches

Net Zero

New target **Scope 1, 2 & 3** **by 2040**

Scope 1&2: CO2 Emissions from energy use such as electricity in business activities

Scope 3 : CO2 Emissions from the use and disposal of sold equipment, material purchases and logistics, etc.

E-COMPASS

Environmental Co-Creation by Material, Process and Subcomponent Solutions

Semiconductors	Products	Business activities
Higher device performance and lower power consumption	Compatibility of equipment process performance and environmental performance	Reduction of CO2 emissions in all business activities

Promoting technological innovation of semiconductors and reducing environmental impact throughout the supply chain

Safety & Quality

Safety

Under the “Safety First” slogan, everyone at Tokyo Electron, from top management to field representative, is actively and continuously improving safety and promoting health, giving safety and health the highest priority when carrying out different types of operations such as development, manufacturing, transportation, installation and maintenance.

Safety Goals
(by FY2027)
TCIR ≤ 0.1

TCIR: Total Case Incident Rate（Number of workplace injuries per 200,000 work hours）

Incident Prevention Initiatives

- Experiential training and VR (Virtual Reality)
- Comprehensive safety inspections
- Feedback on safety specifications
- Safety activities for suppliers

Quality

The Tokyo Electron Group seeks to provide the highest-quality products and services. This pursuit of quality begins at development and continues through all manufacturing, installation, maintenance, sales and support processes. Our employees must work to deliver quality products, quality services and innovative solutions that enable customer success.

Quality Policy

1 Quality Focus

2 Quality Design and Assurance

3 Quality and Trust

4 Continual Improvement

5 Stakeholder Communication

TEL Values as codes of conduct

Engagement

Career

Corporate growth is enabled by people, and our employees both create and fulfill company values

Retention

Work-life balance

Diversity, Equity and Inclusion

3Gs

Global・Generation・Gender

Human Rights Initiatives

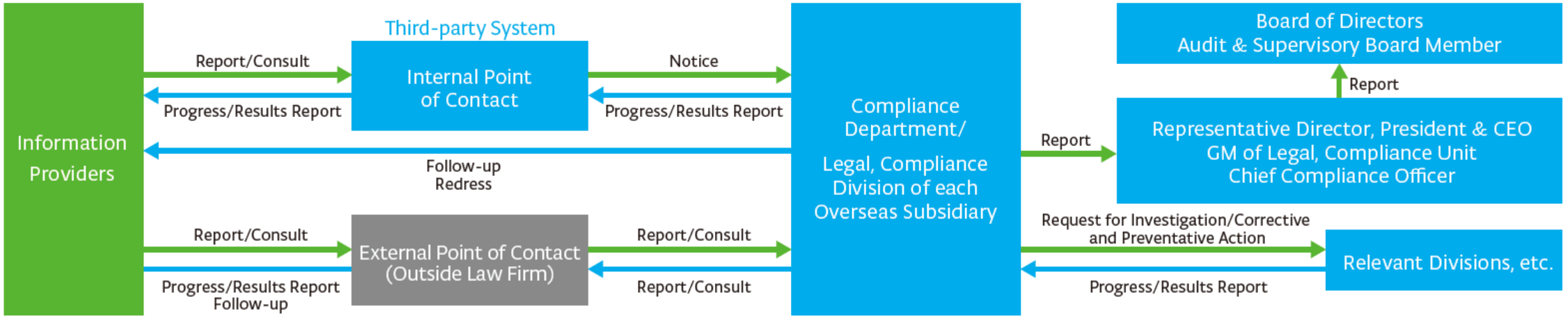
The five focus areas in human rights (Tokyo Electron Group Human Rights Policy)

- Freedom, equality & non-discrimination
- Freely chosen employment
- Product safety & workplace health and safety
- Freedom of association
- Appropriate working hours & breaks/ holidays/vacations

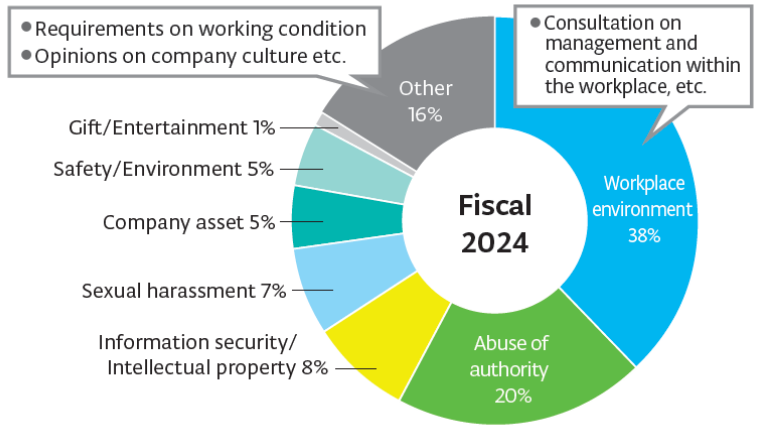
Human Rights Due Diligence

Commitment	Assessment	Remediation	Report
Commitment to respecting human rights	**Assessment of human rights risks in business and supply chains**	**Actions to reduce risks based on assessment results**	**Regular disclosure of information**
▪ Revision of Tokyo Electron Group Human Rights Policy ▪ Awareness and implementation ▪ Education	▪ Human rights risk assessment ▪ Human rights impact assessment	▪ Feedback sheet publication ▪ Program development and review according to issues	▪ Publication of the Integrated Report ▪ Postings on the website

Internal Reporting System



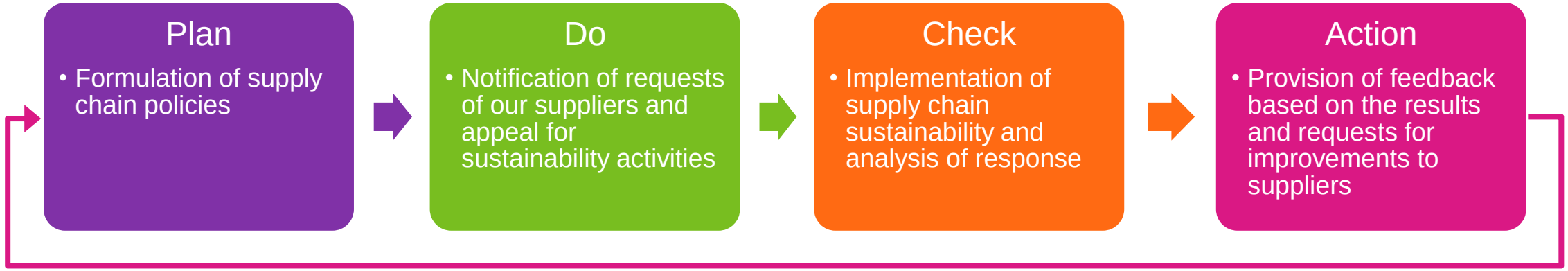
Breakdown of Report/Consultation Contents



Respect for human rights with a strong sense of integrity

Supply Chain Management

Supply chain sustainability process

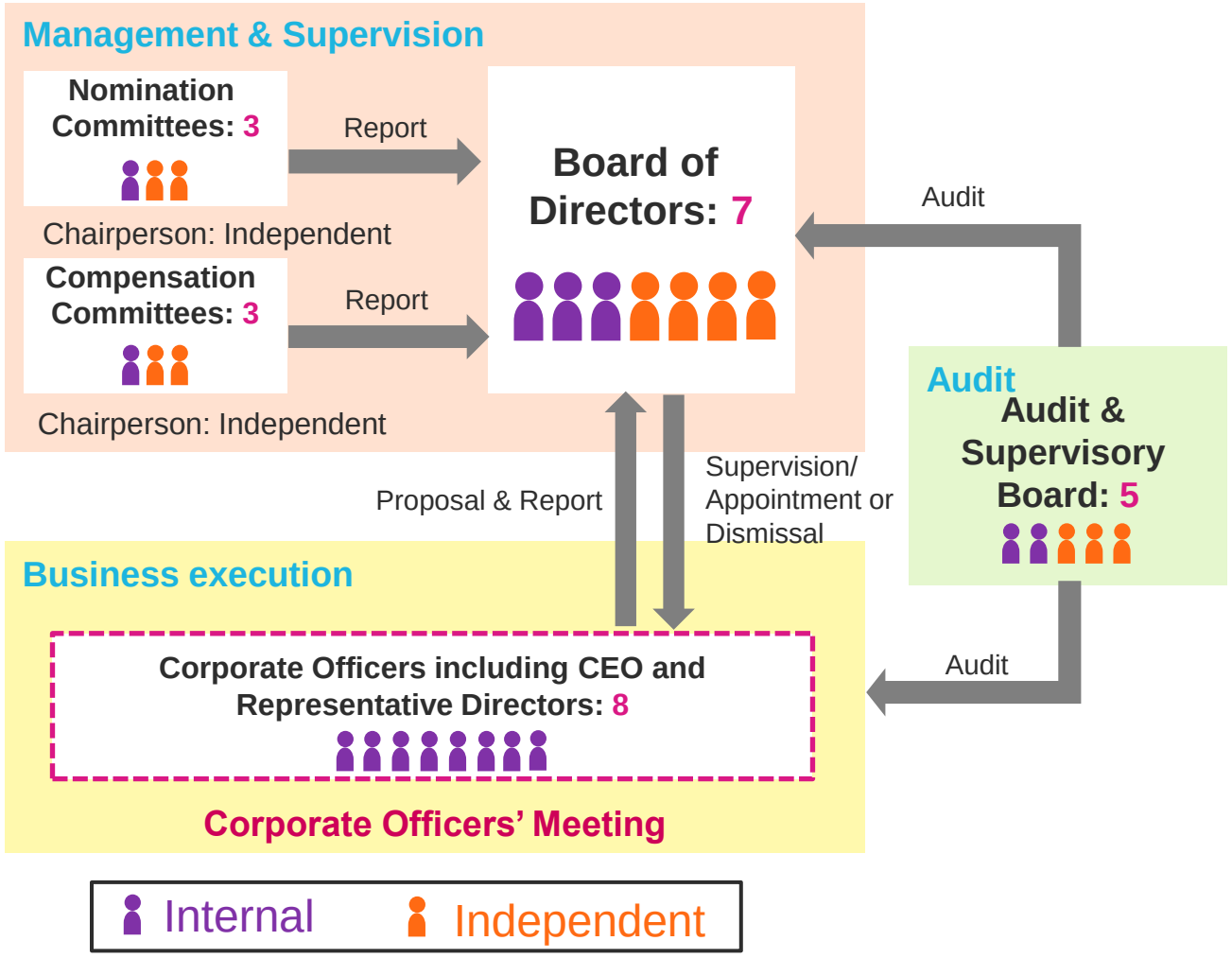


- Annual Sustainability Assessment
  - Assessment base on RBA code of conduct
  - Corrective Action Plans
- RBA Audit
  - At primary manufacturing sites
  - Continuous improvement in respective operations

Pursuit of sustainability conscious operations throughout the supply chain

Corporate Governance Framework (Audit & Supervisory Board System)

＜Framework (Excerpt)＞



The era of ultra VUCA

↓

Sharp growth of the semiconductor market

↓

Need to improve the **quality** and **speed** of decision making in both "**Management & Supervision**" and "**Business execution**"

↓

Strengthen and optimize 3 functions:

1) In-depth discussion of mid- to long-term growth strategies
2) Supervision of business execution
3) Decision-making on business execution

Accelerate "proactive management"

Growth of short-/mid-/long-term profits

Increase corporate value continually

Evaluation of the Effectiveness of the Board of Directors

Internal and external experts analyze and evaluate the effectiveness of the Board of Directors

Global Initiatives

Sustainable Development Goals (SDGs)

Clarify initiatives through business by materiality and deploy company-wide

Tokyo Electron supports the SDGs

Participation in International Initiatives

Signed the UN Global Compact, joined the Responsible Business Alliance (RBA), endorsed the Task Force on Climate-related Financial Disclosures (TCFD)

WE SUPPORT UN GLOBAL COMPACT

Responsible Business Alliance
Affiliate Member

TCFD TASK FORCE ON CLIMATE-RELATED FINANCIAL DISCLOSURES

External Evaluation on our ESG Initiatives

Highly rated by evaluation organizations around the world

Member of Dow Jones Sustainability Indices
Powered by the S&P Global CSA

FTSE4Good

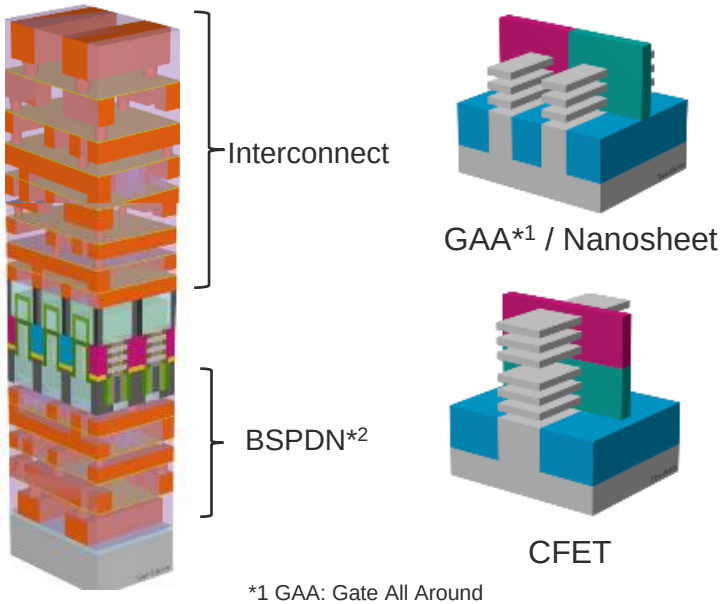
2024 MSCI ESG Leaders Indexes Constituent

6. Diversifying Semiconductor Technology

~ Technology Roadmap~

Semiconductor Devices: Direction of Development

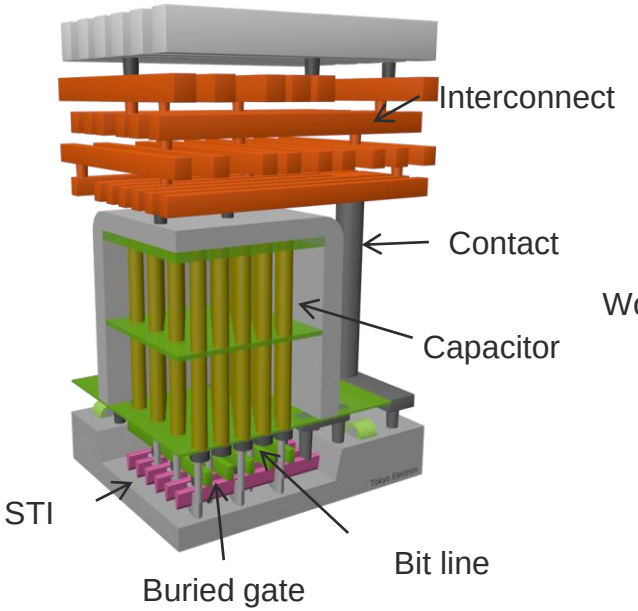
Logic



*1 GAA: Gate All Around
*2 BSPDN: Backside Power Delivery Network
*3 CD: Critical Dimension

Through miniaturization with structural changes
- Lowered cost per transistor
- Lower power consumption
- Higher speed

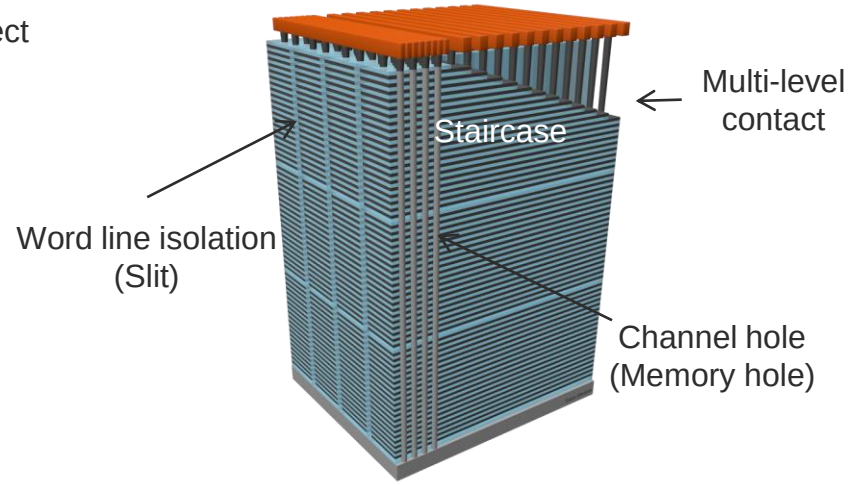
DRAM



Through miniaturization
- Lower cost per bit
- Lower power consumption
- Higher speed

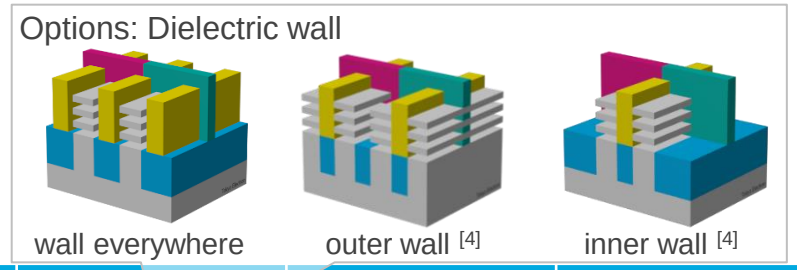
Through new structures
- Lower cost per bit

NAND



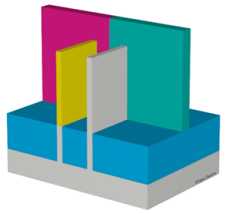
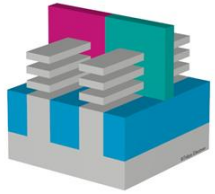
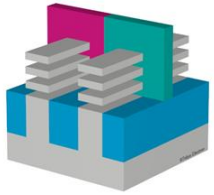
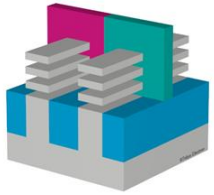
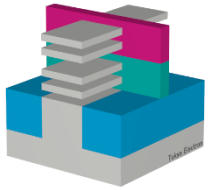
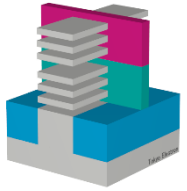
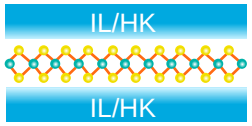
Through high stacking
- Lower cost per bit

Logic Technology Roadmap (Generic)



[1] Chih-Hao Chang (TSMC) et al., IEDM 2022
[2] Shien-Yang Wu (TSMC) et al., IEDM 2022
[3] Sandy Liao (TSMC) et al., IEDM 2024
[4] Mertens and Horiguchi (imec), EDTM 2024

Source: TEL estimates

Year of HVM (20k/month)	2022~24	2025~2026	2027~28	2029~30	2031~32	2033~34	2035~36	2037~38
Node	**3nm**	**2nm/18A/16A**	**14A**	**10A**	**7A**	**5A**	**3A**	**2A**
Transistor	2~1 Fin 	GAA NS 	GAA NS scaling 	GAA NS extension 	CFET 	2nd Gen. CFET 	3rd Gen. CFET 	2D material stack  2D material: TMDC MoS_2, WS_2, $MoSe_2$, WSe_2 etc.
Poly Pitch [nm]	48~45 [1]		45~42		48 [3] ~42	45~39		36
Min. Metal Pitch [nm]	23 [2]		20	18	17	16	14	12
Interconnect booster	Cu Barrier/Seed CIP Backside PDN (HPC)			Cu CIP or Ru subtractive	Ru subtractive AR>3, Airgap	New alloy AR>5, Airgap, BEOL Transistor		
EUV Patterning Technology	EUV MP*1, SE*2			EUV MP, SE High-NA SE		High-NA MP, SE EUV MP, SE		
Resist	CAR*3			CAR (+MOR*4)	CAR+MOR			

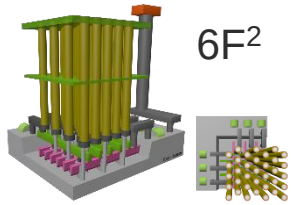
*1 MP: Multi-Patterning, *2 SE: Single-Exposure, *3 CAR: Chemically Amplified Resist, *4 MOR: Metal Oxide Resist

Logic scaling will continue by changing transistor structure and material evolution

DRAM Technology Roadmap (Generic)

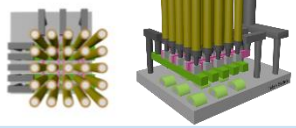
Source: TEL estimates

Year of HVM (20k/month)	2023-24	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
Node	1b	1c	1d	0a		0b	0c		0d		0e	
Cell layout / Structure	2D									3D		
F [nm] in $6F^2$	13~12.5	12~11	10	9		8	7		(3D ~1xxL)		(3D >1yyL)	
Cap. pitch [nm]	39~37.5	36~33	30	27		24	21					
Cap. A.R.	>50	>55	>65	>70		>75	>80					
Cap. Mat.	ZrAlHfO					Alternative (HfZrO Anti Ferro. etc)						
WL	TiN			Low R metal								
Peri. CMOS	HKMG									FinFET		
HBM	HBM3E (8/12Hi,24/36GB)		HBM4 (12/16Hi,36/48GB)		HBM4E (16Hi,64GB)		HBM5 (16,20Hi, 64/80GB)		HBM5E		HBM6	



$6F^2$

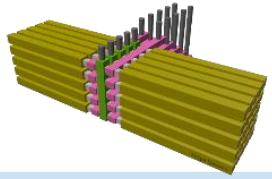
$4F^2$ VCT* [1,2]

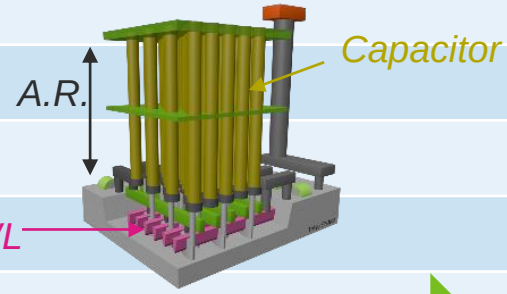


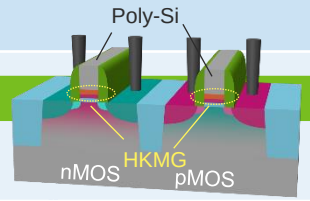
* Vertical Channel Transistor

[1] Seokhan Park (Samsung) et al., IEDM 2023

[2] Daewon Ha (Samsung) et al., IEDM 2023





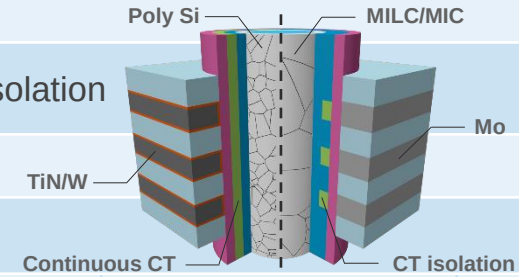


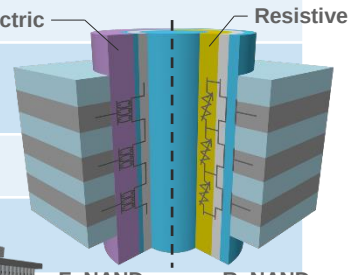
Bonding

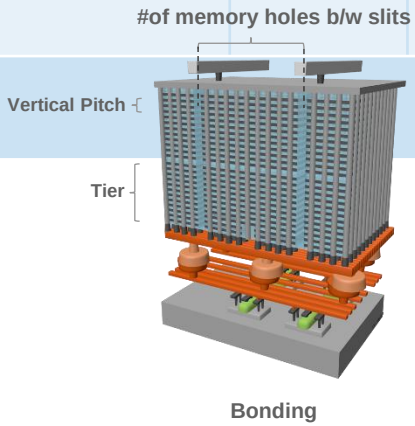
NAND Technology Roadmap (Generic)

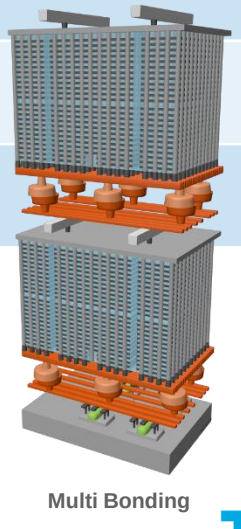
Source: TEL estimates

Year of HVM (20k/month)	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
Stack (~1.3x/1.5years)	3xxL		4xxL	5xxL		7xxL	1xxxL		*1yyyL	*1zzzL		*2xxxL
Tier	2 or 3		3 or 4	3 or 4		3 - 5	4 - 6		5 - 7	6 - 8		7 - 10
Vertical pitch [nm]	39 - 45		38 - 43	38 - 42		37 - 41	36 - 40		35 - 39	34 - 38		33 - 37
Memory height [μm]	12 - 14		15 - 19	18 - 27		24 - 36	34 - 45		45 - 62	57 - 74		70 - 84
Charge trap (CT)	Continuous CT					CT isolation				Fe/Re NAND[3]		
Channel	Poly Si grain CIP			MILC[1]/MIC[2]								
WL metal	W or Mo		Mo									
Layout/Structure	Under array or Bonding		Bonding			Bonding or Multi Bonding						
Peri. CMOS	Poly Si Gate					HKMG						





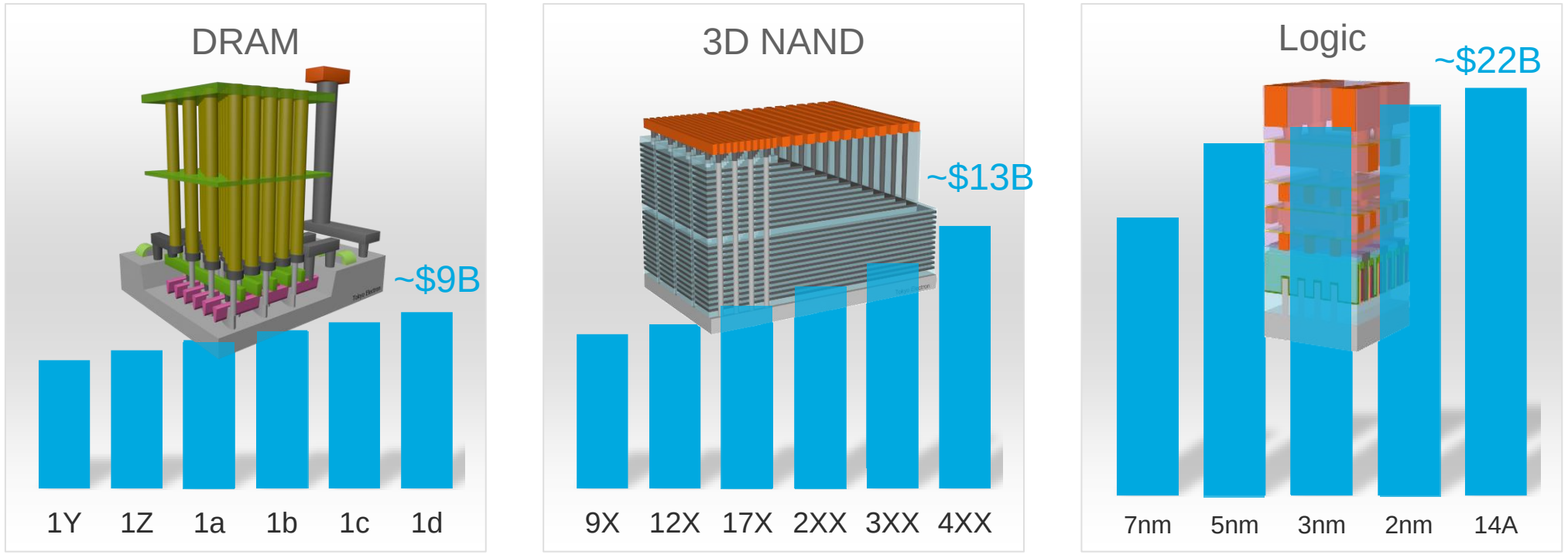




* Trend Extrapolation
[1] Metal induced lateral crystallization, N. Ishihara (Kioxia) et al., VLSI 2023
[2] Metal induced crystallization
[3] Jeehoon Han (Samsung) et al., IEDM 2023

Raising Added-value in SPE

WFE investment (100k WSPM*, Greenfield/TEL estimates)



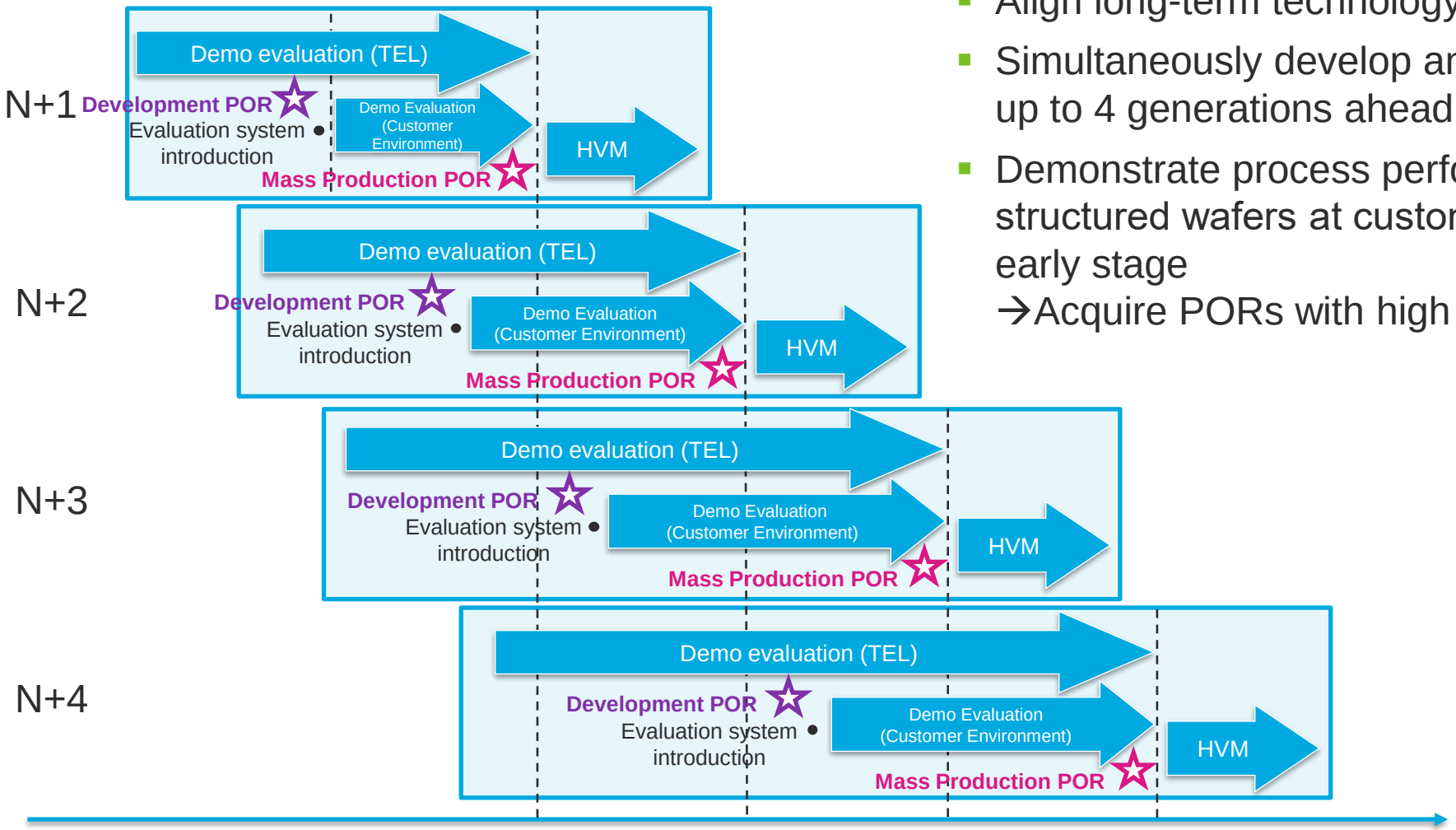
Expanding business opportunities for SPE manufacturers on arrival of new applications and rising level of technological difficulty

* WSPM: Wafer starts per month

7. SPE New Equipment Initiatives

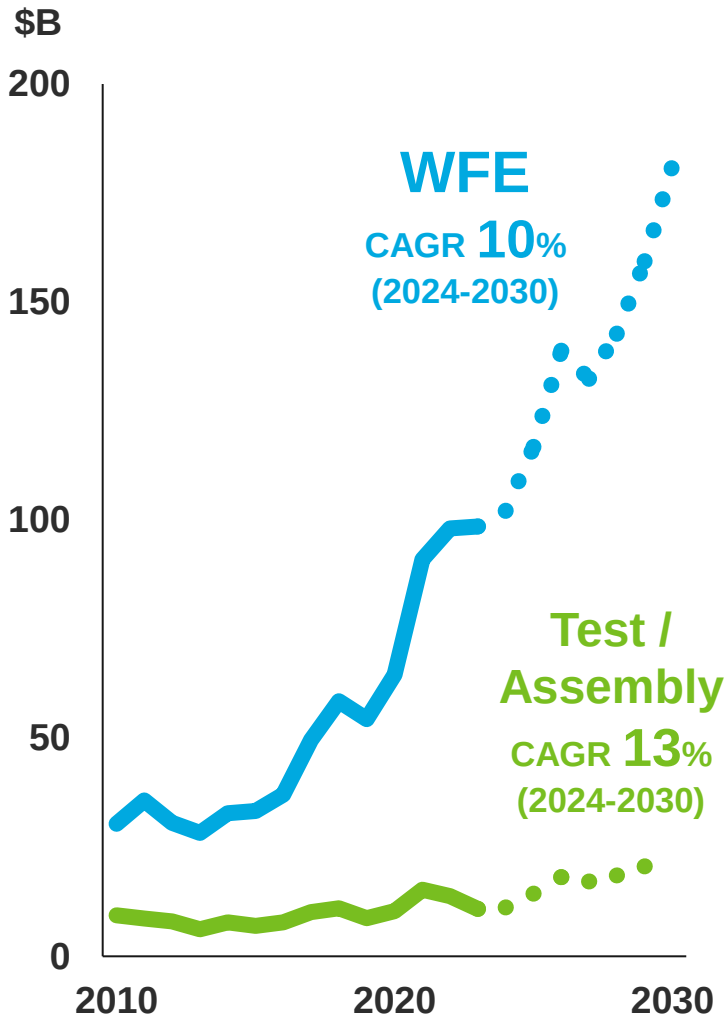
Development Efforts

Simultaneous 4-Generation Developments



- Align long-term technology roadmap with customers
- Simultaneously develop and evaluate technologies up to 4 generations ahead
- Demonstrate process performance on customer structured wafers at customer's environments at early stage
  →Acquire PORs with high value-added products

Our Growth Opportunities in the Frontend Market



Source : TechInsights

- CAGR driven by AI-related devices to continue to drive high growth of WFE’s CAGR
- Leveraging TEL's strengths to address high-growth market areas:
  - Leading-edge logic: The etch market is expected to grow by 2.7 times, the deposition market by 2.5 times*
  - DRAM: The etch market is expected to grow by 2.3 times, exceeding the CAGR of WFE*
- By introducing new products focused on the key technological inflection points, we aim to further expand our areas of entry

* TEL Estimates

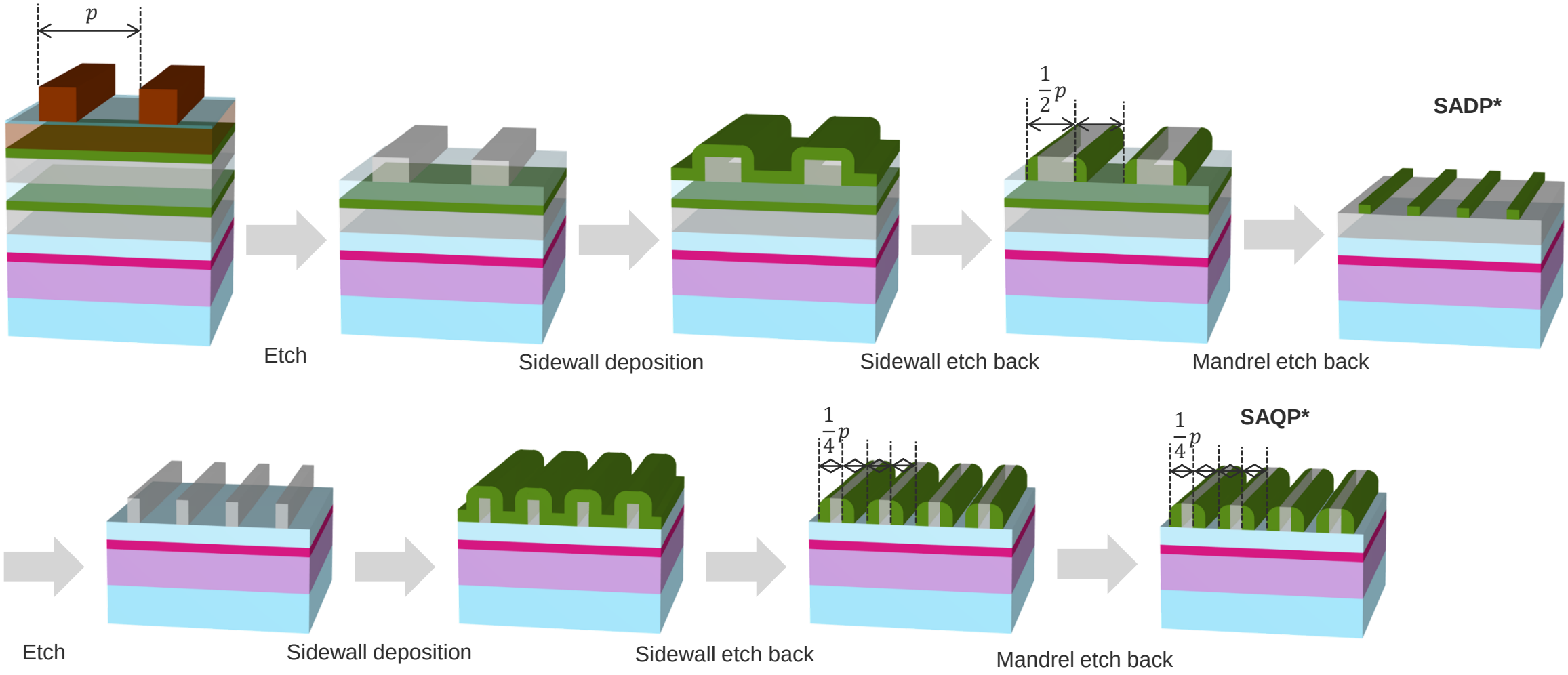
Growth opportunities at Technological Inflection Points in Frontend Process

- Logic: GAA*1, BSPDN*2, CFET
  - Adaption of High-NA lithography, combined with multi-patterning and MOR technologies, presents opportunities for new technology Acrevia™
  - Adoption of multi-patterning to increase demand for deposition, etch, and cleaning processes.
  - GAA and CFET transistors to drive an increase in gas chemical etch processes
  - New materials like ruthenium and structural innovations such as air gaps to generate fresh opportunities
- DRAM: HBM, VCT*3, 3D DRAM
  - Adoption of multi-patterning driving increased demands in deposition and etch
  - Capacitor formation remains essential, driving ongoing demand for advanced etch and deposition
  - 3D DRAM leading to increased processes in deposition, etch and gas chemical etch
- NAND: Beyond 4xx
  - Increased layer counts leading to higher investments in deposition and etching processes
  - High aspect ratio etch to become increasingly important
  - New materials such as molybdenum, and low-resistance channel silicon to be utilized

*1 GAA: Gate All Around
*2 Backside PDN: Backside Power Delivery Network
*3 VCT: Vertical Channel Transistor

7-1. Frontend, Patterning Technologies

Self-aligned Multiple Patterning to Supplement Lithography

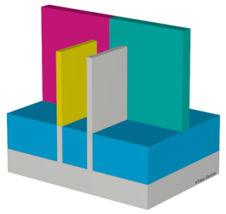
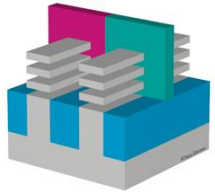
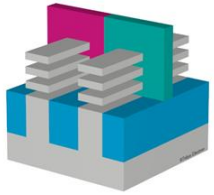
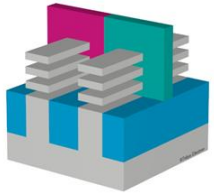
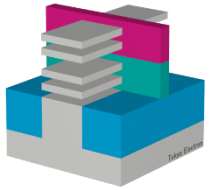
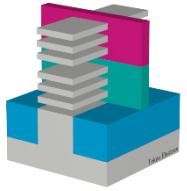
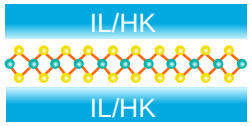


SADP: Self-aligned double patterning
SAQP: Self-aligned quadruple patterning

EUV Lithography Technology Roadmap in Logic

[1] Chih-Hao Chang (TSMC) et al., IEDM 2022
[2] Shien-Yang Wu (TSMC) et al., IEDM 2022
[3] Sandy Liao (TSMC) et al., IEDM 2024
[4] Mertens and Horiguchi (imec), EDTM 2024

Source: TEL estimates

Year of HVM (20k/month)	2022~24	2025~2026	2027~28	2029~30	2031~32	2033~34	2035~36	2037~38
Node	**3nm**	**2nm/18A/16A**	**14A**	**10A**	**7A**	**5A**	**3A**	**2A**
Transistor	2~1 Fin 	GAA NS 	GAA NS scaling 	GAA NS extension 	CFET 	2nd Gen. CFET 	3rd Gen. CFET 	2D material stack  2D material: TMDC MoS_2, WS_2, $MoSe_2$, WSe_2 etc.
Poly Pitch [nm]	48~45 [1]		45~42		48 [3] ~42	45~39		36
Min. Metal Pitch [nm]	23 [2]		20	18	17	16	14	12
EUV Patterning Technology	EUV MP, SE			EUV MP, SE **High NA SE**		**High NA MP, SE** EUV MP, SE		
Resist	CAR			CAR (+**MOR**)		CAR+**MOR**		

MP: Multi-Patterning, SE: Single-Exposure, CAR: Chemically Amplified Resist, MOR: Metal Oxide Resist

Enhancing versatility of coater/developer to respond to future EUV lithography technologies including MOR and high-NA EUV

Coater/Developer: CLEAN TRACK™ LITHIUS Pro™ Z for EUV

LITHIUS Pro™ Z released in 2012
(＞3000 systems shipped)

New features to support EUV CAR*1/MOR*2
to be released as on an ongoing basis

High Reliability
High share in EUV market

High Productivity
Maximizes output of EUV lithography tools, and reduces chemical consumption

High Versatility
Supports CAR, MOR and underlayers

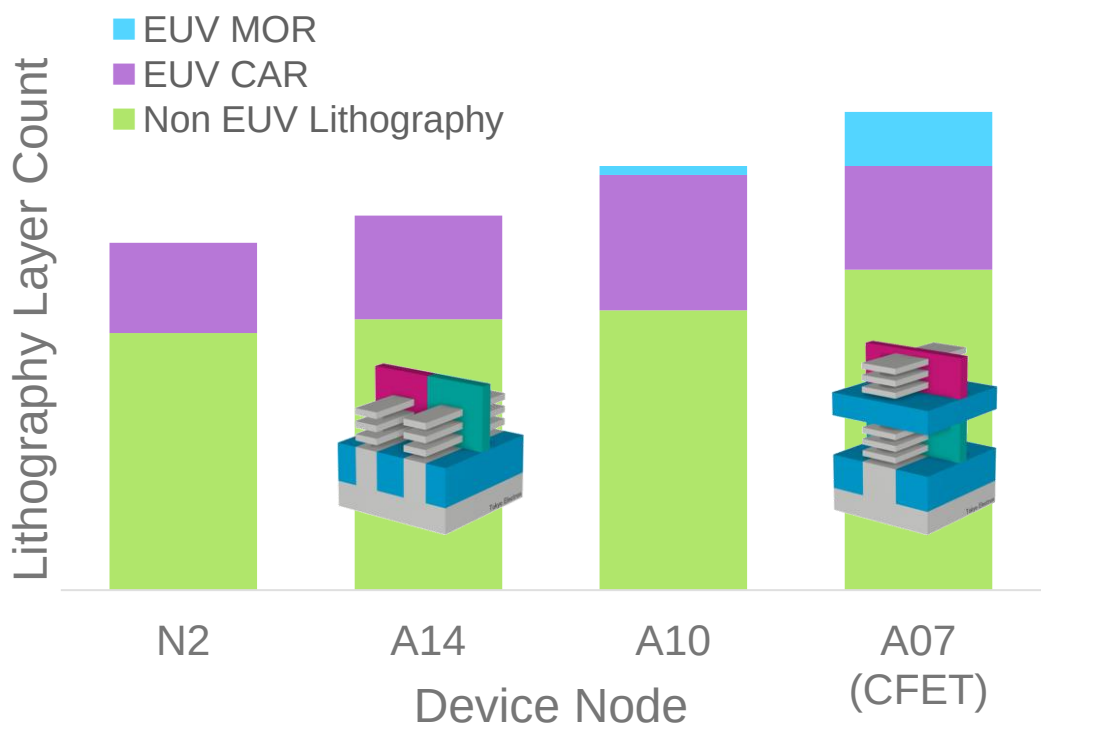
*1 CAR: Chemically Amplified Resist
*2 MOR: Metal Oxide Resist

LITHIUS Pro™ Z platform with its proven mass production for various litho tools, ensures high reliability and productivity for EUV litho, along with high versatility for next-generation EUV

Outlook on Lithography Layer Count

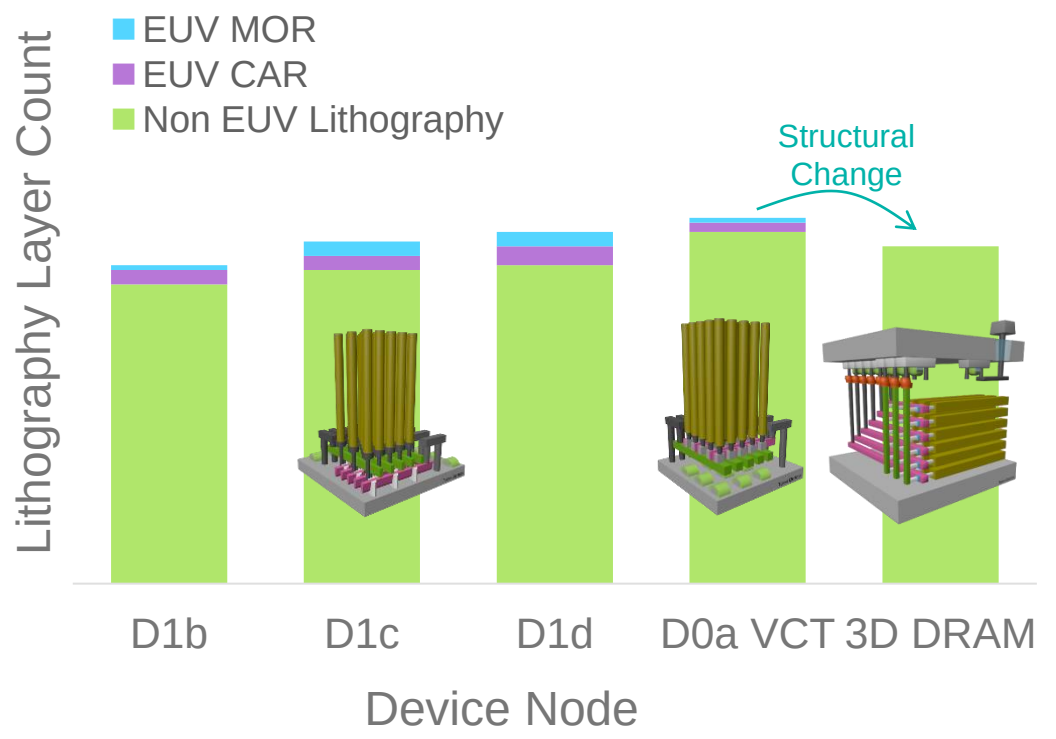
Logic

TEL Estimates



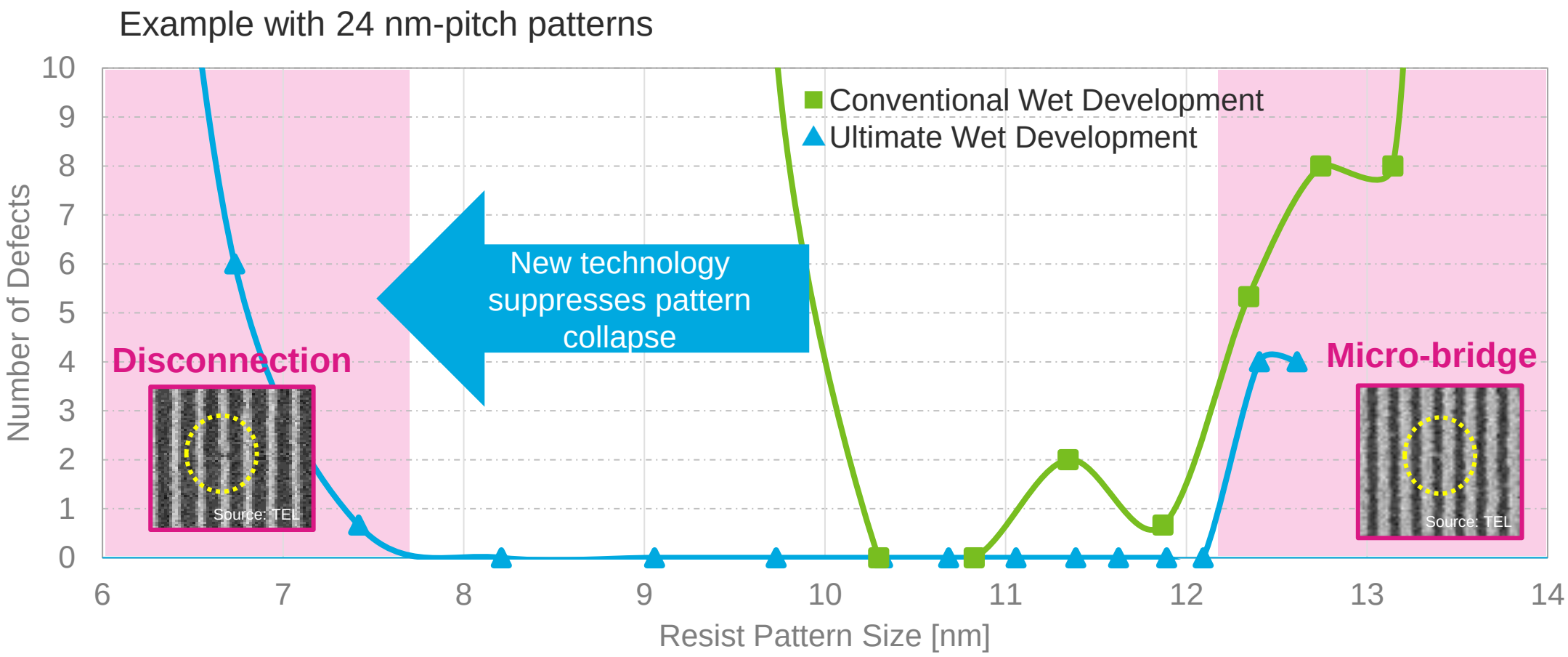
DRAM

TEL Estimates



MOR expected for Logic 10A/ DRAM D1b, development ongoing for MOR

Example of MOR Process: The Ultimate Wet Development



The Ultimate Development technology enables the suppression of pattern collapse

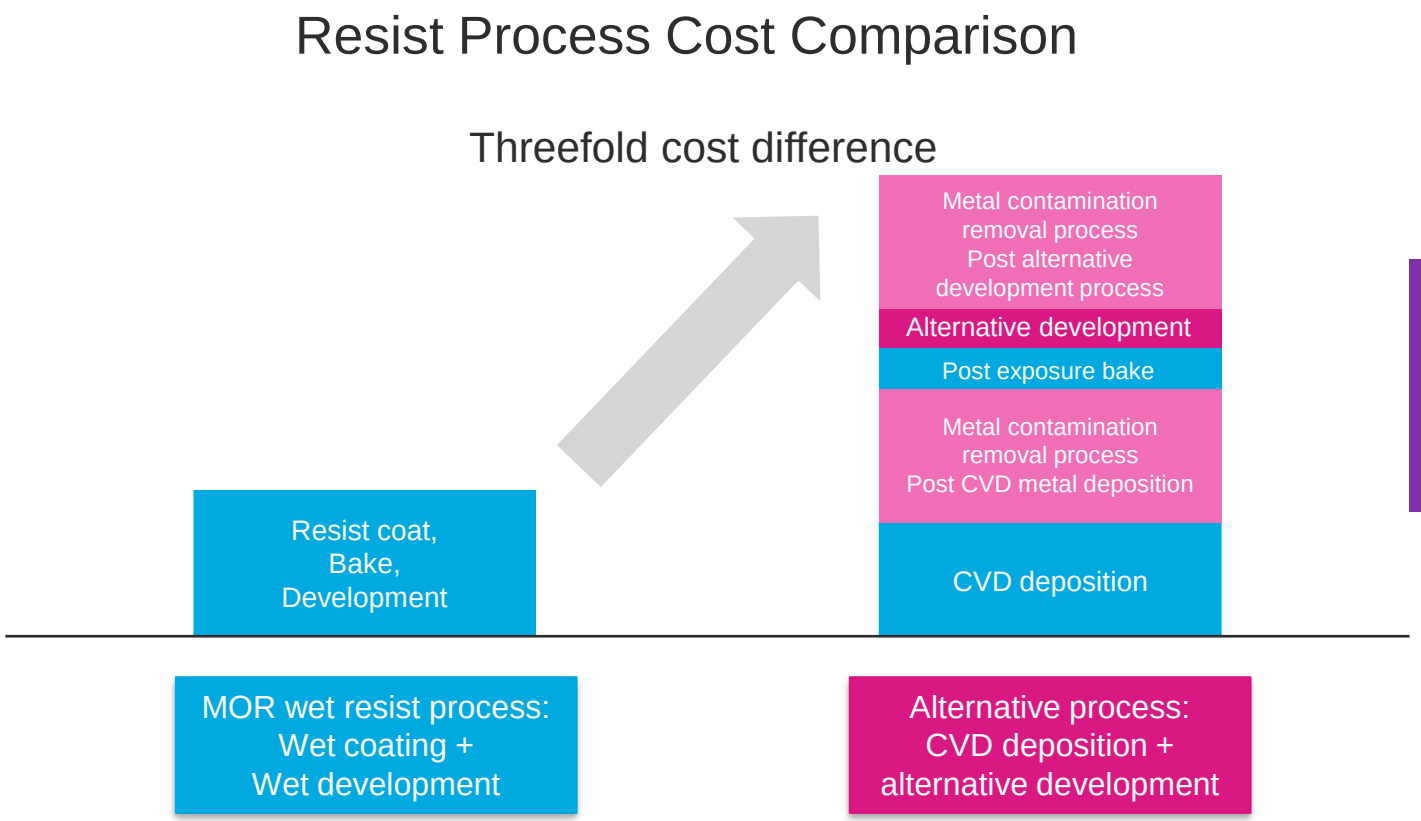
Example of MOR Solution: The Ultimate Wet Development

*1 Based on internal information and development targets
*2 Based on results of developing 24 nm-pitch lines

	Ultimate Wet Development Technology	Conventional Wet Technology	Alternative Technology
Base Technology	Coater/Developer	Coater/Developer	Etch
Process Ambient	Atmospheric	Atmospheric	Vacuum
Reaction	Chemicals	Chemicals	Corrosive Gas
Throughput*1	4x	4x	1x
Chemical Consumption*1	50% (vs. conventional)	100 %	N/A (uses gas) exhaust processed in combustion abatement post process
Anti-Pattern Collapse*1 Performance	< 8 nm*2	> 10 nm*2	< 8 nm*1
Footprint*1	In-Line	In-line	Additional Footprint

Evaluation of Ultimate Wet Development ongoing with key customers, with emphasis on productivity (throughput, footprint, maintainability, utilize existing facilities)

Cost Comparison of MOR Wet Resist Process to Alternative Process



The CoO of CVD deposition & alternative development process is around three times higher than that of wet coating and development

TEL estimates

MOR wet resist process is superior to alternative process (CVD & alternative development) not only in terms of operational advantages including cost, TAT, queue time management, equipment footprint and power consumption, but the wet process also demonstrates superior data in terms of process performance

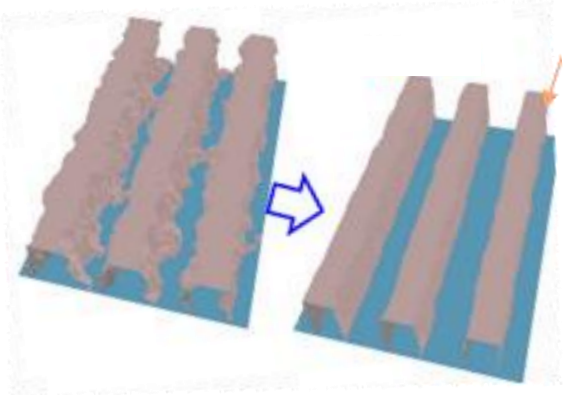
Acrevia™

TEL's Original Gas Cluster Beam (GCB) System

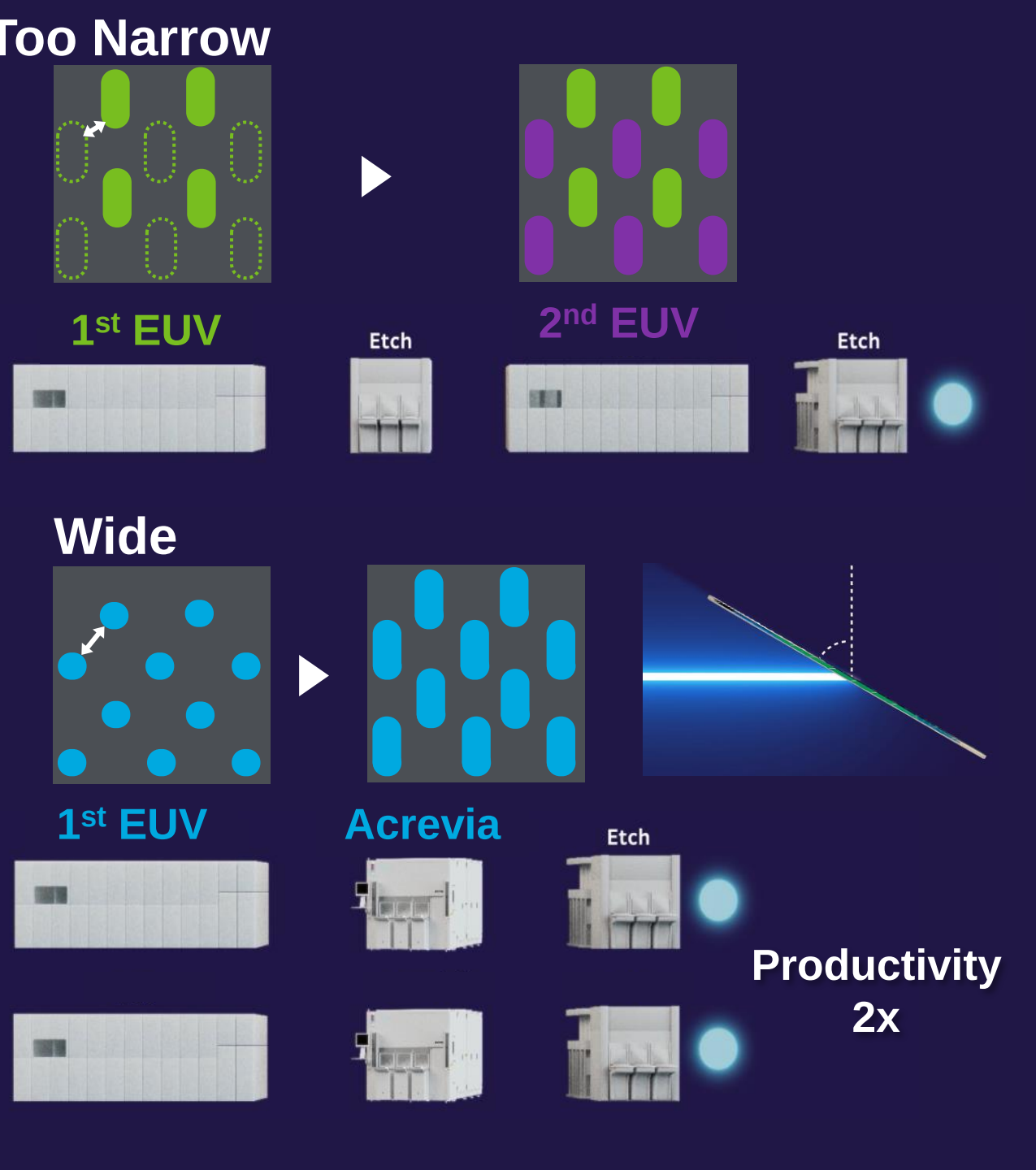
- Beam Angle is freely Adjustable
- LSP（Location Specific Processing）Wafer Scan
  → Enable 3 Dimetional Etching

✓ Drastically Improve EUV productivity
by EUV step reduction with fine patterning

✓ Realize yield by removing defect between pattern and improving LER/LWR*

Before  After

* LER/LWR: Line Edge Roughness / Line Width Roughness

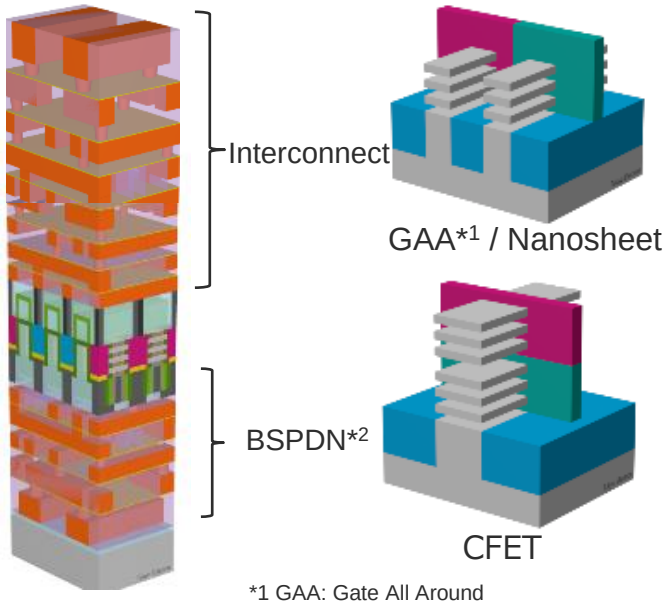


7-2. Frontend, Unit Process

7-2-1. Etch System

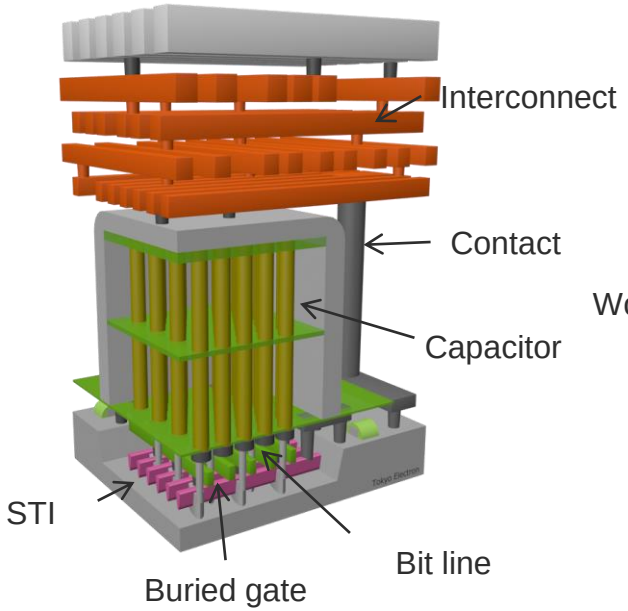
Requirements and Various Etch Technologies

Logic

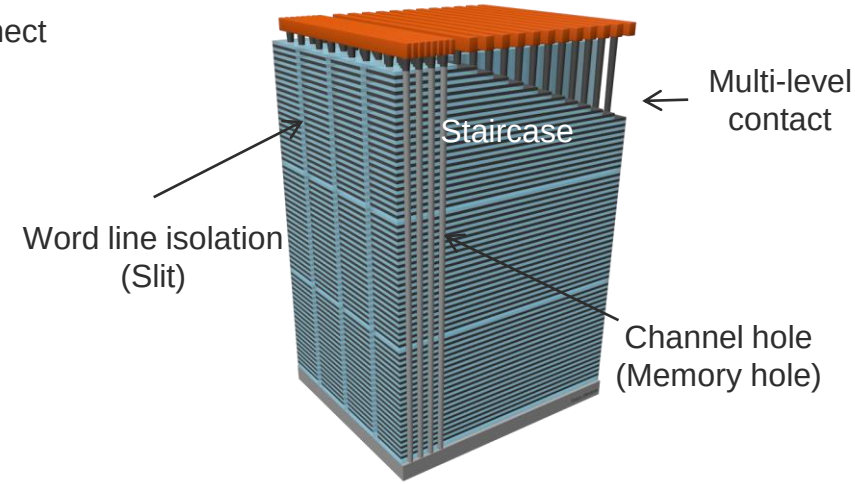


*1 GAA: Gate All Around
*2 BSPDN: Backside Power Delivery Network
*3 CD: Critical Dimension

DRAM



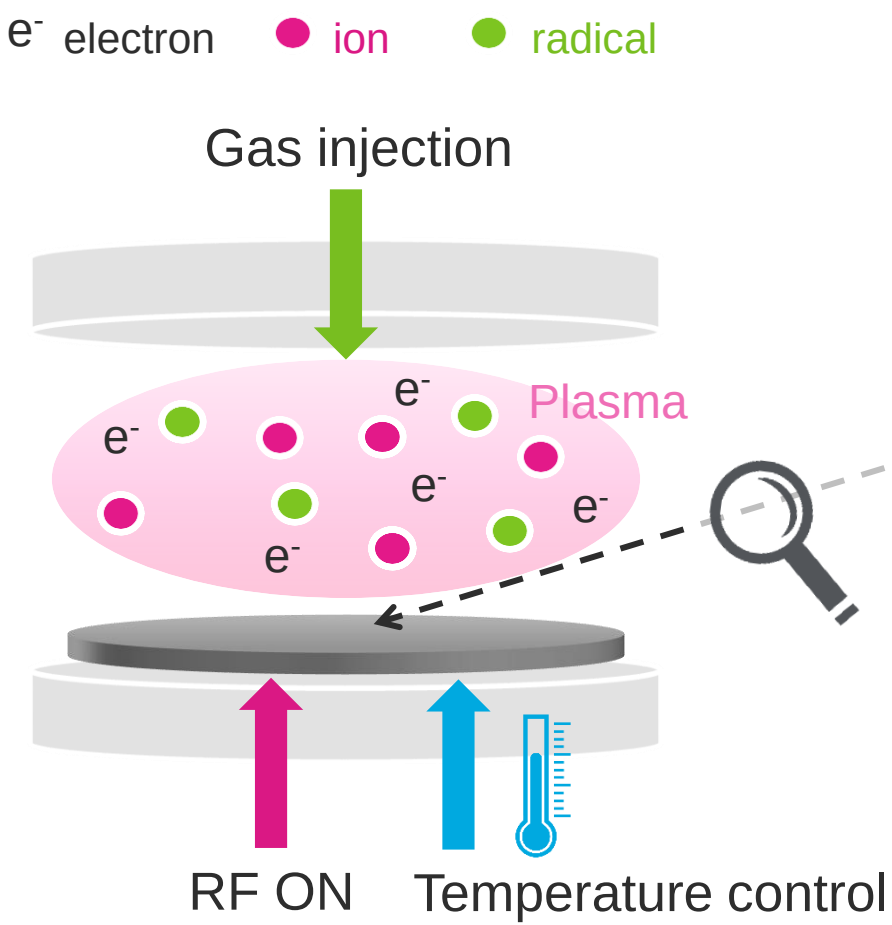
3D NAND



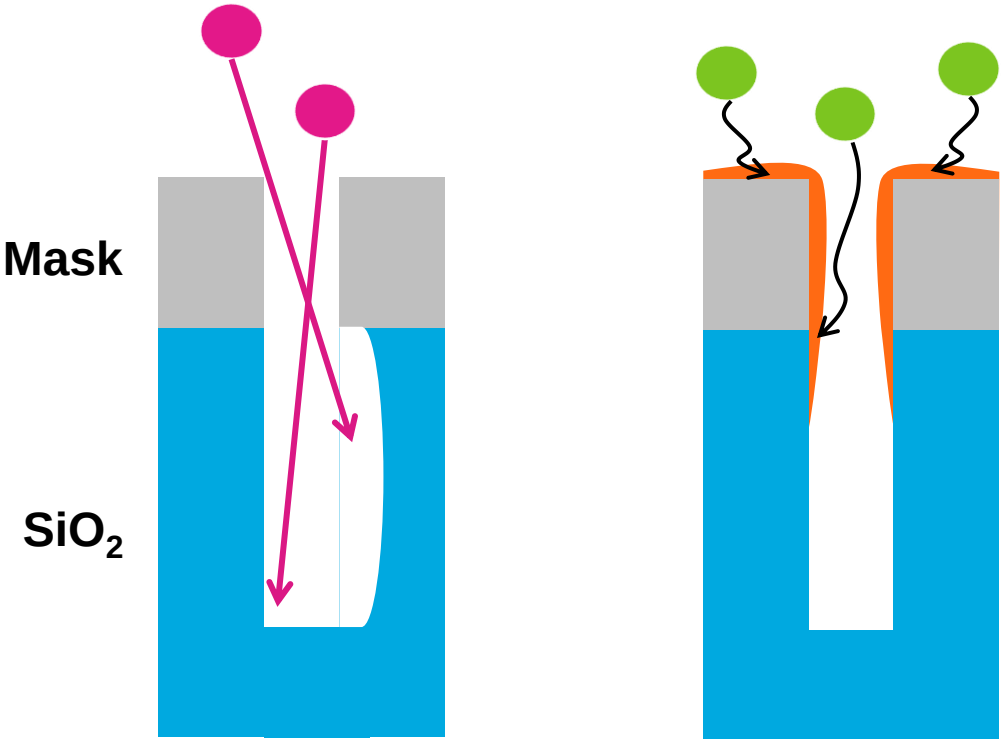
Device trend	Scaling/new structure	Scaling/new structure	Stacking
Technology Required	High selectivity through precise ion control Low-damage process Profile control (vertical, etc.)	Small CD*3, high aspect ratio capacitor etch Scaled mask etch (EUV, multi patterning) HBM (increase in interconnect, etc.)	Fast and vertical high aspect ratio etch Depth monitoring and process control Within wafer uniformity control

Etch technology with precise controllability is required for further evolution of devices

Overview of Etching and Key Parameters



Key Parameters for Etch Controllability



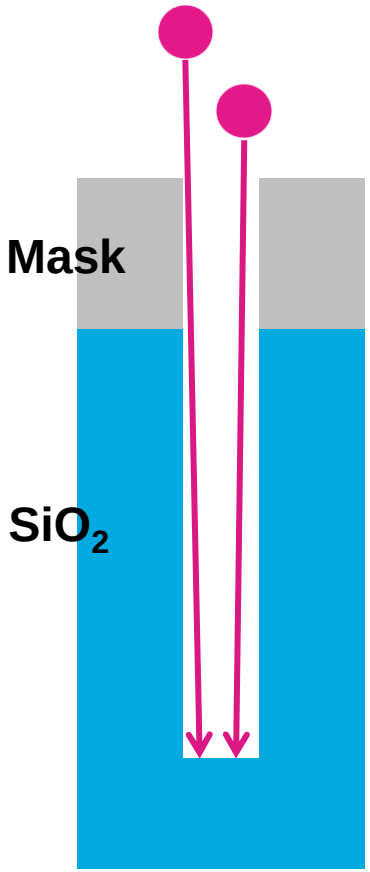
- Ion energy
- Ion incident angle

- Gas species
- Wafer temperature

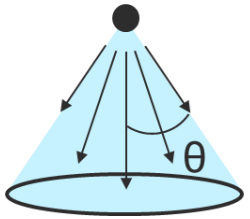
Our Unique Technology 1: HERB™

(HERB™: High Efficiency Rectangular Bias™)

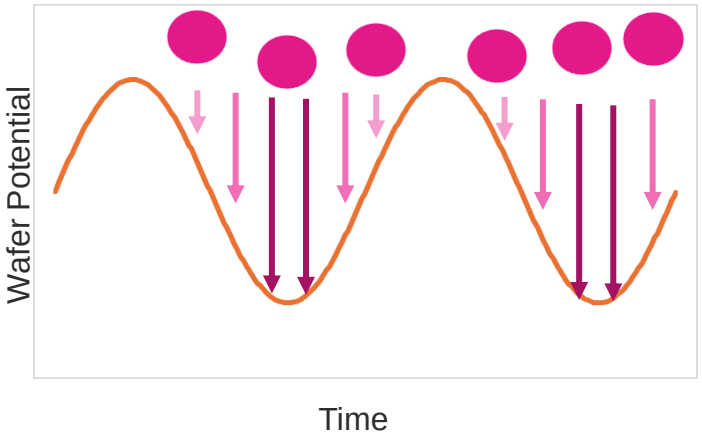
Ion transportation



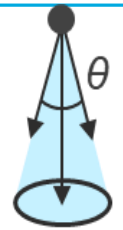
Conventional Technology (Sine wave)



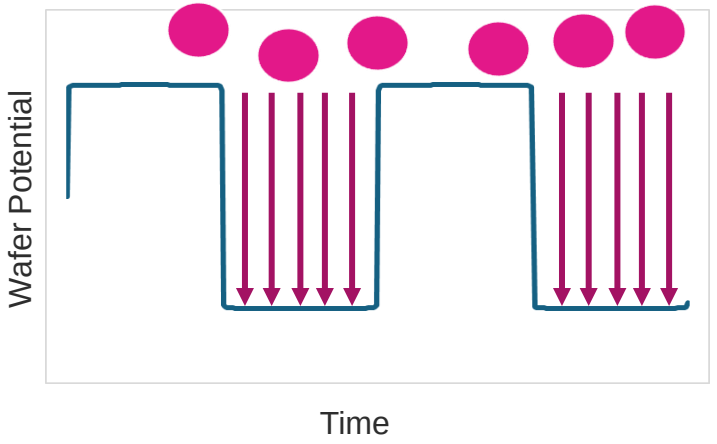
The force attracting ions varies
→incident angle varies



Novel Technology (HERB™)

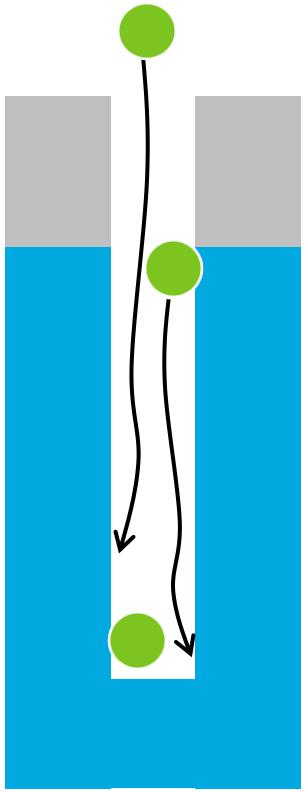


Force attracting ions are strong and consistent
→incidence angle becomes perpendicular

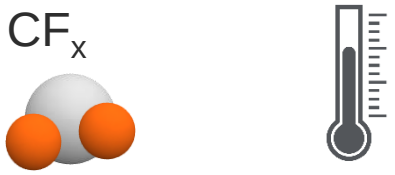


Our Unique Technology 2: PHastIE™

Radical transportation

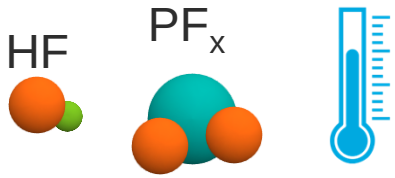


Conventional Technology (CF$_x$ + room temp.)



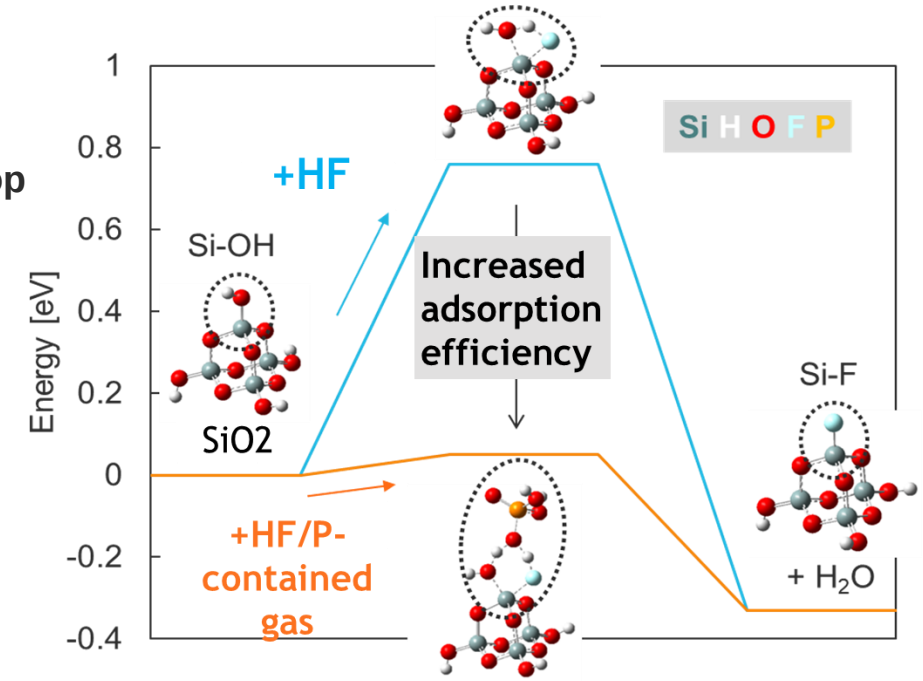
CFx tends to polymerize/adsorb easily
Hinders transportation when accumulated at top

Novel Technology (PHastIE™)



Resolved the issue with novel gas
Achieved high etch rate in combination with low temp.

(PHastIE™: Phosphorus + Hydrogen based “Fast” Ion Etch™)



Novel Cryogenic HARC Etch

Beyond

10μm

2.5x

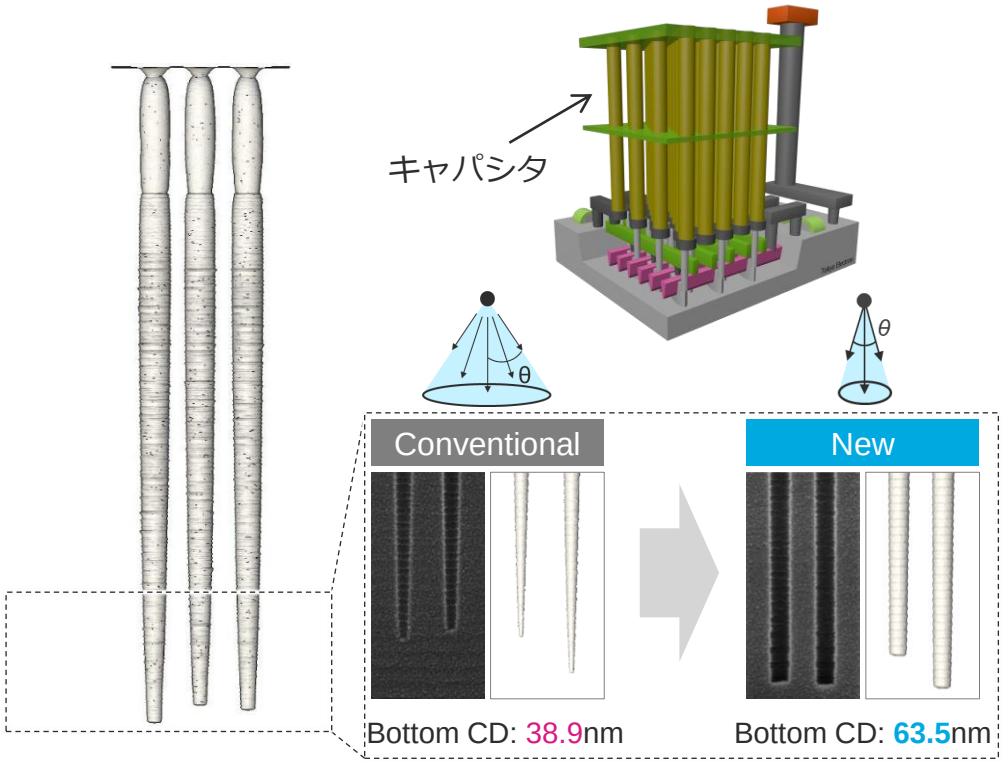
Faster

Process	Environment
Cryogenic temp.	**Power Consumption**
More Linear, Deeper & Faster	Less Power **-43%**
Plasma Control	**CO_2e** **-83%**
Deep-learning Optimization	Less Carbon Footprint

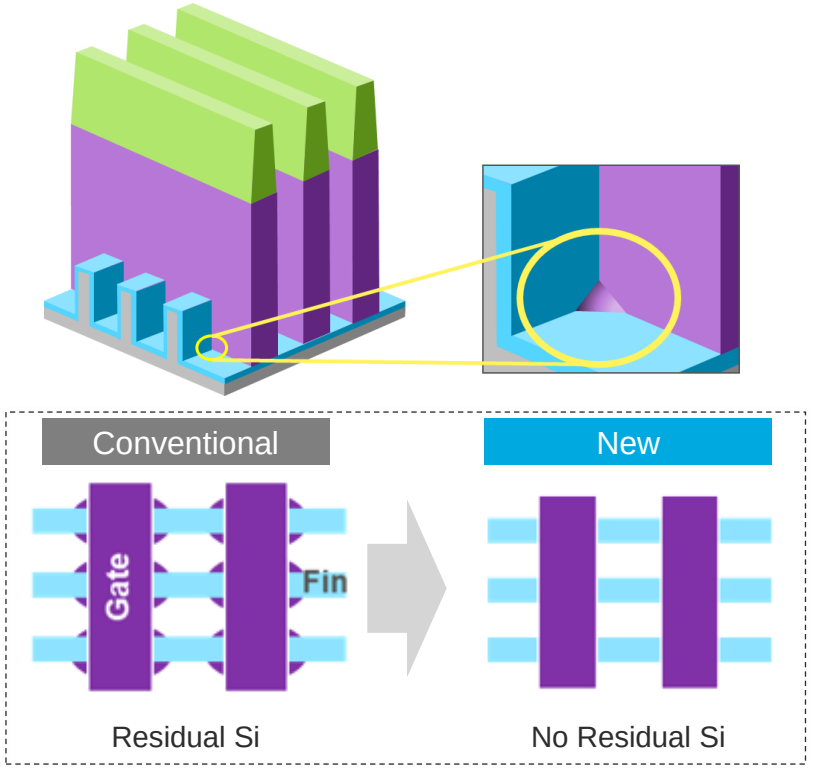
Presented world's first new cryogenic process in 2023 (@VLSI 2023), achieving both high process and environmental performance

Future of New Etch Technologies

DRAM: Capacitor SiO_2 Etch

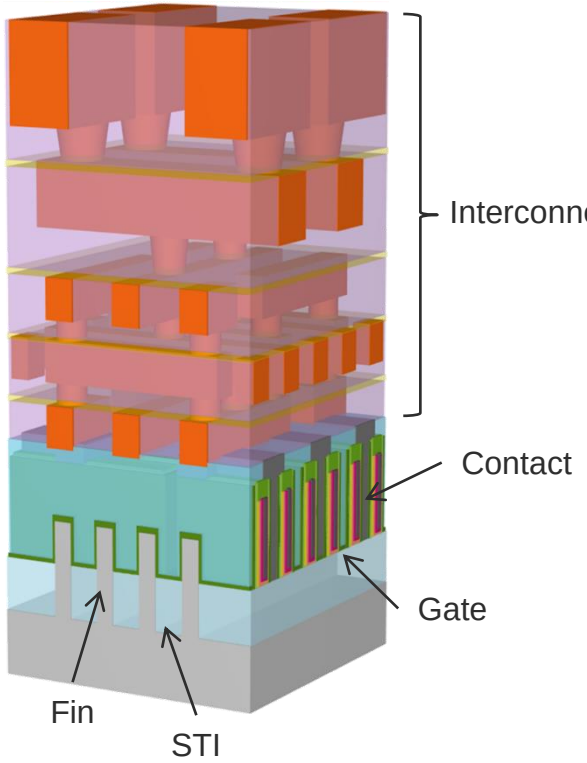


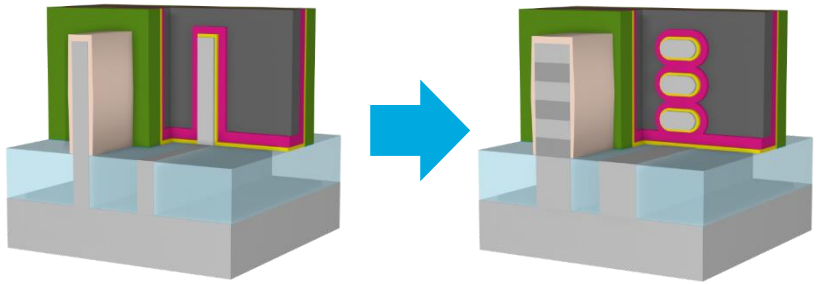
Logic: Gate Silicon Etch



New technologies created through the development of ideal etching process development, will be applied to a variety of critical processes

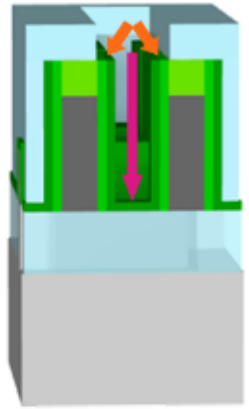
Business Opportunities in Logic



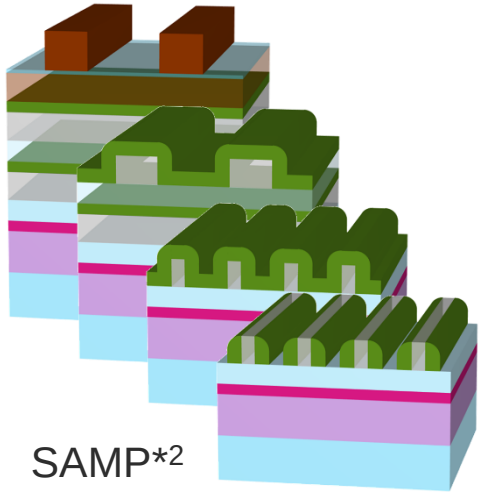


FinFET

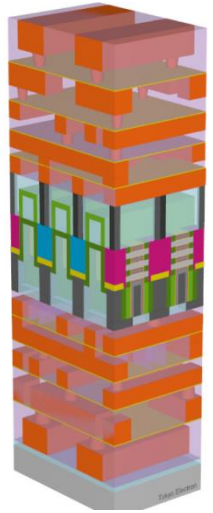
GAA*1 Nanosheet



Self-aligned Contact



SAMP*2



Backside PDN*3

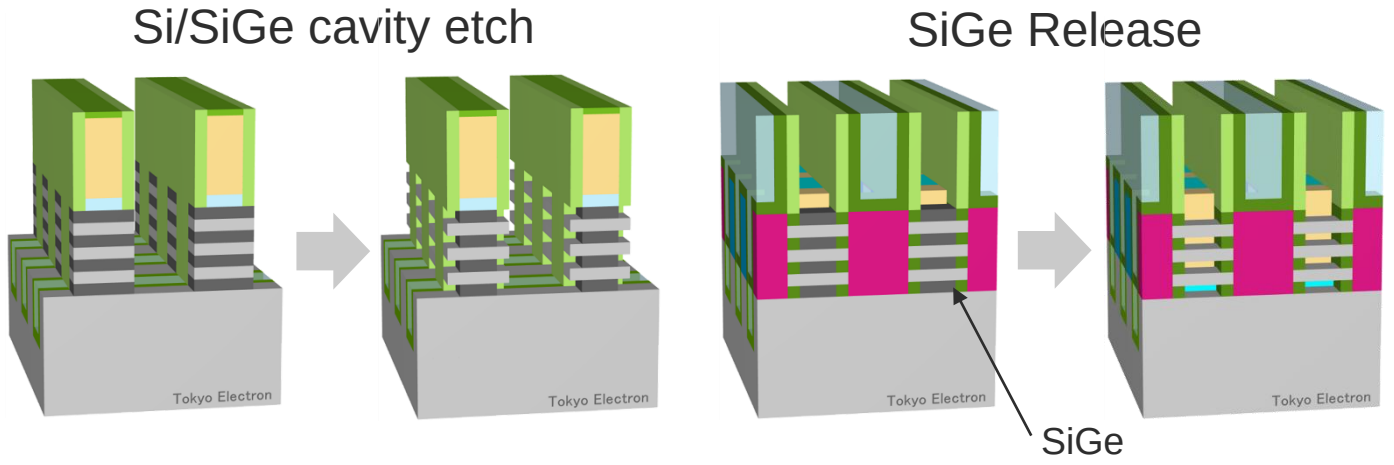
*1 GAA: Gate all around
*2 SAMP: Self-aligned multiple patterning
*3 PDN: Power delivery network

Respond to changes in device manufacturing and EUV lithography for further scaling

Initiative for GAA Nano Sheet Structures

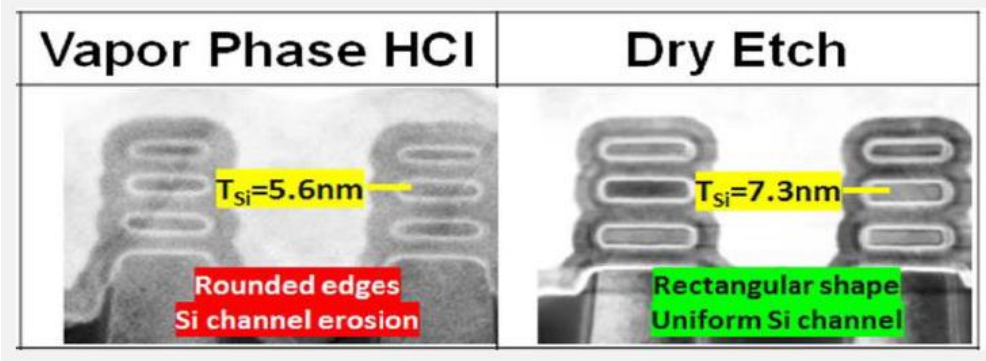
Nano Sheet process challenges:

- Uniformity in rectangle shape
- Mitigation of roughness/residue on patterned surface



TEL's initiative: Gas chemical etch

- High etch selectivity
- High uniformity
- Residue removal/decreased roughness



Source: N. Loubet, et al., IBM, TEL Technology Center, America (IEDM2019)

Leveraging the advantages of gas chemical etch to contribute to leading-edge processes

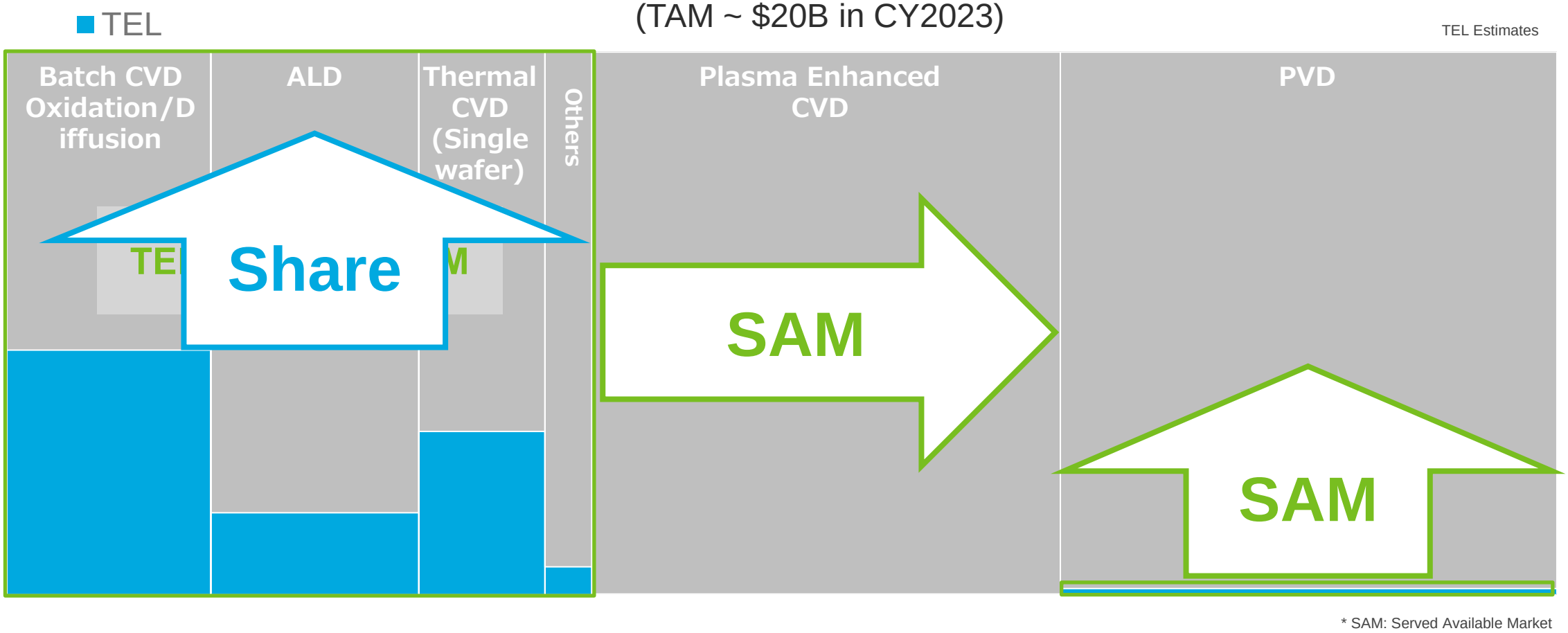
7-2-2. Deposition System

Business Strategy in the Thin Film Deposition Market

Expanding Market Share and SAM*

TEL's Market Share and SAM in Thin Film Deposition

(TAM ~ $20B in CY2023)

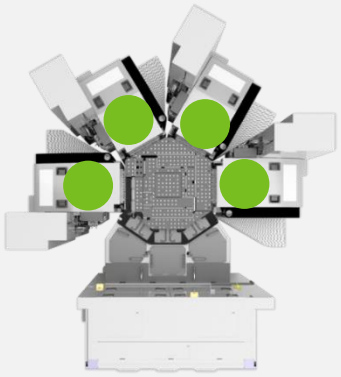


* SAM: Served Available Market

Strategies in the Film Formation Business 1:

Expand SAM with Single Wafer CVD

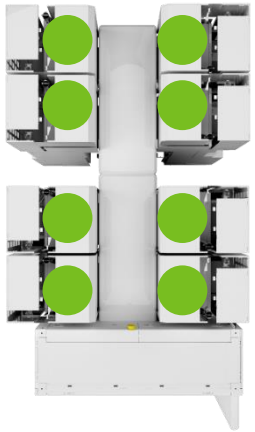
Triase+™



Single Reactor

Existing Platform

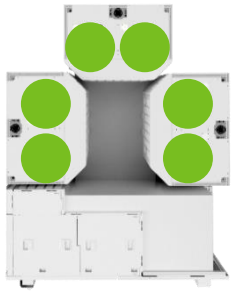
Episode™ 1



Single Reactor

Equipped with up to eight process modules

Episode™ 2 DMR*



***Duo Matched Reactor**

Achieved high productivity
by processing 2 wfs/PM

Released in July 2024

Episode™ 2 QMR

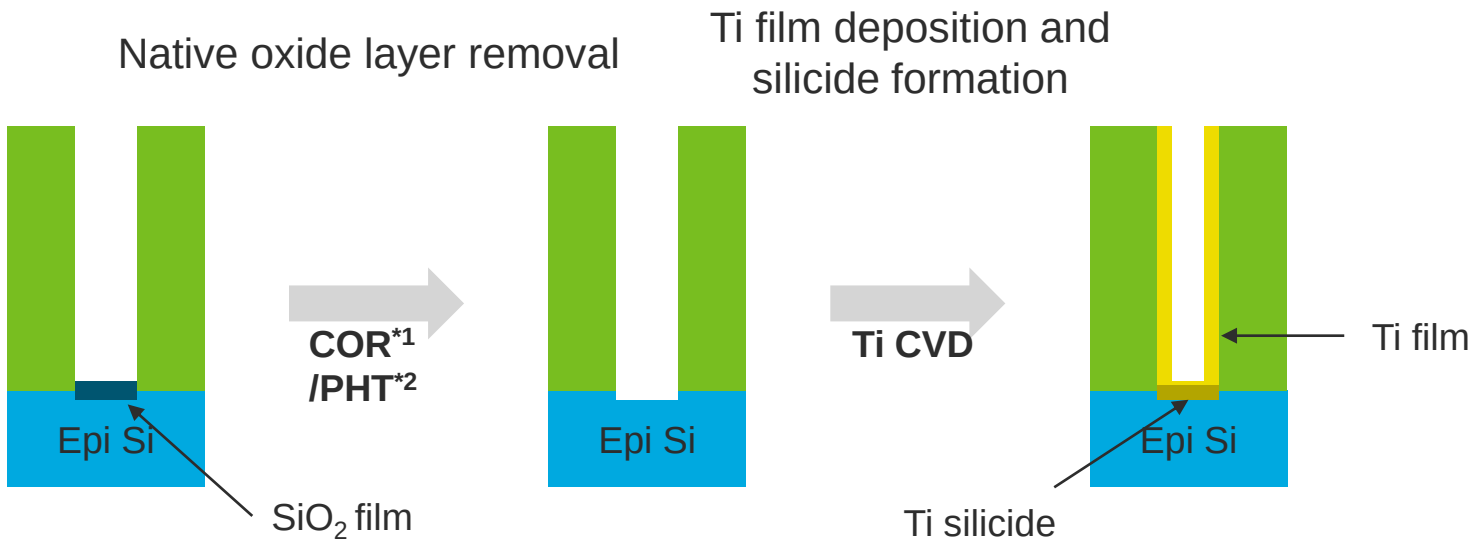
Quad Matched Reactor

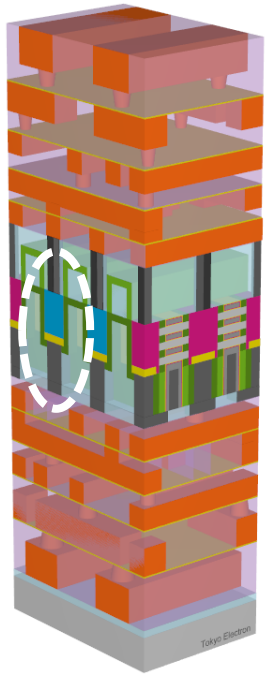
Equipped with a newly developed
high-density plasma source

Scheduled for release in 2026

Episode™ 1: Contact Formation Process

- Example of process flow



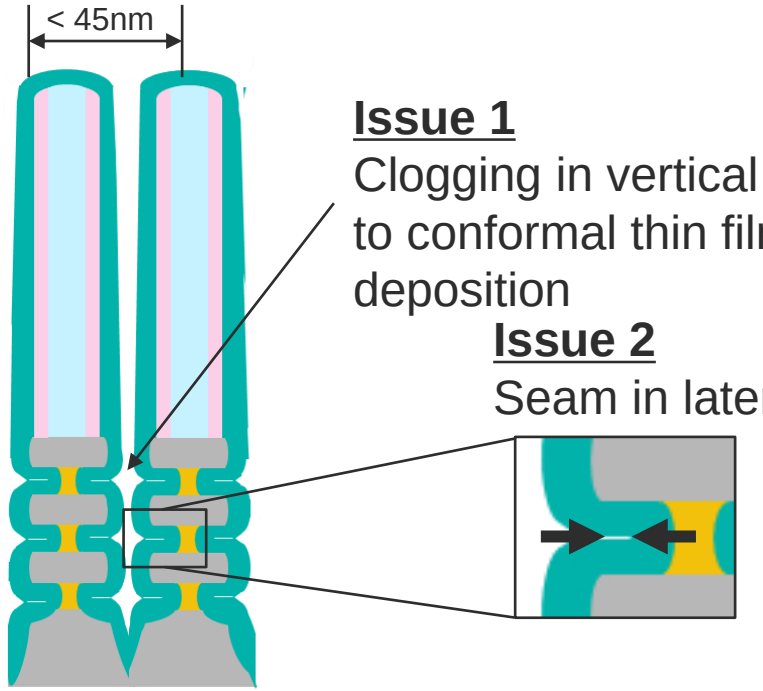


*1 COR: Chemical Oxide Removal
*2 PHT: Post Heat Treatment

Multiple types of process modules are equipped on a high-vacuum transfer module, and low-resistance contacts are achieved by sequentially processing native oxide layer removal and metal film formation

Episode™ 1: Inner Spacer Formation - Lateral Gapfill

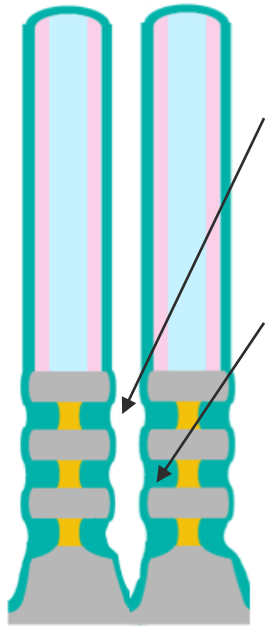
- Issues :
  Leak due to dielectric breakdown due to etching



Issue 1
Clogging in vertical gap due to conformal thin film deposition

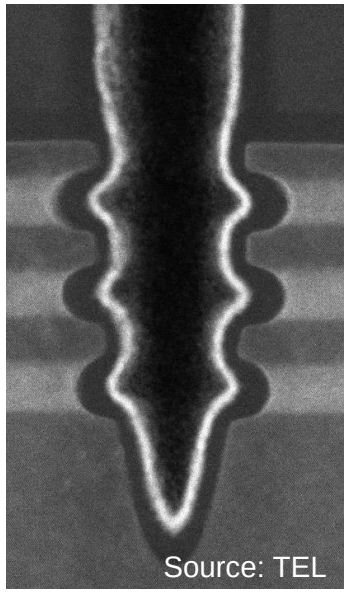
Issue 2
Seam in lateral gap

- Solutions :
  Improve lateral gapfill performance



Solution 1
Thinner film deposition on the side walls

Solution 2
Seamless gapfill in lateral gap



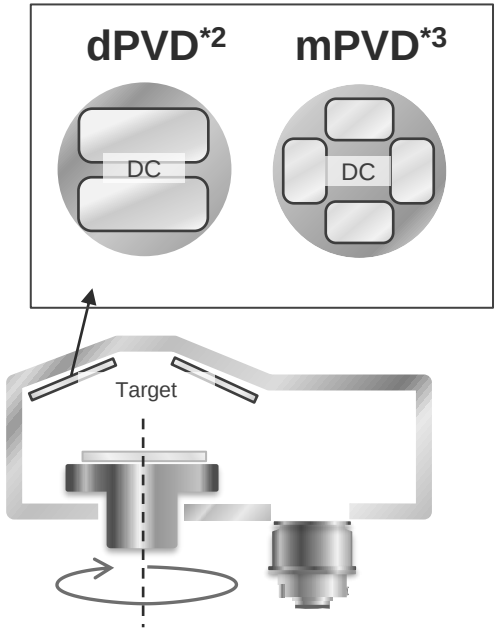
Realized seamless lateral gapfill using a unique thin film deposition technique and laterally uniform film modification using a newly developed high-density plasma

Strategies in the Film Formation Business 2:

SAM Expansion with PVD

LEXIA™ -EX **Released in December 2024**

- Oblique angle sputter with wafer rotation system
  - Excellent thickness uniformity (1σ 0.5%)
- Unique multi-cathode*1 configuration
  - High deposition rate
  - Capability of tuning film composition ratio with multiple materials
- High throughput (~100WPH)
- Significant footprint reduction vs conventional model



*1 Cathode: An electrode for material deposition
*2 dPVD: Dual cathode PVD
*3 mPVD: Multiple cathode PVD

Strategies in the Film Formation:

Growth in Batch Thermal Process/Deposition

- Major applications
  - Silicon process in general (dummy gate, channel Si, etc.)
  - Batch ALD high-k (capacitor dielectric)
  - Plasma/Thermal ALD-SiN/SiO_2
  - Batch molybdenum (word line)

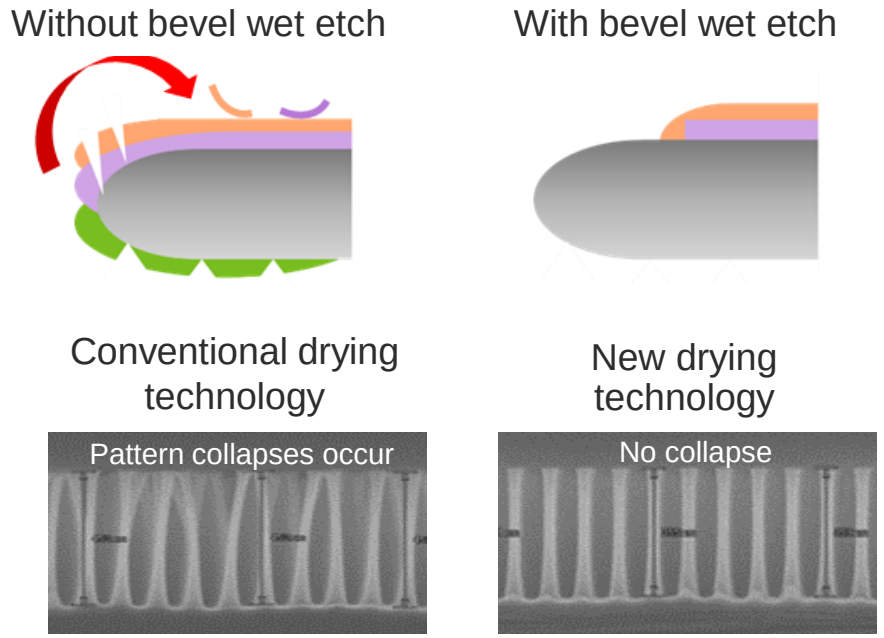
- Development plans
  - Increase load port size (8 lots, 200 wafers/batch)
  - Improve exhaust conductance to mitigate pattern loading effect
  - Enhance energy efficiency (elevate heater performance)
  - Enhance labor reduction (one-touch start-up, self-maintenance, DX)

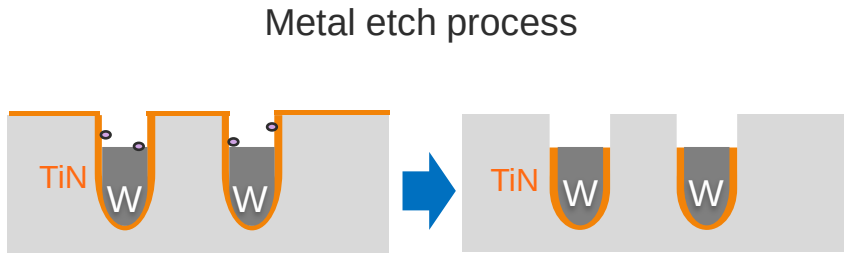
TELINDY™ PE-II

7-2-3. Cleaning System

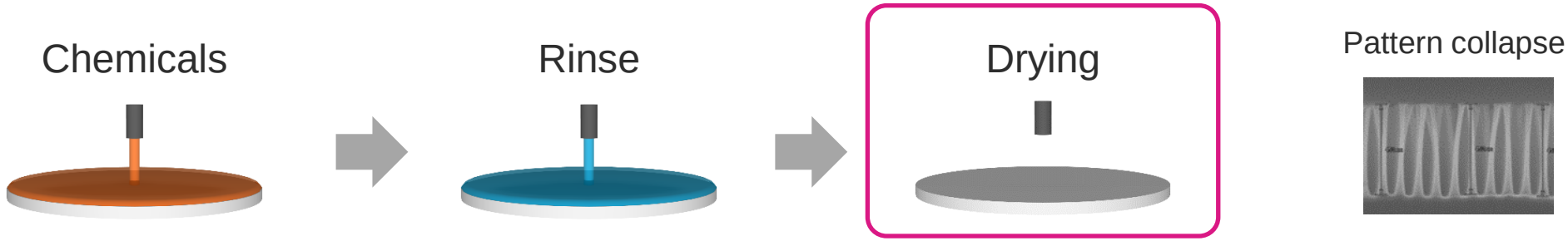
Single Wafer Cleaning Strategy

- Single wafer cleaning
  - Bevel wet etch
    - Expect annual market growth rate of around 10%
    - Contribute to improving customers' yields.
      Maintain a high market share by differentiating through performance in precisely removing film from the outer part of the wafer
  - Prevent pattern collapse
    Expand market share by TEL original technology to reduce collapse of high aspect ratio pattern
  - Metal etch
    Launched new dedicated SPM chambers for controlling selectivity for metal in order to solve reduced yield issues caused by dry etch damage and residue

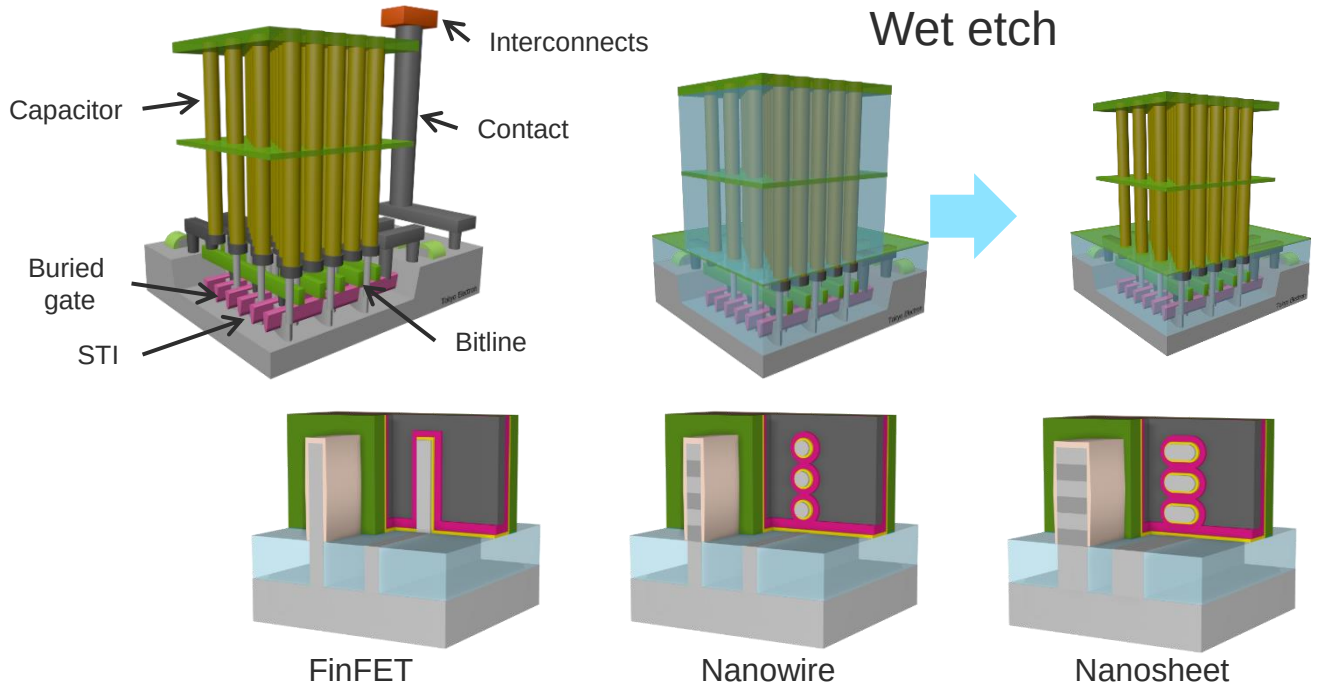




Technology Challenges in Cleaning for State-of-the-Art Devices



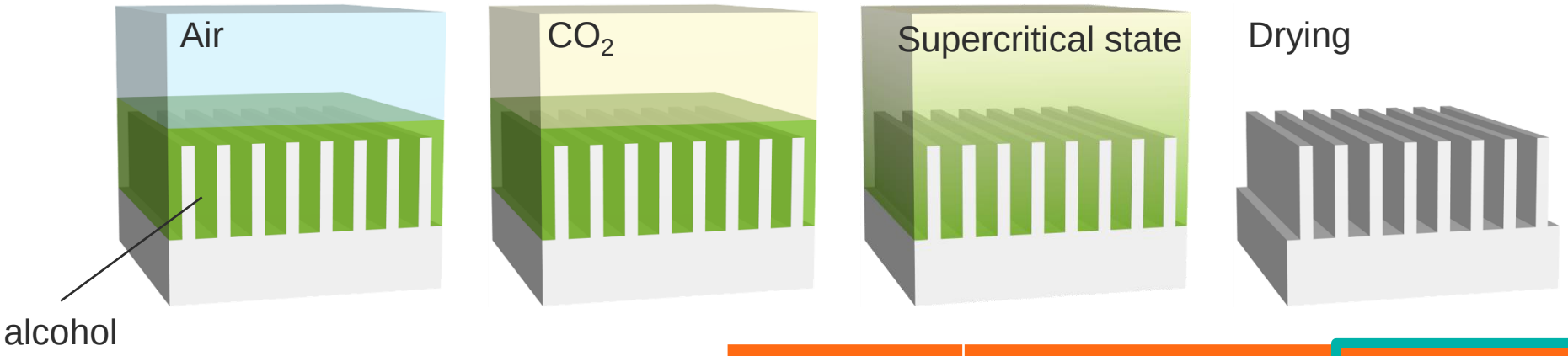
- DRAM
  - Post-STI etch cleaning
  - Mold wet etch after capacitor electrode formation

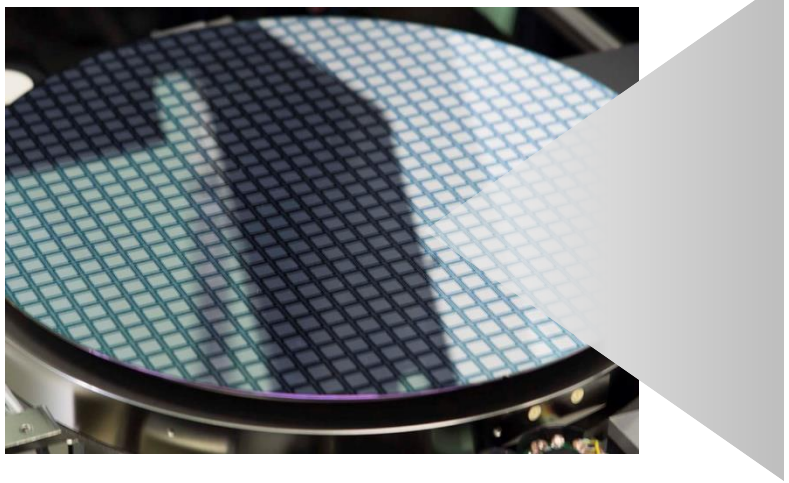


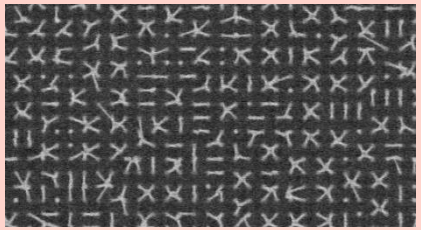
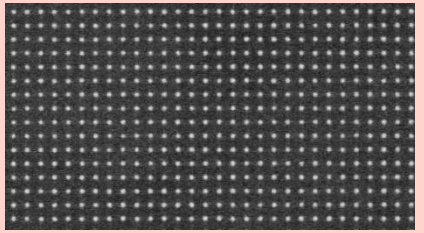
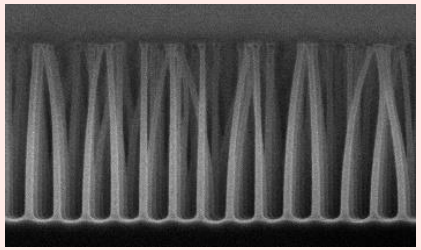
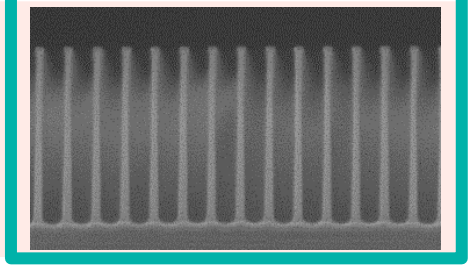
- Logic
  - Post-fin etch cleaning
  - Post-nanowire/nanosheet formation cleaning

Drying technology more difficult due to further scaling and higher aspect ratios in device manufacturing

Supercritical Drying Technology





	Traditional drying	TEL's supercritical drying
Top View		
Side View		

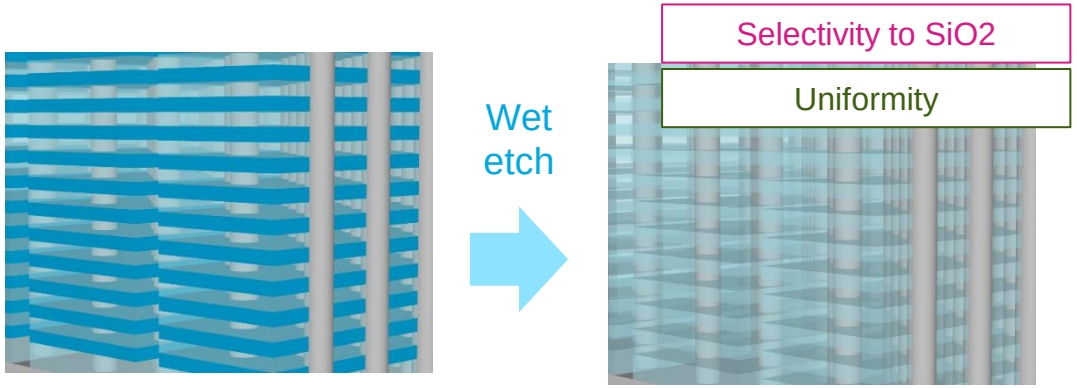
Supercritical drying technology prevents pattern collapse

Batch and Scrubber Cleaning Strategy

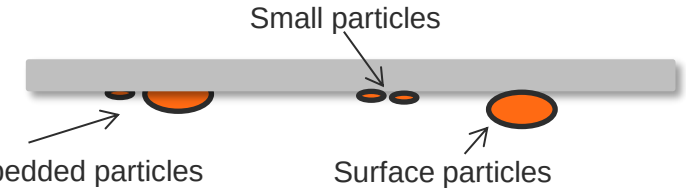
- Batch cleaning
  - SiN etch and W etch processes for 3D NAND
    Focus on processes that require long durations and advanced process technology. Differentiate by realizing high uniformity, high selectivity and high productivity in wet etch

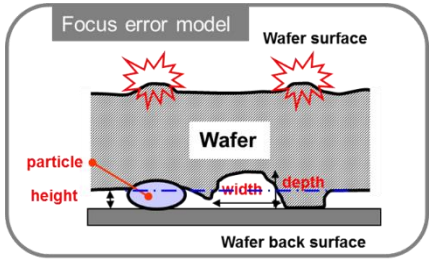
- Scrubber cleaning
  - Pre-lithography process
    Provide high-value solutions such as reducing particles brought in by wafers, contributing to the improvement of exposure tool availability which have grown increasingly important due to the introduction of EUV

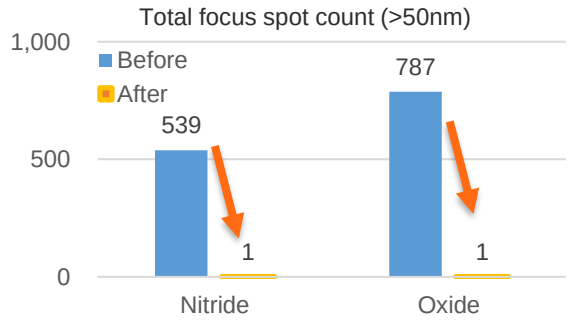
SiN etch process



Wafer back and defocus diagram

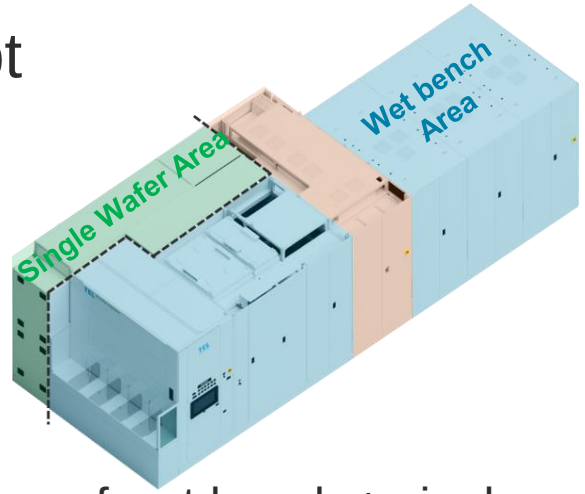






ZEXSTA™

- Concept



A combination of wet bench + single-wafer process

Method	Features
Wet Bench	High-temp/ long-duration process, wet etch
Single Wafer	Advanced drying technology, particle control

- Target Application
  - Advanced wet etch + advanced dry tech

    - Highly selective wet etch process will be required for also 3D DRAM in addition to 3D NAND
  - High throughput + surface cleanliness

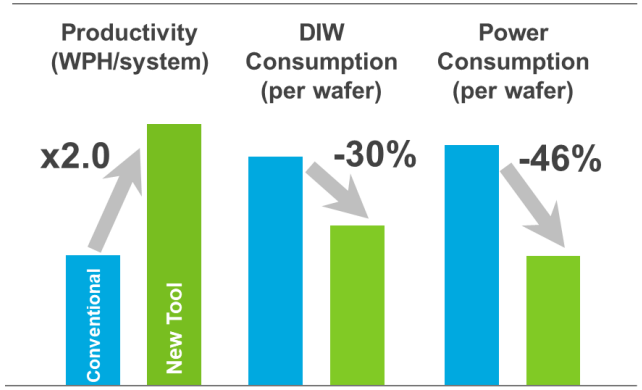
    - High surface cleanliness is required for logic and DRAM

TEL will contribute to customer technology development by continuing to create new value, overcoming the constraints of traditional equipment classifications

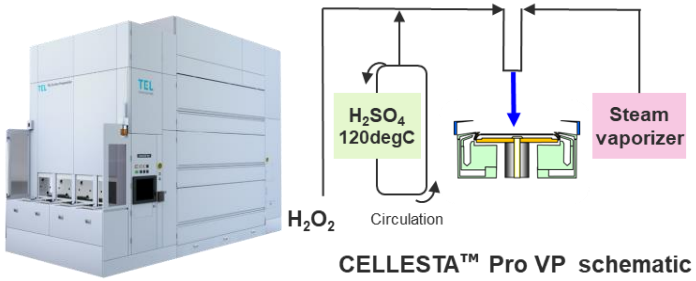
Development of Cleaning Systems

High Productivity Wet Bench (EXPEDIUS™-R)

Industry's first large-batch process (increased wafer counts)



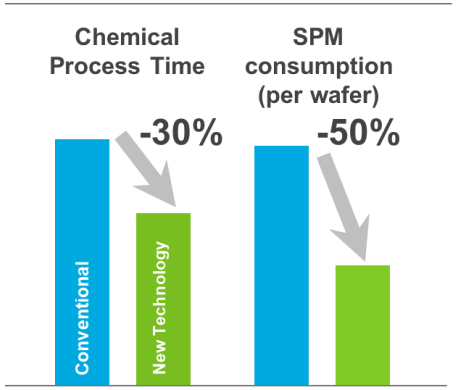
SPM*1 Vapor Technology (CELLESTA™ Pro VP)



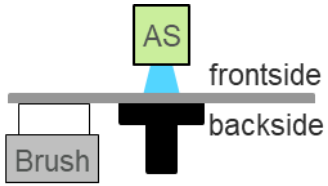
CELLESTA™ Pro VP schematic

Enabled higher temperature process due to a more effective rection by adding water vapor to chemicals

*1 SPM: Sulfuric Acid and Hydrogen Peroxide Mixture

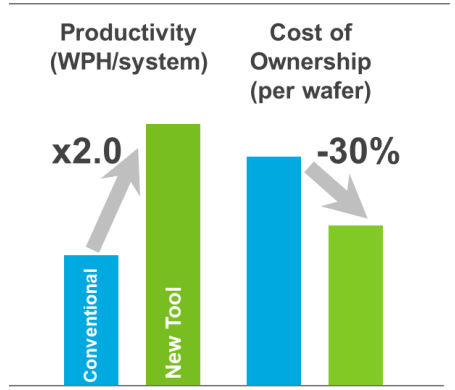


Simultaneous Scrubber (CELLESTA™ MS2)



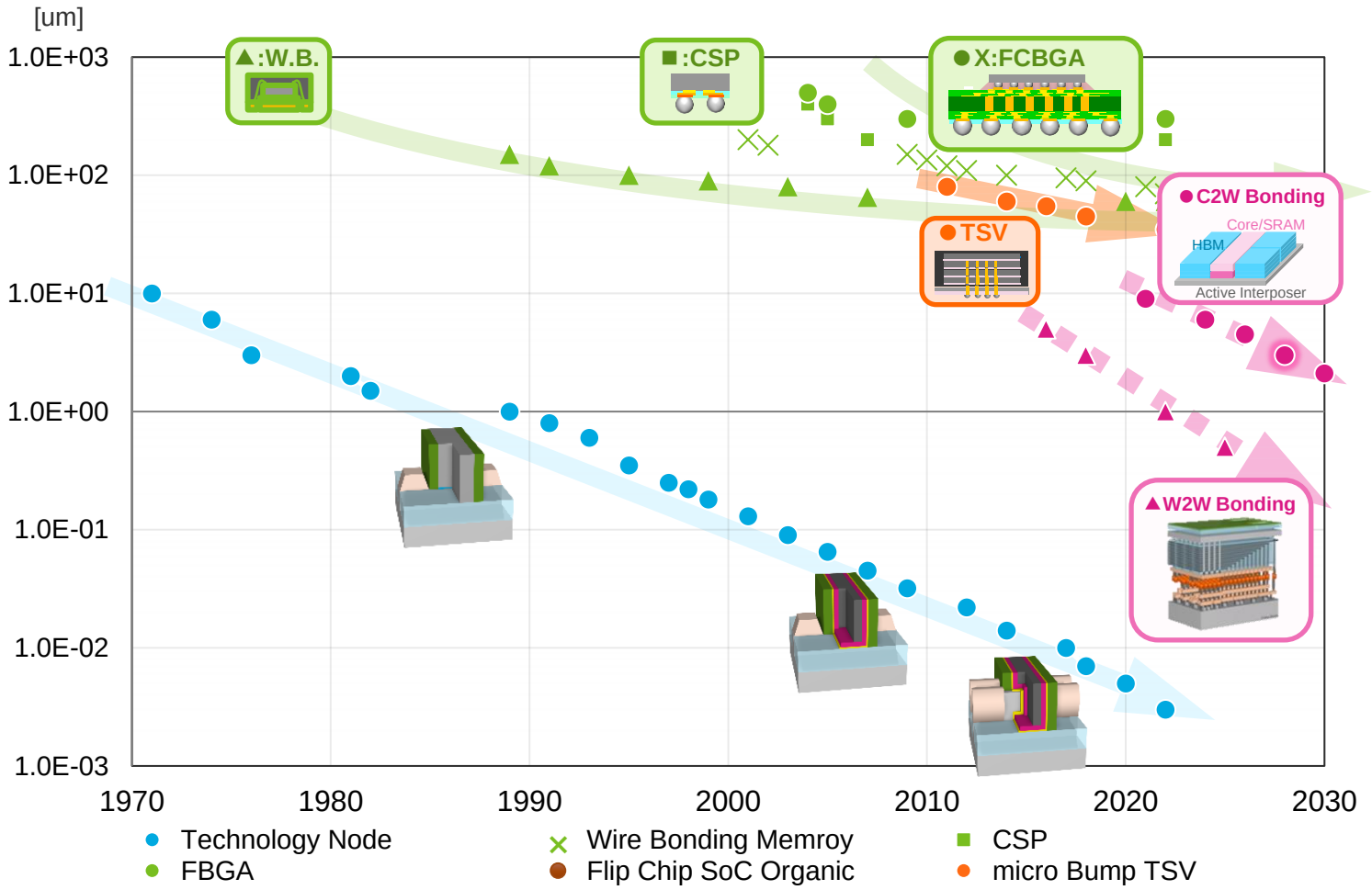
A tool enabling AS*2 process on wafer frontside and physical brushing process on wafer backside simultaneously in a single chamber

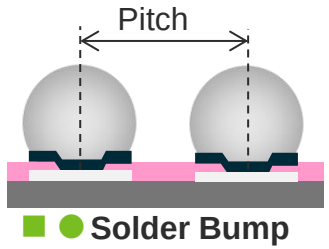
*2 AS: Atomized Spray

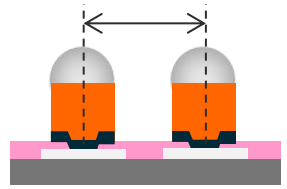


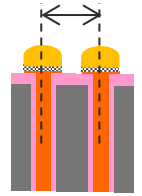
7-3. Backend Business Strategy

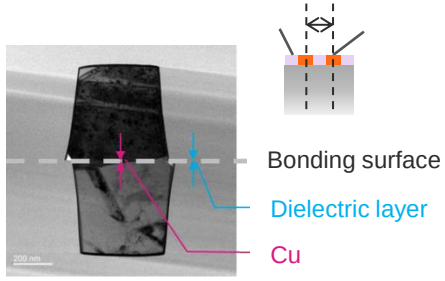
Semiconductor Technology Node and Bump Pitch









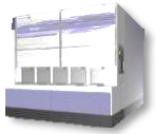


Introduction of wafer bonding technology accelerates further reduction of pitch

History of Product Launches in Assembly and Test* Systems

New Category Product　　Next Generation/Improvement Product

Synapse™ S
Fusion bonder



Synapse™ V
Temporary bonder

Synapse™ Si
Cu hybrid / Fusion wafer bonder

Prexa™
Wafer Prober

Ulucus™ L
Laser Edge Trimmer

Synapse™ Si (high accuracy)
Cu hybrid / Fusion wafer bonder

Ulucus™ LX
Extreme Laser Lift Off

Die Test Prober
Upcoming system for release

Year | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026

Synapse™ Z plus
De-bonder

Synapse™ ZF
Post bond re-worker

Ulucus™ G
Wafer Thinning

3DI
Upcoming system for release

Accelerating product development to prepare for the era of 3D integration

*Test : Prober for Advanced Packaging Test

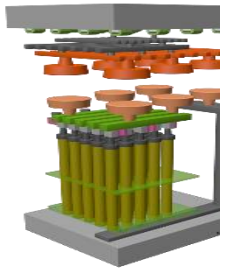
3DI / Test Business Expands Opportunities for HPC/AI Device

Frontend Process

Device Manufacturing

BSPDN*1

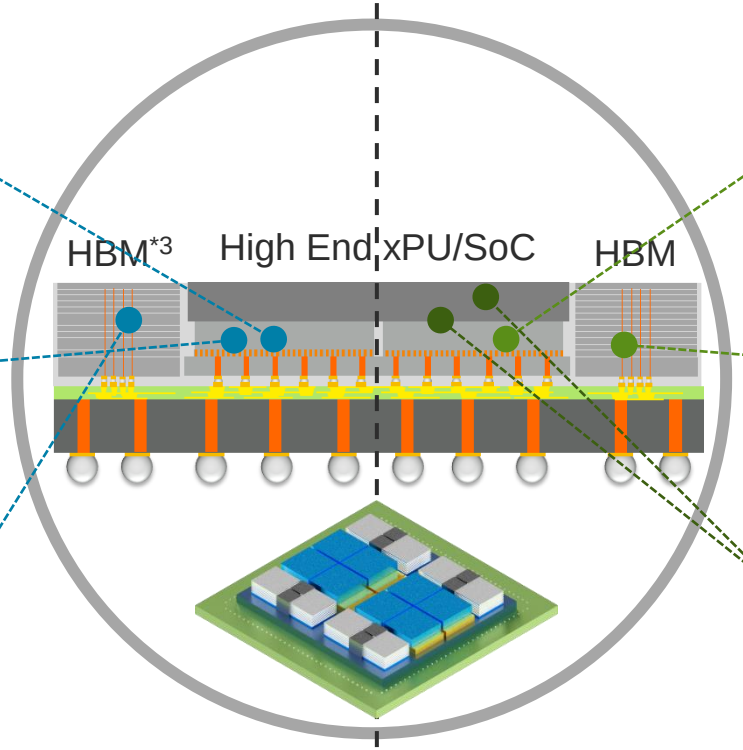
CFET*2



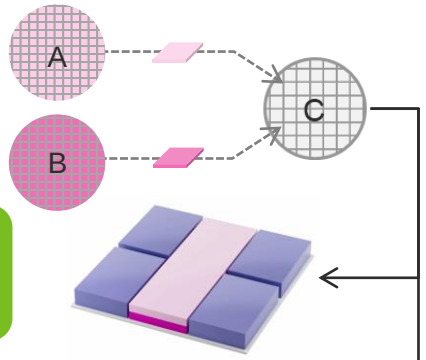
DRAM

Advanced Packaging

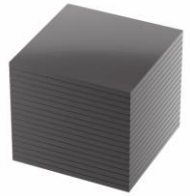
Assembly after Dicing/Singulation



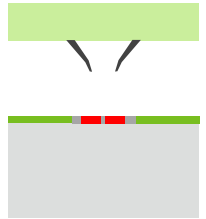
3DIC



Stack Memory



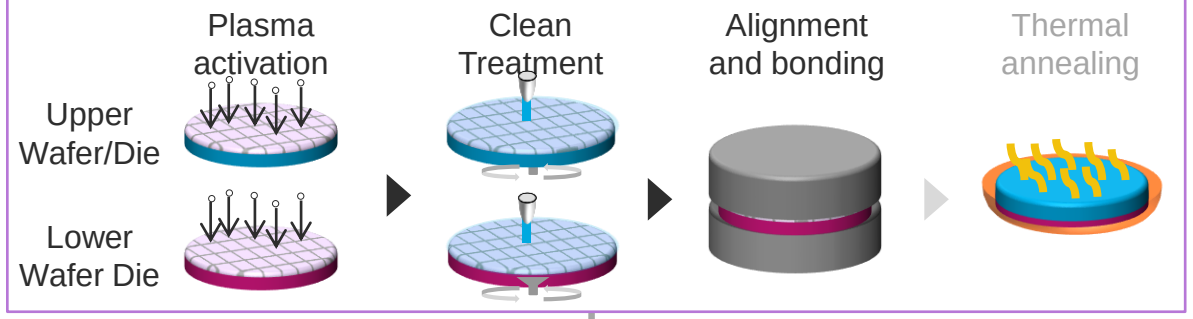
Die Test for KGD*4

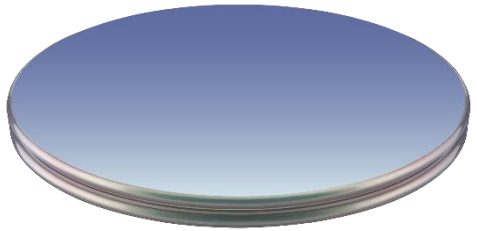


*1 BSPDN: Back Side Power Delivery Network
*2 CFET: Complementary Field Effect Transistor
*3 HBM: High Bandwidth Memory
*4 KGD: Known Good Die

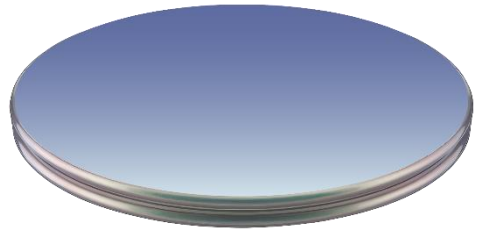
TEL's Opportunities for Bonding Technology

Bonding Technology

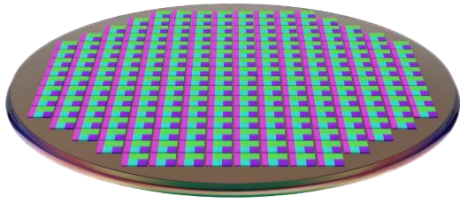




Wafer-to-Wafer Bonding



Wafer-to-Wafer Bonding



Die-to-Wafer Bonding

Benefits for Pitch scaling & Higher speed / Lower power consumption

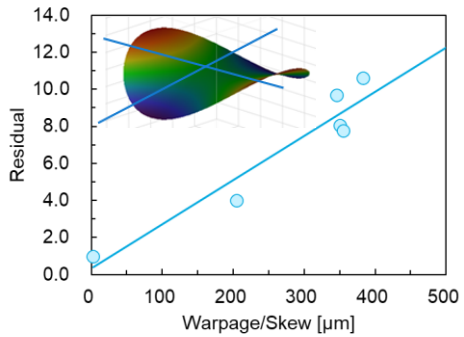
Frontend Process

Advanced Packaging

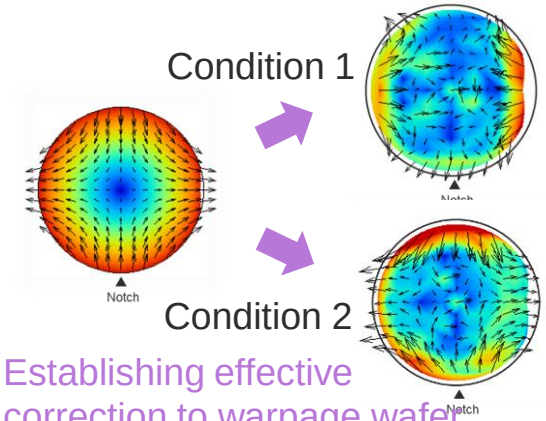
Wafer Bonder Technology Roadmap and Challenges

CY	2024	2025	2026	2027	2028	2029	2030	Beyond
Logic Node	2nm	2nm	2nm+	14A	14A	10A	7A	5A
Logic	Distortion ≤ 4nm （BSPDN）			Distortion ≤ 3nm （BSPDN）		Distortion ≤ 2nm （CFET）		
NAND	2-wafer-bonding				3-wafer-bonding		≥ 4-wafer-bonging	
NAND	Wafer warpage < 500μm				Wafer warpage > 500μm			
DRAM	2D DRAM			2D/3D DRAM				
DRAM	Distortion ≤ 5nm / DxDy ≤ 70nm			Distortion ≤ 3nm / DxDy < 50nm				

Wafer Warpage Challenges and Actions

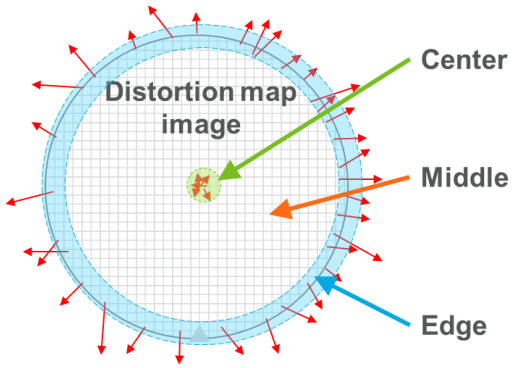


Relation between wafer warpage and residual (distortion)

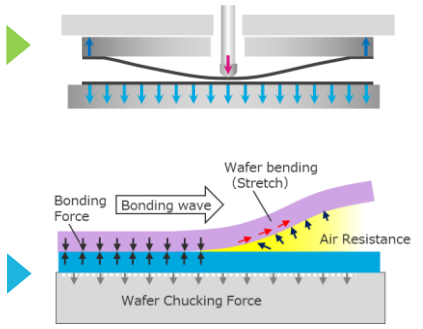


Establishing effective correction to warpage wafer

Distortion Challenges and Actions



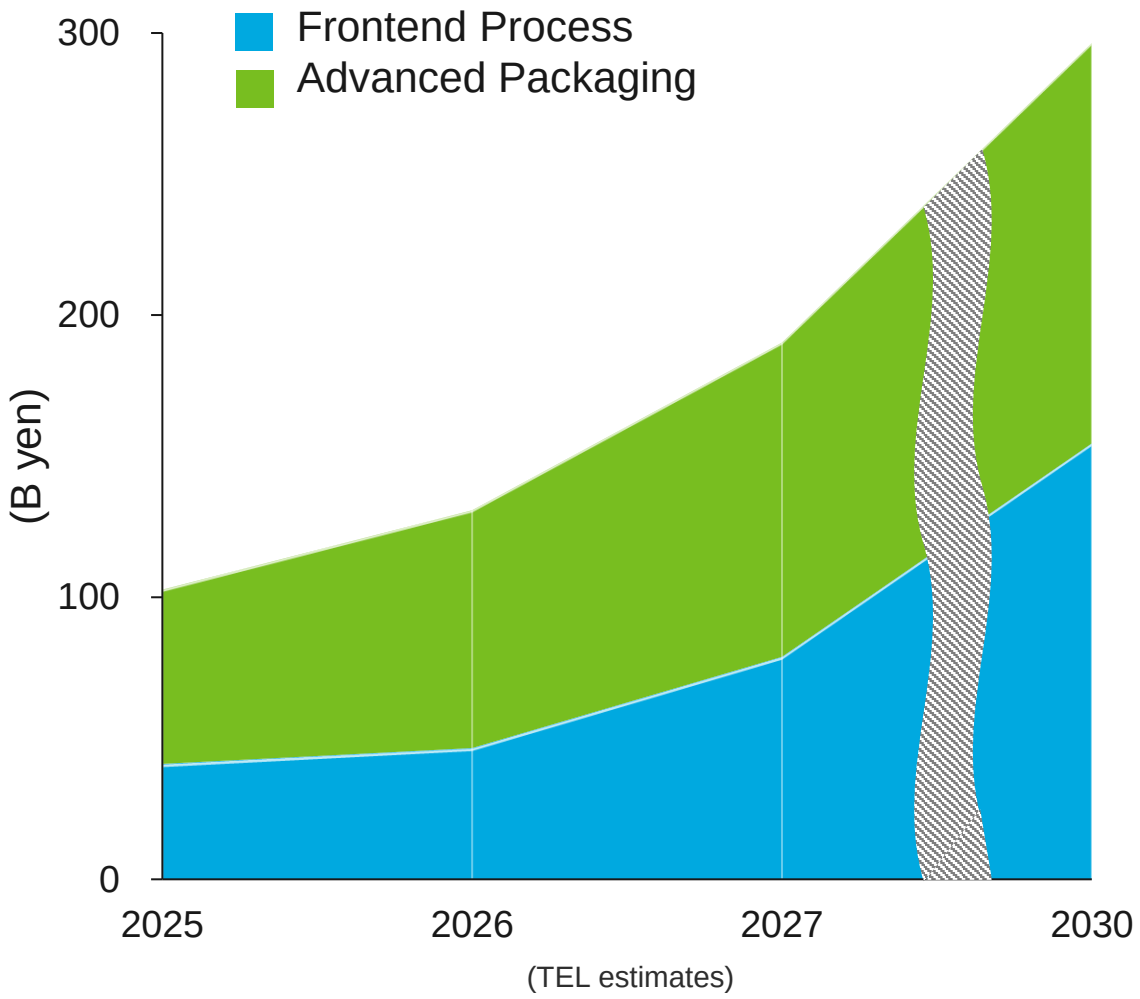
Distortion vector



Optimizing hardware and process

TEL is developing various technologies in advance to prepare for next-generation devices

Bonding Process Equipment TAM*

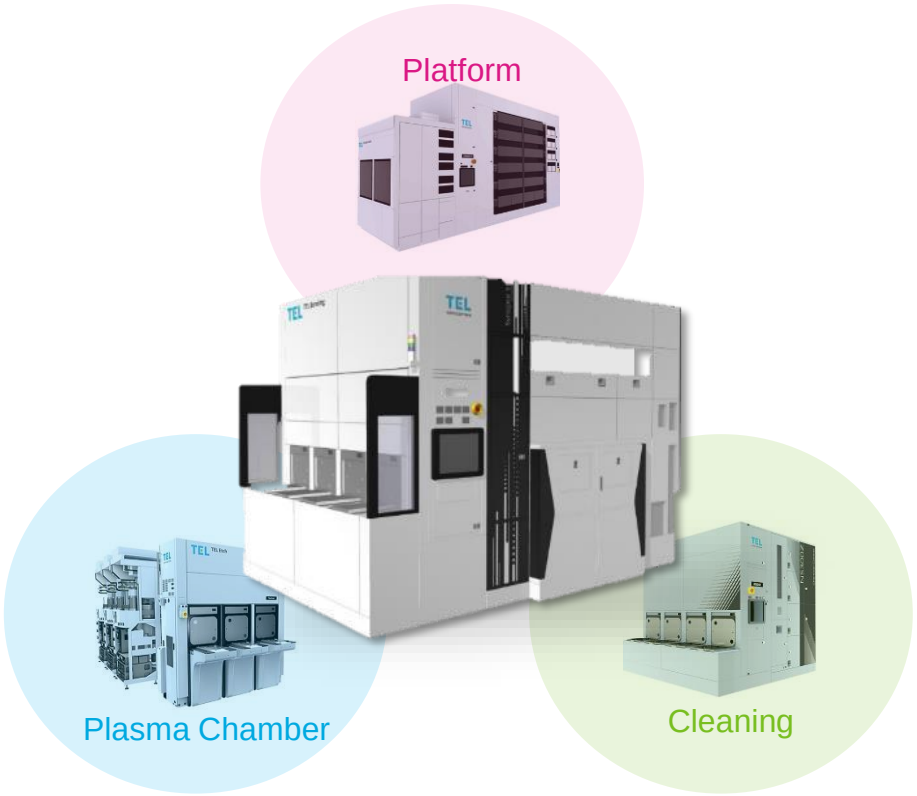


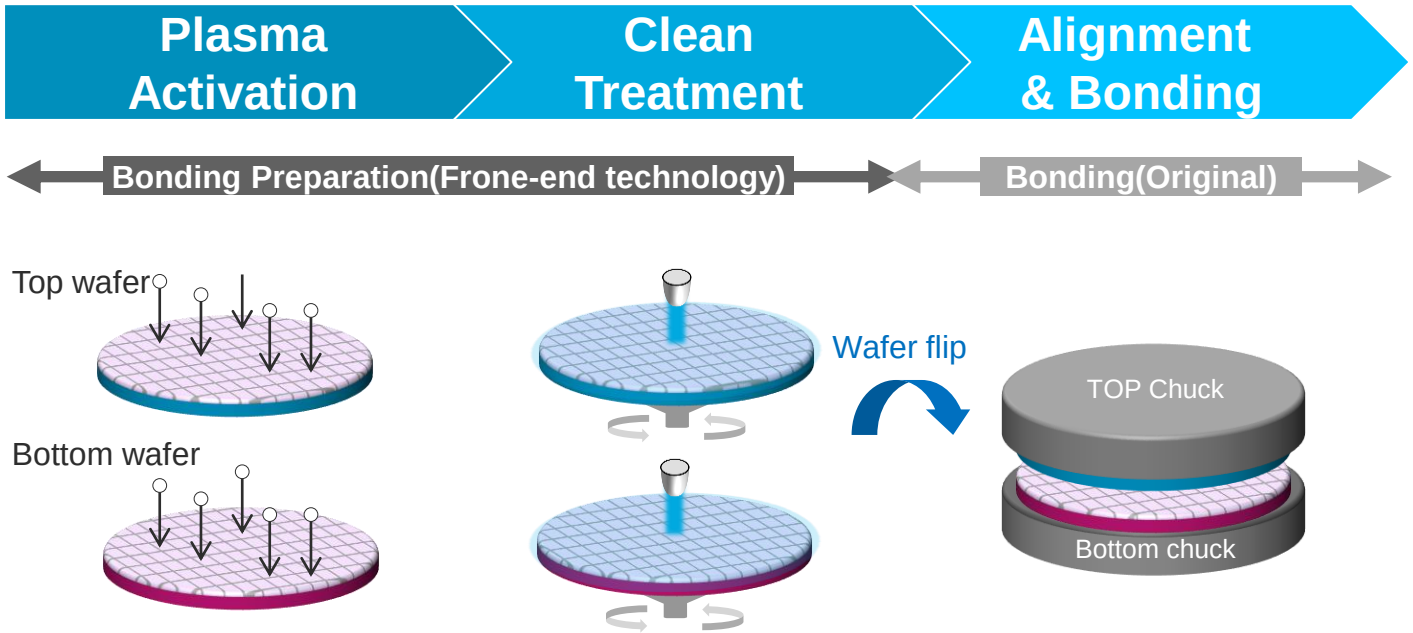
Anticipating a TAM CAGR of 24% from CY2025 to CY2030

- Projected to achieve 300 billion yen by CY2030
- Encompassing both frontend processes and advanced packaging equipment
- Addressing bonding/debonding, slicing, and thinning process equipment utilizing various technologies

* TAM : Total Available Market

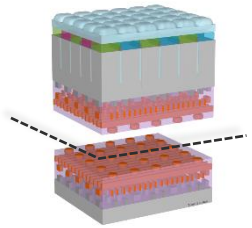
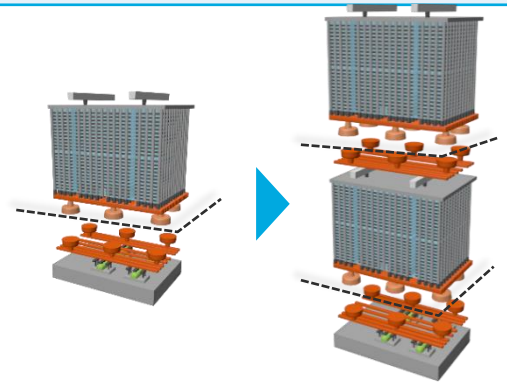
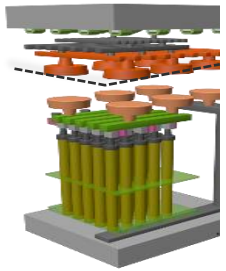
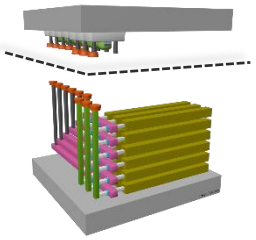
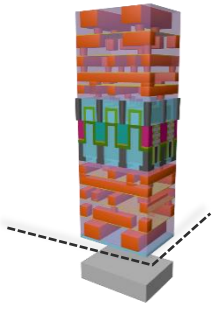
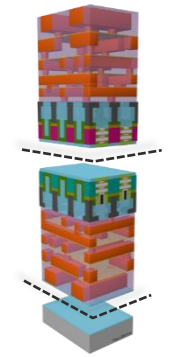
Wafer-to-Wafer Permanent Bonder Synapse™ Si





- TEL's existing broad technology and business contributing effective product development/CIPs
- Making good progress with major memory, logic customers towards high volume manufacturing
- Leading W2W Fusion/Cu hybrid bonding technology for next generation device manufacturing

Broad Applications and Expansion of Bonding Technology

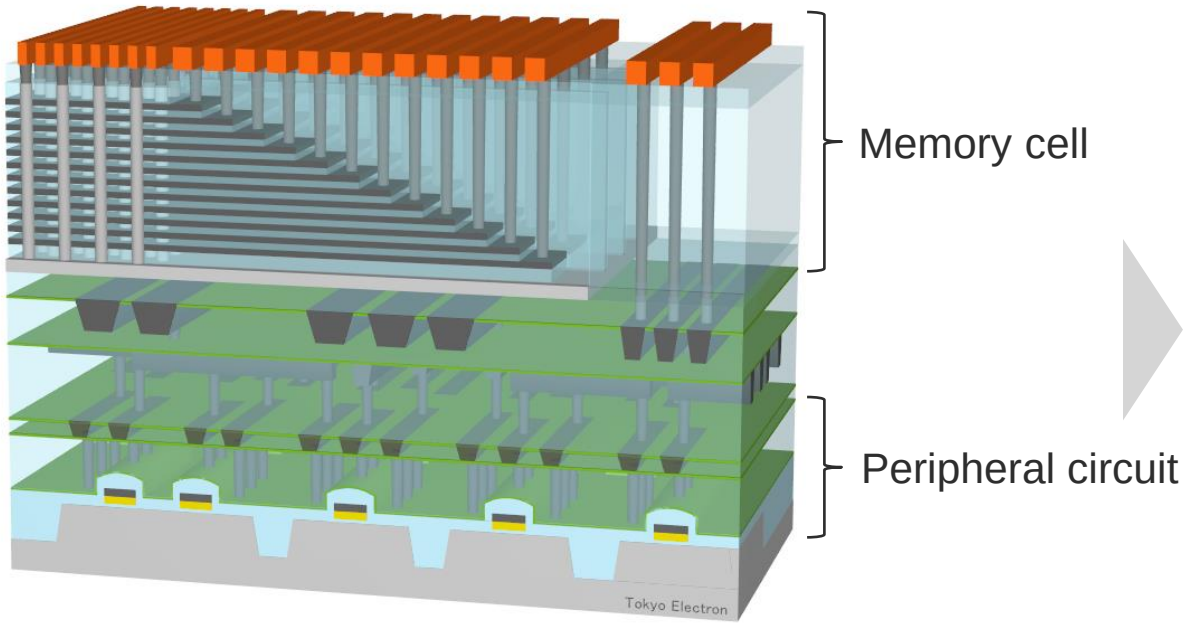
Application	Frontend Process					
	CIS[*1]	NAND		DRAM		Logic
Stacking Device	BSI[*2] Pixel + (Peripheral) + Logic	3D NAND Cell + Peripheral	: + Cell + Cell + Peripheral	VCT[*5] DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	3D DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	BSPDN Logic + Si Substrate	BSPDN & CFET Logic + Logic + Si Substrate
Bonding	Wafer to Wafer (CHB[*3]/Fusion)	Wafer to Wafer (CHB)		Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)	
Structure							
Status	HVM[*4]	R&D~HVM	R&D	R&D	R&D	R&D~HVM	R&D

The design of future devices is transitioning from single bonding to multi-bonding structures

*1 CIS: CMOS Image Sensor
*2 BSI: Backside Illumination
*3 CHB: Cu Hybrid Bonding
*4 HVM: High Volume Manufacturing
*5 VCT: Vertical Channel Transistor

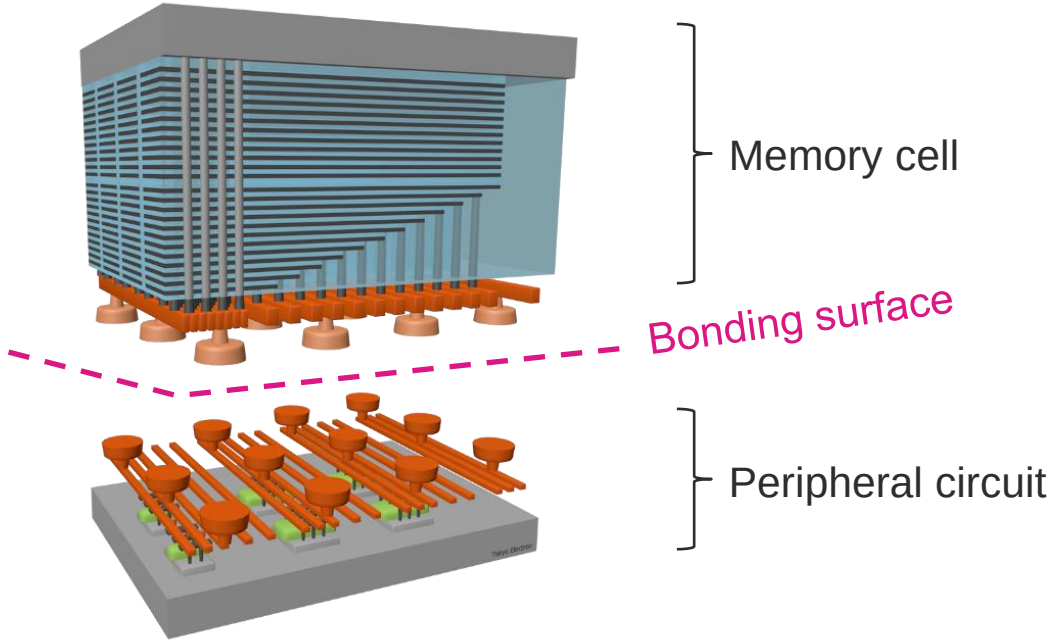
Wafer Bonding Application for 3D NAND

Current structure



- ✓ Peripheral circuit performance deteriorates due to exposure to high temperature during memory cell manufacturing
- ✓ Long interconnects wiring

New structure

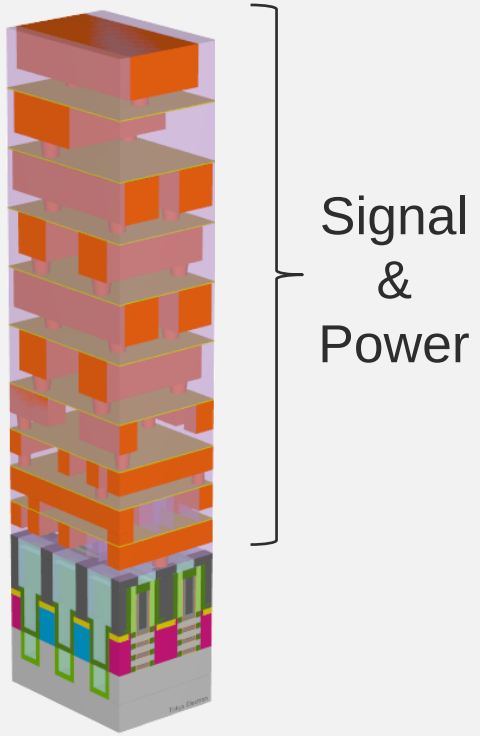


- ✓ Peripheral circuit is manufactured on the separate wafer and bond to the memory cell wafer
  - higher peripheral circuit performance
  - shorter TAT* process
- ✓ Shorter interconnects wiring

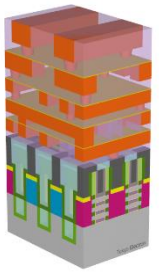
* TAT: Turnaround time

Wafer Bonding Application for Logic Backside PDN

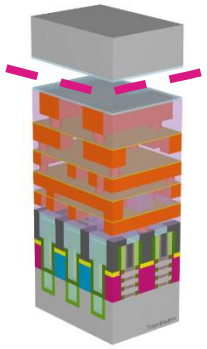
Conventional Structure



1. Signal BEOL (Front side)

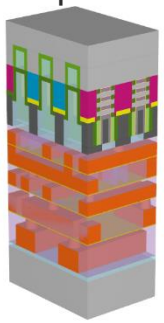


2. Si Wafer Bonding

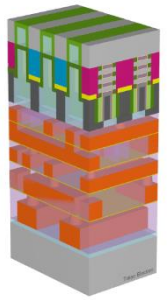


flip

3. Flip Wafer



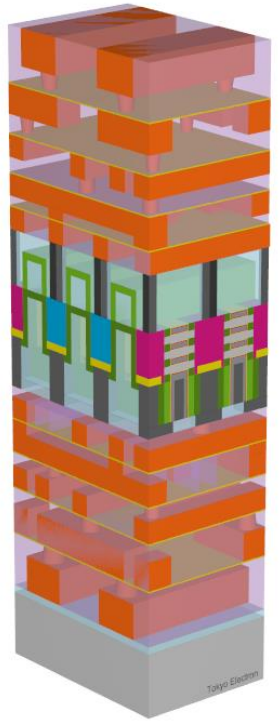
4. Backside Thinning



5. Power BEOL (Backside)

Backside PDN*

*Power Delivery Network



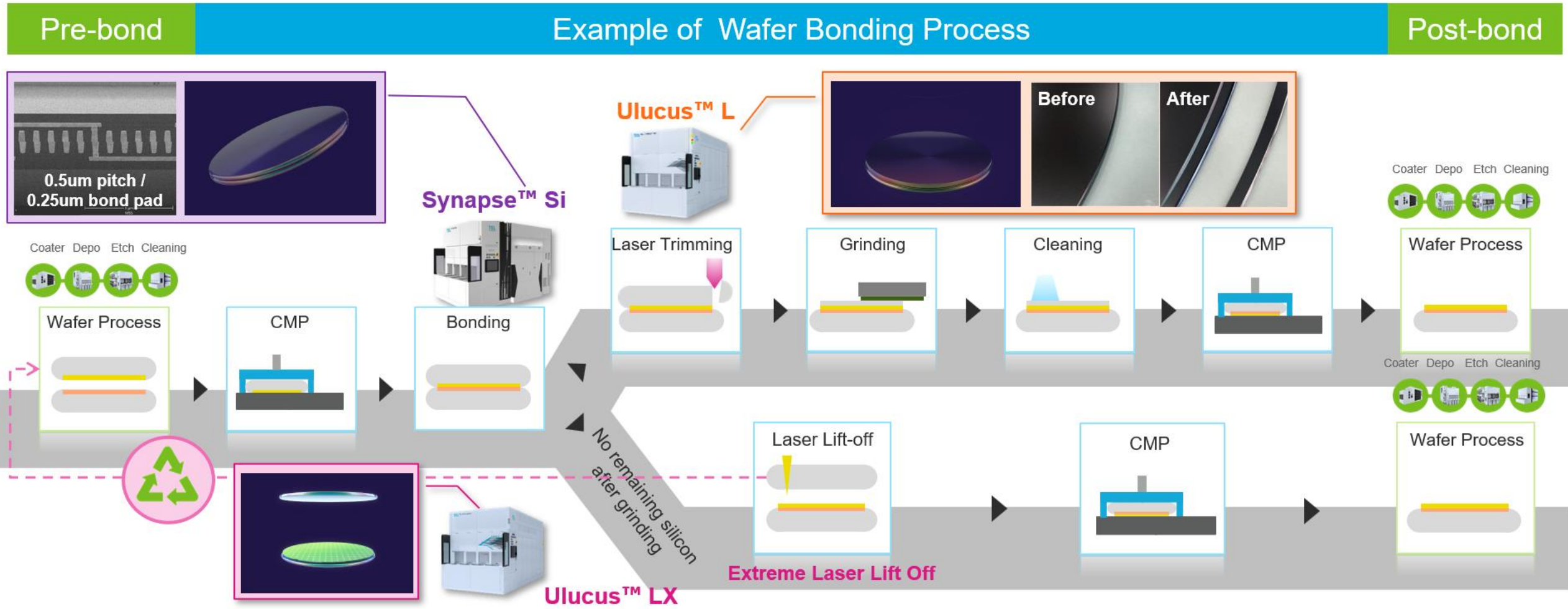
Can pursue further scaling without the bottleneck due to power wiring

Broad Applications and Expansion of Bonding Technology

Application	Advanced Package		
	Stack Memory / HBM	3DIC	
Stacking Device	DRAM Wafer ⋮ DRAM Wafer + DRAM Wafer + Logic Wafer OR DRAM (Die) ⋮ DRAM (Die) + DRAM (Die) + Logic Wafer	SoC Disaggregation Device A Wafer + Device AorB Wafer OR A, B → Die → C → Wafer	Heat Spreader Heat Spreader + Device
Bonding	Wafer to Wafer / Die to Wafer (CHB/Fusion)	Wafer to Wafer / Die to Wafer (CHB)	Wafer to Wafer (Fusion)
Structure	**Micro Bump** → ***Cu hybrid*** (More stacks) Change • Thinner die / more stacks • High density connection • Better thermal conductance Cu	**Monolithic SoC** → ***3D Stack IC*** SRAM, CPU/GPU, I/O&Peripheral Change • Small formfactor (3D stack vs. 2D) • Higher speed (shorter wiring, no bump) • Lower power (shorter wiring, no bump) • Lower cost (higher yields, easy to mix processes) • Shorter time to market (matured IP block reuse)	Heat Spreader • Better thermal conductance
Status	R&D	R&D ~ HVM	HVM

The opportunity for CHB/fusion bonding is growing to encompass advanced packaging

Frontend Wafer Bonding Process and TEL Products



Integrating various TEL equipment enables next generation wafer bonding processes that deliver high performance and process efficiency

Laser Trimming System: Ulucus™ L

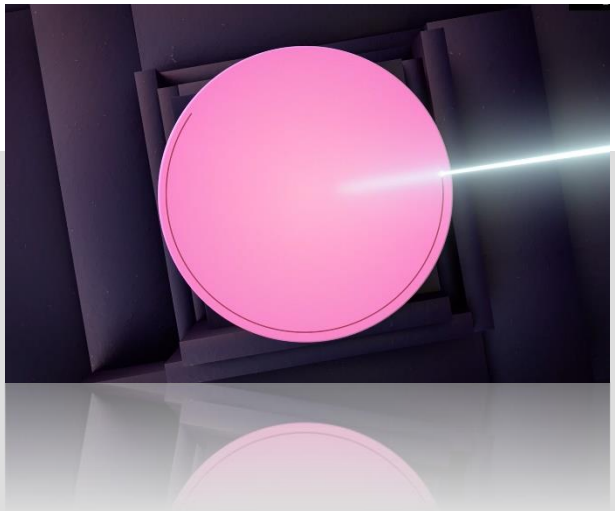
- Concept
  - Edge trimming on bonded wafer
  - Latest platform utilizing super clean technology from the front-end process, with the integration of laser control technology

Laser technology realizes high accuracy and quality trimming processes, and environment-friendly capability through the reduction of DIW usage

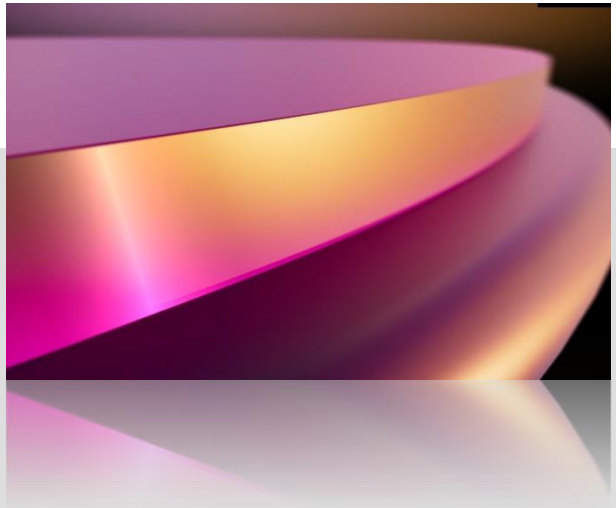
Laser Trimming System

Revolutionize wafer bonding process with laser technology

Enhance yield and significantly reduce the use of DIW in the edge trimming process



Higher Accuracy
Enabling narrower trimming width



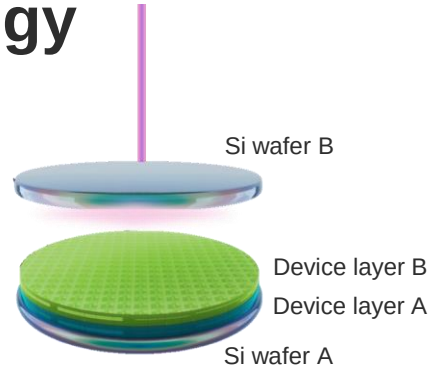
Smooth Sidewall
Less damage, Better yield

Higher Throughput
High productivity, Reliability

Save Water
Reducing DIW to 70% or more

Introducing Ulucus™ LX for Post-Wafer Bonding Process

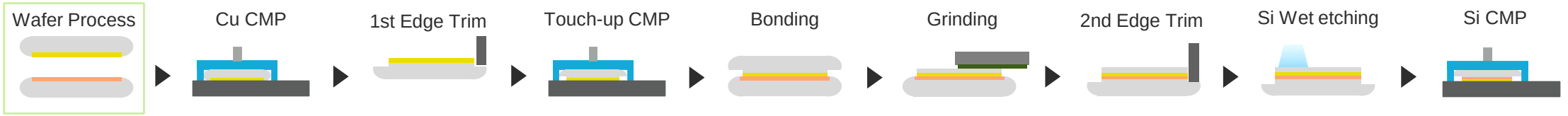
- **Extreme laser lift-off (XLO) technology**
  - Advanced thinning and critical technology for post-wafer bonding process
  - Unique laser technology enables separation of the Si-substrate from the device layer



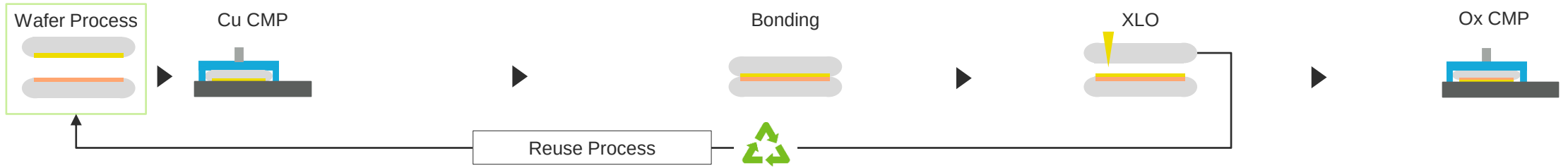
- **Advantages for process and environment**
  - Enhanced efficiency in silicon active areas
  - Fewer process steps required
  - Reduced need for DI water usage and CO_2 emission
  - Opportunity for wafer reuse
- **Equipment released in December 2024**

Ulucus™ LX Advantages

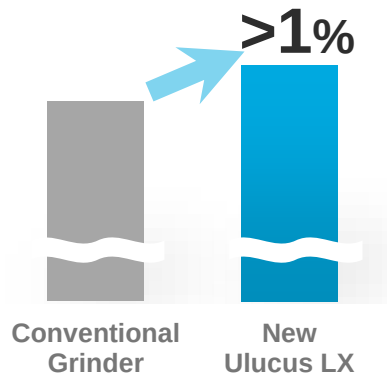
Permanent Bonding Process with Grinding & Blade Edge Trimming (Conventional)



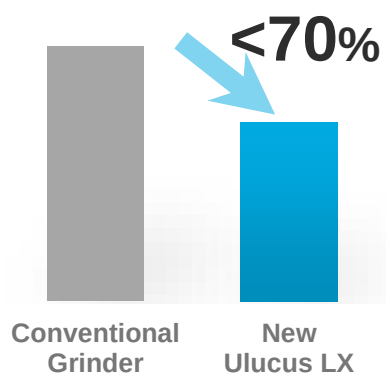
Permanent Bonding Process with XLO (Extreme Laser Lift Off)



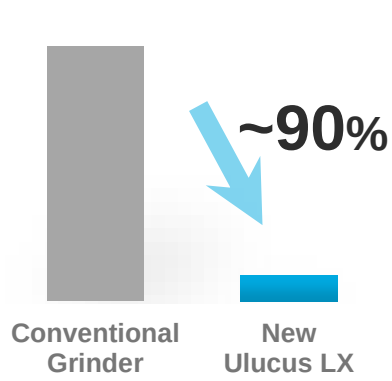
Active Silicon Area



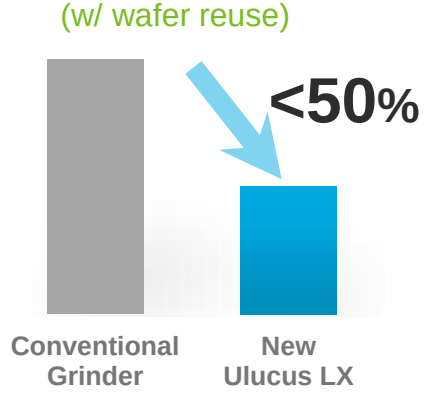
of Process Steps



DIW* Usage



CO_2 Emission
(w/ wafer reuse)



No Silicon Sludge
→ Advantage Over Grinder

Source: TEL

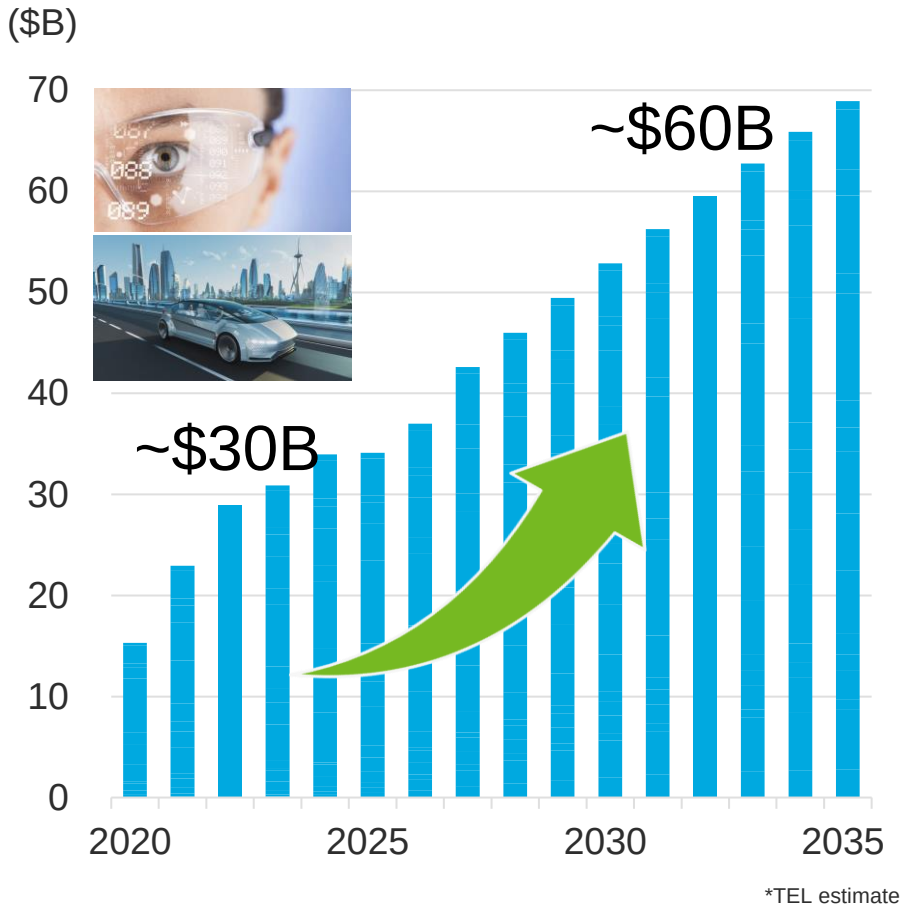
* DIW : De-ionized Water

8. MAGIC Market and Field Solutions Business Initiatives

MAGIC Market

- MAGIC Market to double
- Development & sales for MAGIC specialty applications
- Demo line ready for 200mm MAGIC
  - ✓ Yamanashi, Kumamoto, Miyagi
  - ✓ Massachusetts, Minnesota, Florida

- Market Estimates



*TEL estimate

Equipment for Mature Generations

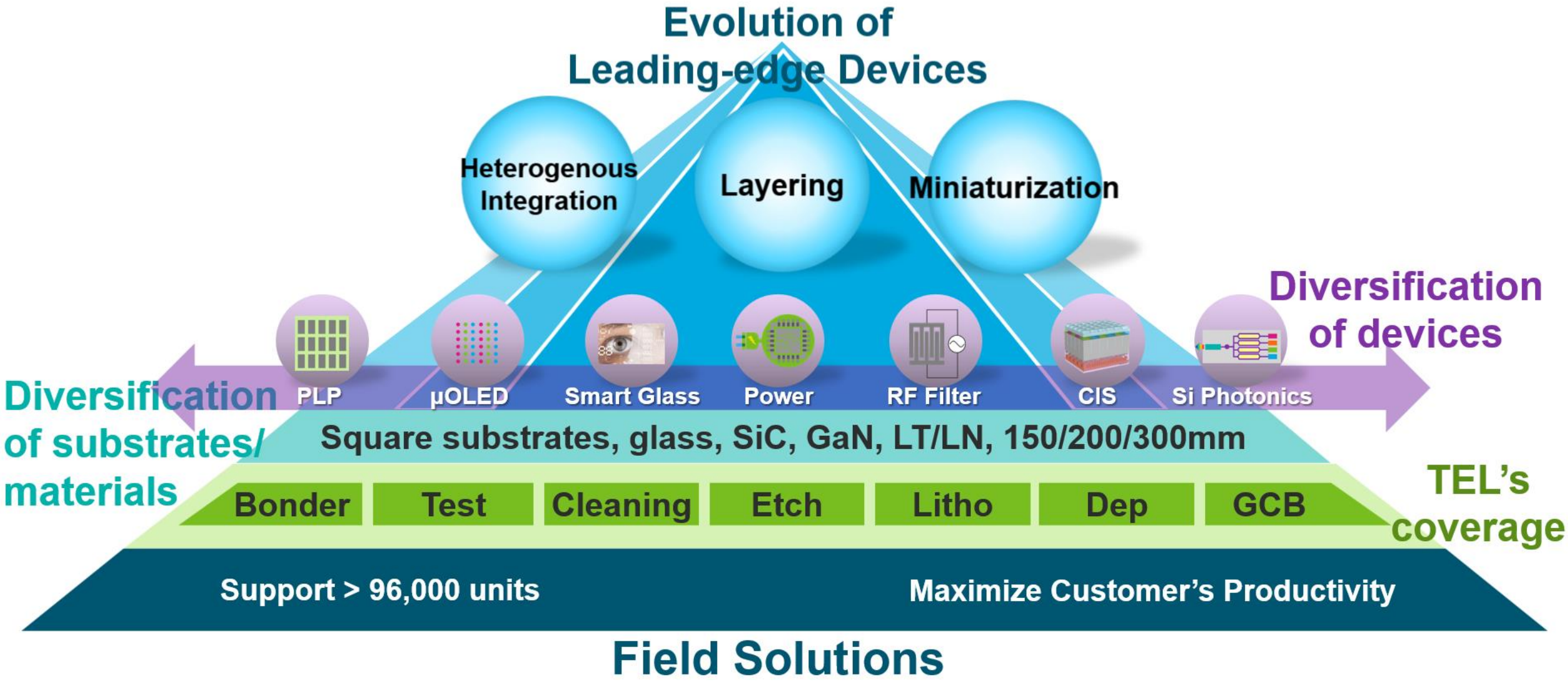
- Reengineered equipment for 200mm wafer
  - Thermal deposition systems, coater/developer, etch systems, etc.
  - Sales expansions not only for replacement demand of existing customers, but also for emerging customers

- Equipment for power devices
  - Equipment for SiC wafer, 300mm etch system
  - Respond to rapid growth in demand for power devices, such as for automotive

SiC epitaxial CVD system

By integrating our technological assets with new technologies, improve productivity and reduce impact on the environment

Providing Diverse Systems and Solutions for Diverse Needs

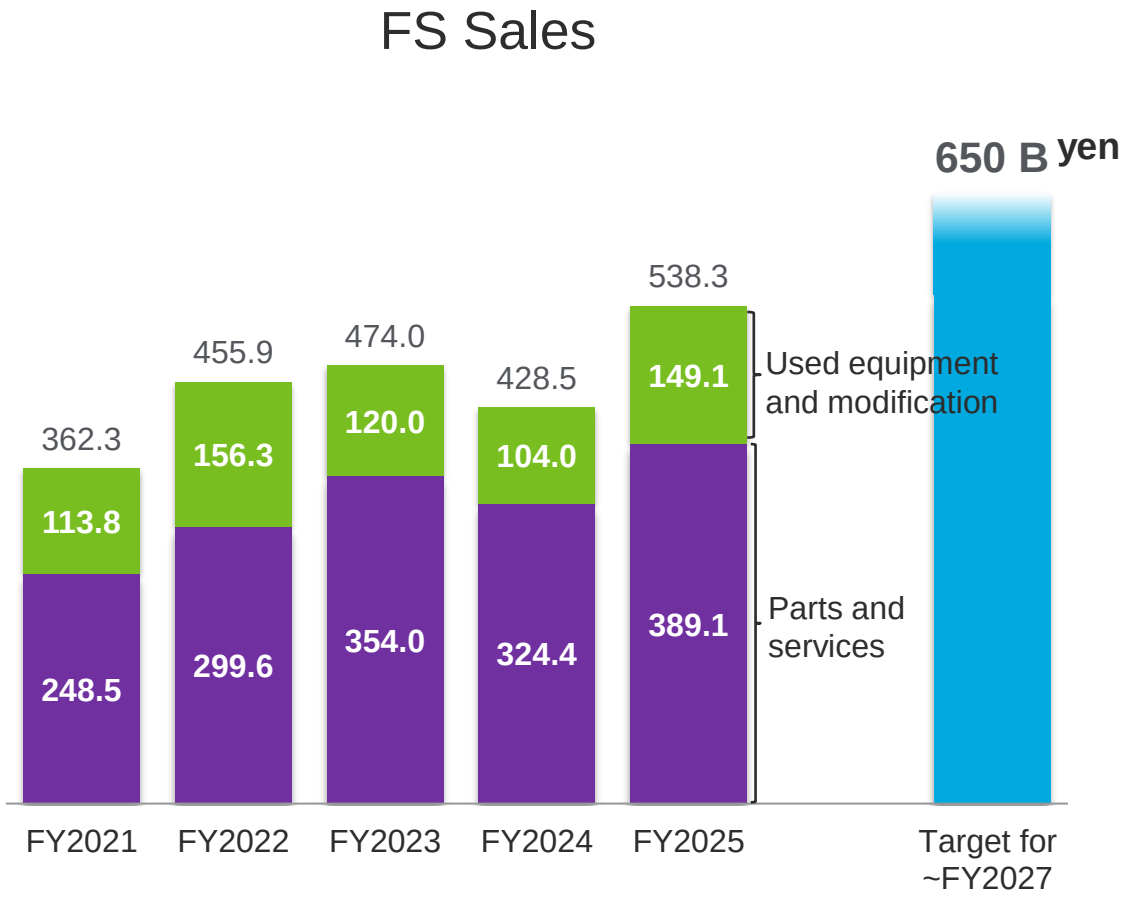


Basic Strategy for Field Solutions (FS)

- Expand sales for equipment for mature (legacy) nodes
- Deploying solution business based on installed base
- Development and promotion of advanced Field Solutions
  - Providing leading-edge and sustainable support that utilizes the latest technology, such as DX
  - Development of remote maintenance support and training tools
- Enhancing the front-lines engineers and capabilities
  - Continuous skill improvement for field engineers

Support customers to maximize their business operations
through services with high added value

Field Solutions (FS) Sales Results and Business Contents



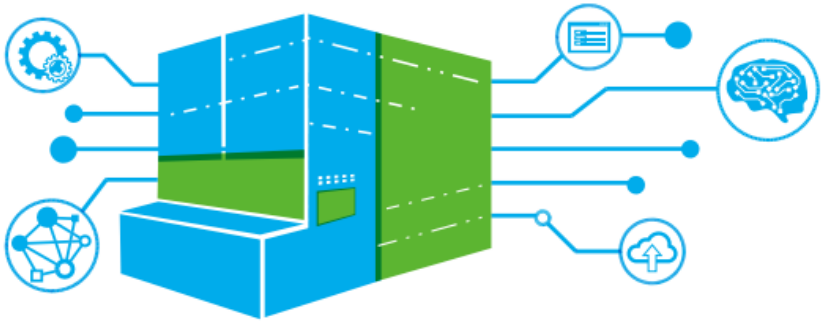
- Parts and repair
  - Predictive maintenance for parts deterioration
  - Appropriate parts inventory management and prompt delivery
- Services
  - Providing “comprehensive contract type” services that encompass everything from equipment delivery to after-care maintenance
  - Proposing solutions that address customer demands and maximizing equipment utilization rates
- Modification
  - Productivity improvement
  - Yield improvement

SAM*1 is expanding with 96,000*2 installed base currently and increasing by approx. 4,000 to 6,000 units each year

*1 SAM: Served available market
*2 As of December 2024

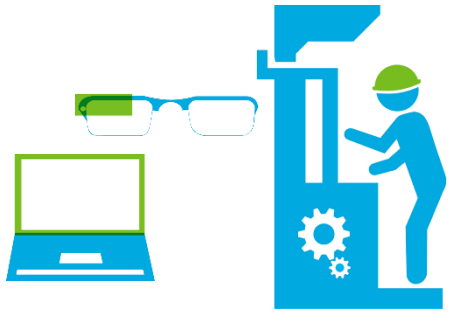
Advanced Field Solutions

TELeMetrics™



- Monitoring data on individual equipment
- Knowledge management and accumulation of problem case studies

Remote Support



- Minimization of downtime through predictive maintenance of equipment
- Remote support that enables prompt response even under travel restrictions

Strengthen Global System

- Provision of support that takes advantage of time differences
- Parts management and delivery through advanced logistics
- Engineer training program

Proposing solutions with high added value centered around “TELeMetrics™” that utilize DX

9. Digital Transformation (DX) Initiatives

Leveraging Digital Transformation (DX)

Best Product Dev. | Start up / Process Ramp up | Production | Best Service Delivery

MI (Materials Informatics) | Self-diagnostics (Sensors) | Robotics

PI (Process Informatics) | High Throughput Platform | AR/VR

Developing digital enablers for use throughout the business
to leverage productivity and profitability

Leveraging Digital Transformation (DX) in Field Solutions

Maximize work efficiency for startup and maintenance in the Clean Room by using smart glasses and remote expert support. Use of AR/VR and DX including digital twin technology.

Use of robots for parts replacement without human assistance is expected to minimize downtime and improve the quality of engineering work.

TEL DX Vision

- The tide of DX ripples throughout the industrial world as a whole, and the semiconductor industry is no exception. It is positioned as a part of the solution toward further demands for die miniaturization and layering

AI Chip


Autonomous


Cloud Service

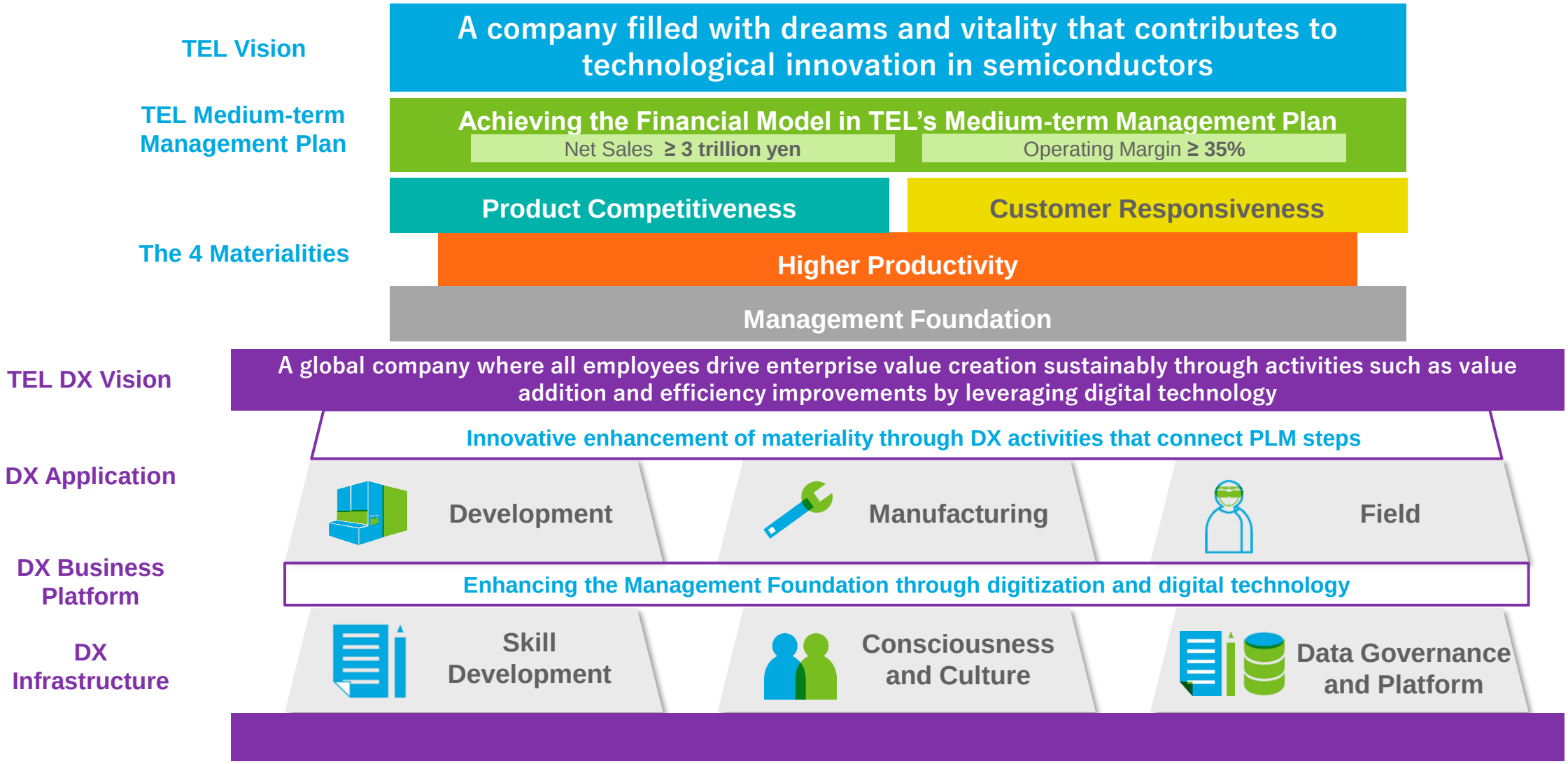

AR/VR

TEL DX Vision

A global company where all employees drive enterprise value creation sustainably through activities such as value addition and efficiency improvements by leveraging digital technology

DX activities are ultimately a method and an opportunity to realize sustainable creation of corporate value. We have defined the image we must achieve (our “To-Be Image”) in order to realize transformation

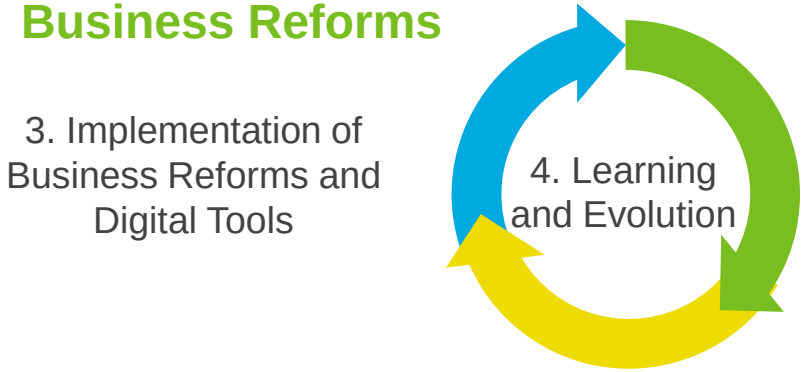
TEL DX Grand Design



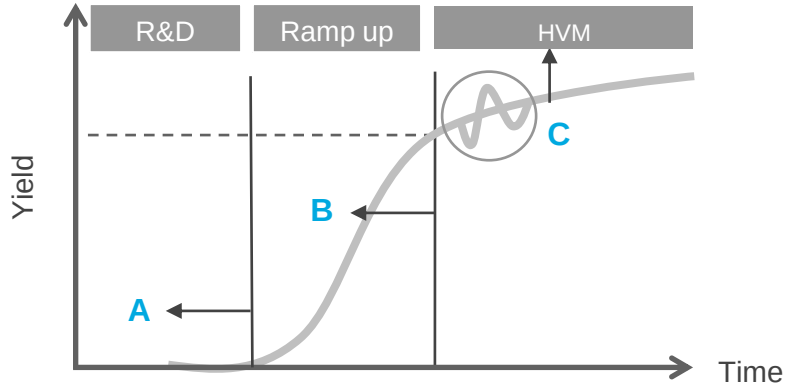
Steps of DX Activities

Product Innovation

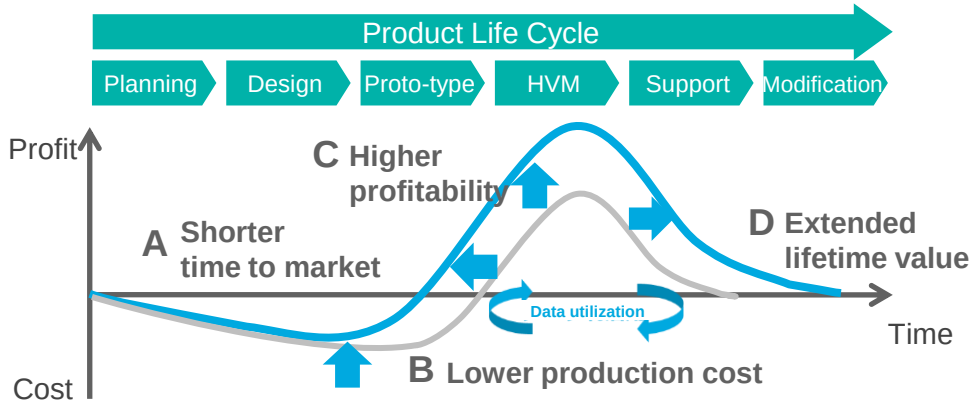
Business Reforms



DX in Contributing to Customers' Value Creation



DX in Raising Capital Efficiency



Solving issues of a higher dimension through digital transformation

Relationships between Projects in DX-related Developments

Equipment Foundation

- Development of equipment frames
- Development of equipment foundation technologies

Added Value Application

- Development of equipment AEPC
- Development of service tools
- Development related to measuring instruments

DX Foundation

- Company-wide DX training
- Data lake maintenance
- Maintenance of environments for DX development

Capital Efficiency/ Management Foundation Application

- Development of apps for equipment
- Development of apps for the field
- Development of apps for GBP

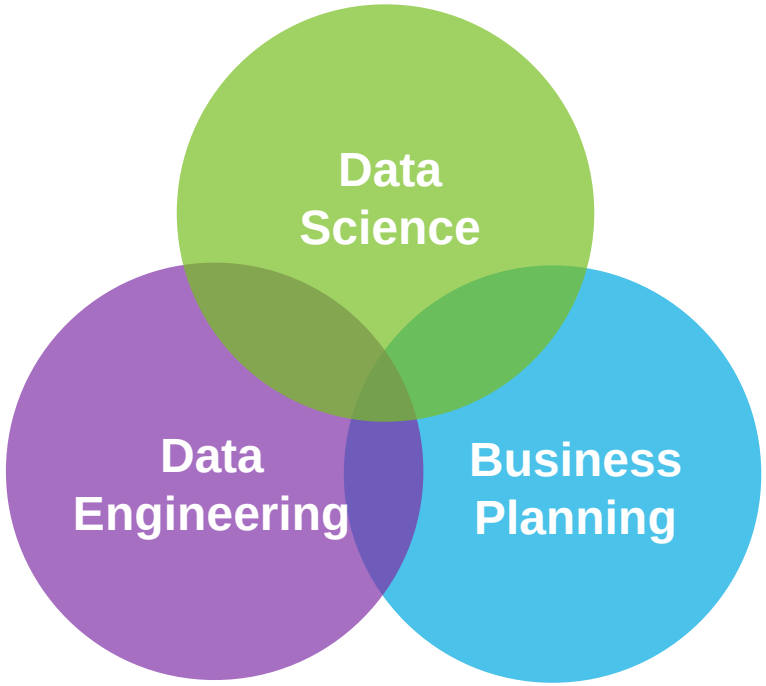
Quality

Time

Talents

Through a DX foundation and DX that improves capital efficiency,
we will improve the quality and speed of our work,
and transition toward a use of time that creates even greater value

DX Engineer Training Plan



All Employees

The ability to understand and utilize knowledge of information science, such as cutting-edge information processing, artificial intelligence and statistics

The ability to realize a form of data science that meaningfully contributes to TEL's creation of corporate value, and to practice and operate data science in a manner that fits our purposes

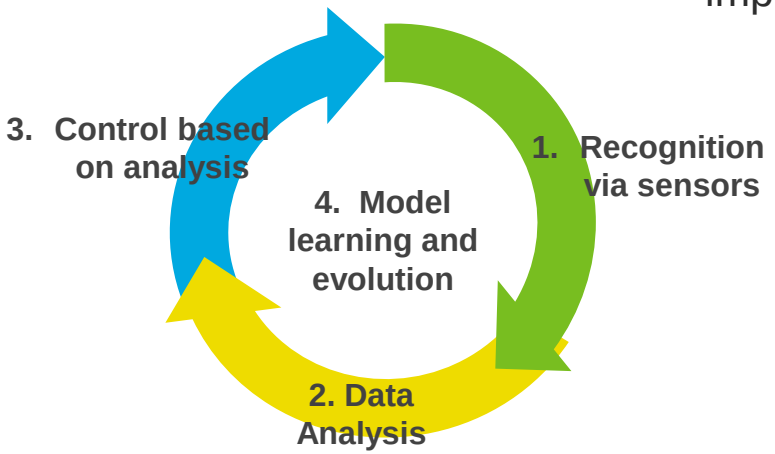
The ability to organize issues and their backgrounds, derive solutions, and connect them to our business

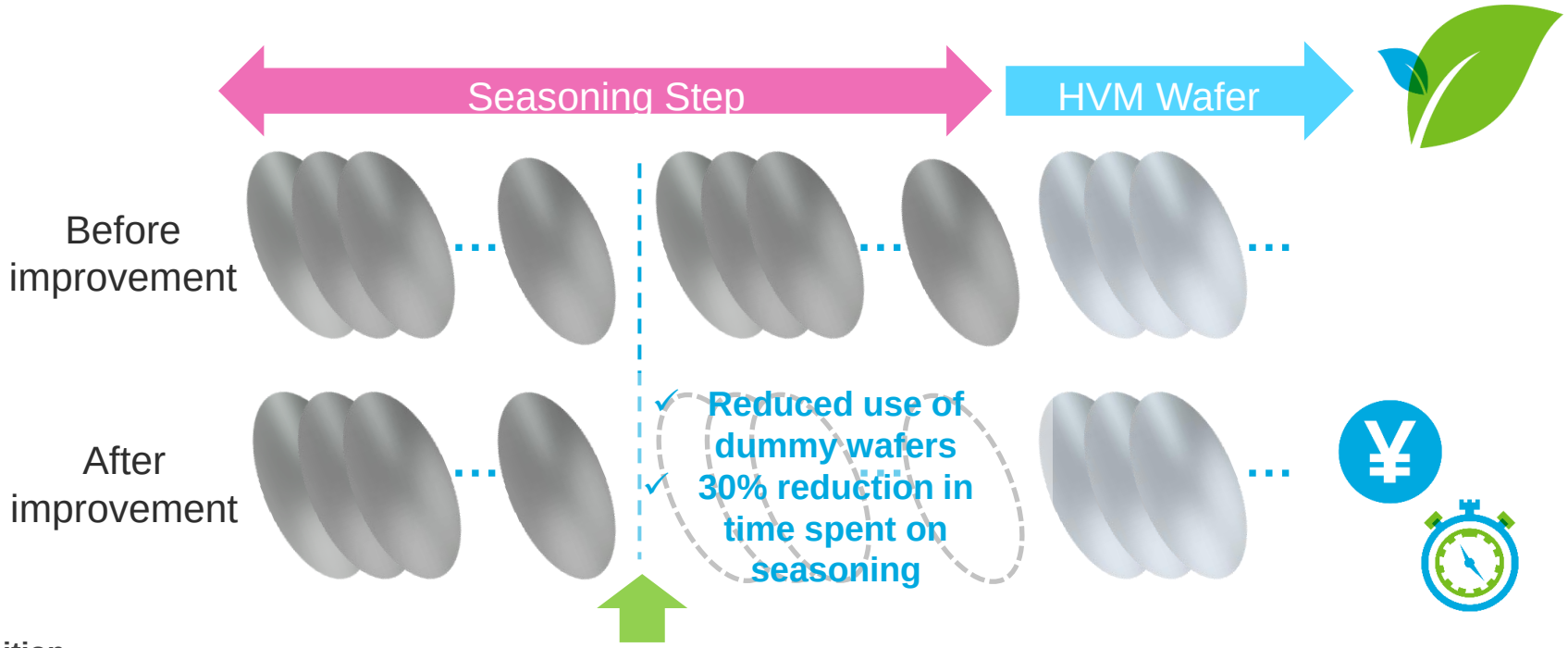
Utilizing data and digital technology in our day-to-day business operations in order to optimize our business operations and create added value

Engaging in planned training to foster personnel who can capitalize data science in TEL's business

Example Activity 1 – Increasing Productivity of Equipment:

Improving Utilization of Etch Equipment





Seasoning at the right time with endpoint detection

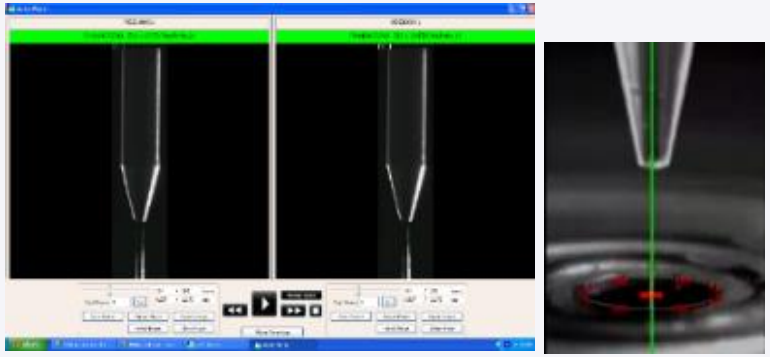
*ISSM 2020, from "Seasoning Optimization by using Optical Emission Spectroscopy," published by the Company

Feedback from the sensor provided an appropriate understanding of chamber conditions and improved utilization of equipment

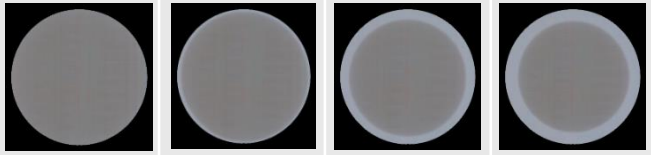
Example Activity 2 – Increasing Operation Cost of Equipment:

Reducing Chemicals of Coater/Developer

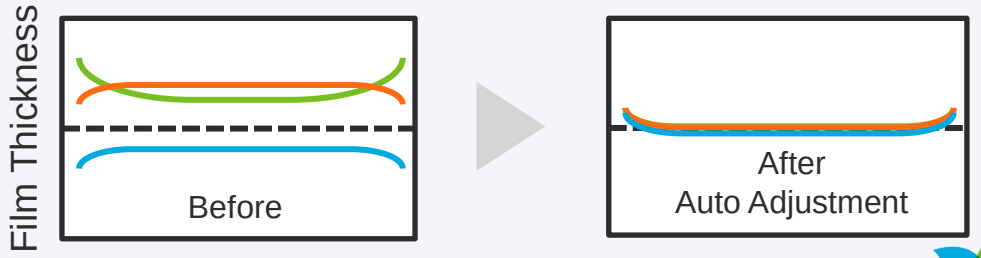
Monitoring of chemical discharge status
using image processing technology

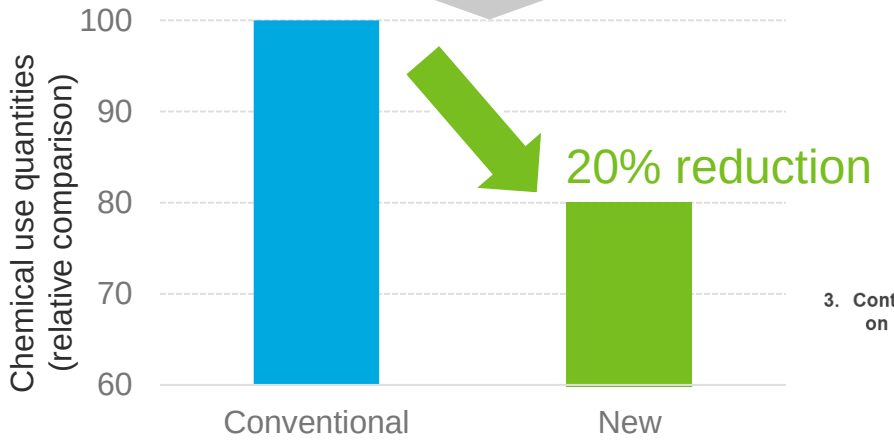


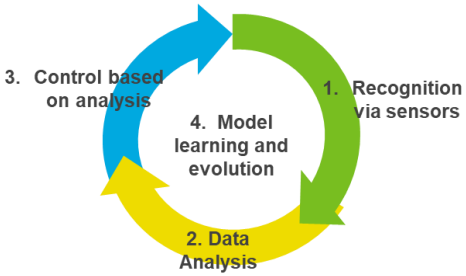
Monitoring of chemical coverage of interior of surfaces
using image processing technology

Dispense Volume	X ml	Y ml	Z ml	A ml
Judgement	Passed	Passed	Failed	Failed
Wafer image by WIS				

Automatic film thickness adjustment function

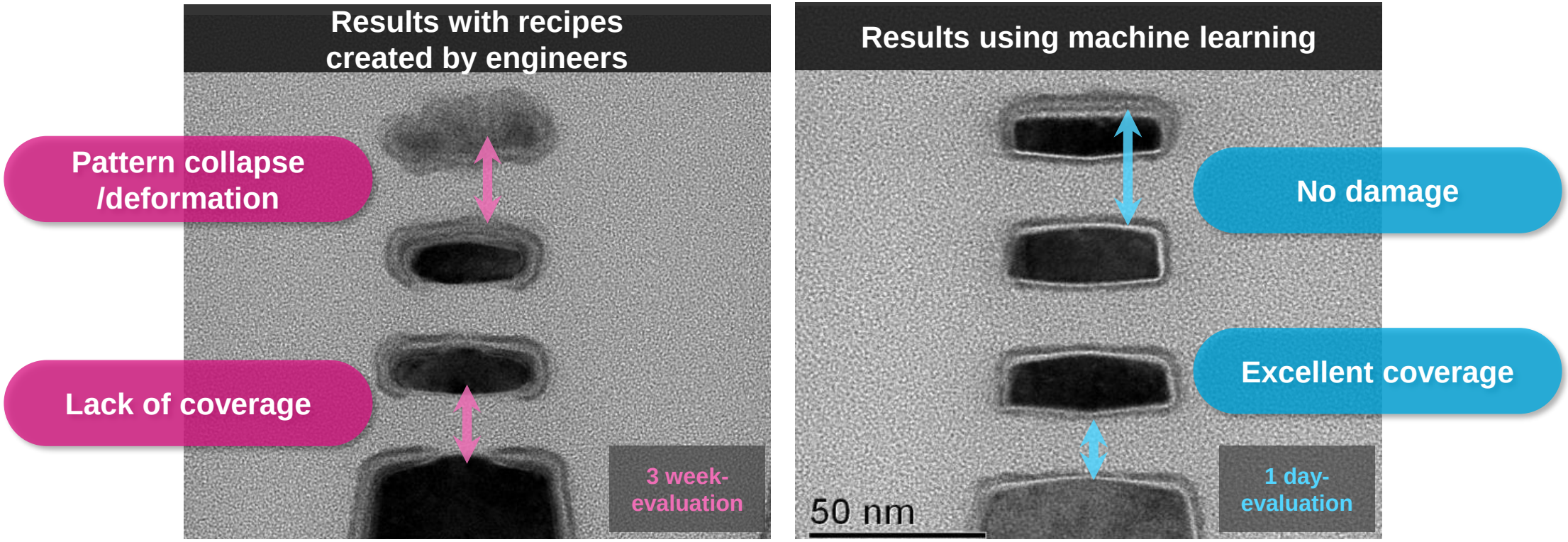






Contributed to customer operation costs
and the environment by using machine learning

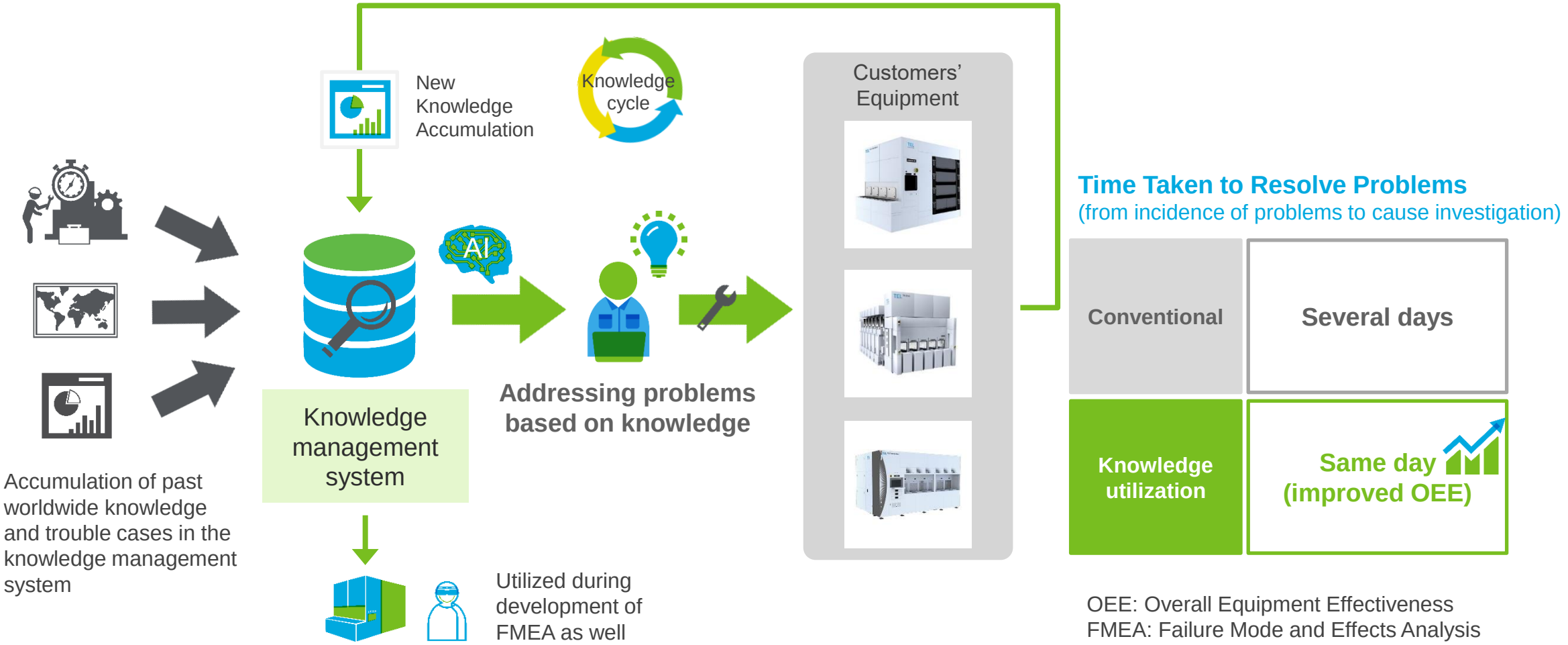
Example Activity 3 – Increasing Productivity of R&D:
Process Informatics



Source: Tokyo Electron Technology Solutions Limited / Tokyo Electron Limited

Achieved good step coverage with no pattern deformation in the ALD process by machine learning

Example Activity 4 – Improving Overall Equipment Effectiveness



OEE: Overall Equipment Effectiveness
FMEA: Failure Mode and Effects Analysis

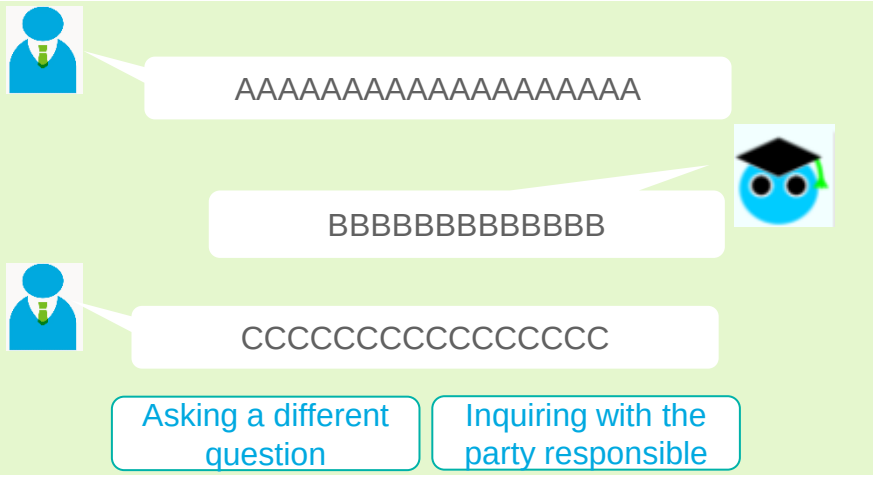
Using the Knowledge Management System to reduce the time taken to resolve problems and improve equipment operation rates

Example Activity 5 – Increasing Productivity of Operations:
Optimizing Business Operations by Implementing Chat-bots in Back-Office Work

Legal Department, Finance Department, Personnel Department, General Affairs Department

Responding department

- Reduce the number of inquiries, man-hours spent on inquiries
- Share know-how to resolve issue of tasks becoming too personalized, train younger employees



- Make it possible to answer using choices or free input
- If chat-bot cannot provide an automated answer, make it possible to use the system to engage in inquiries
- Realize a smarter system by analyzing user histories and adding FAQs

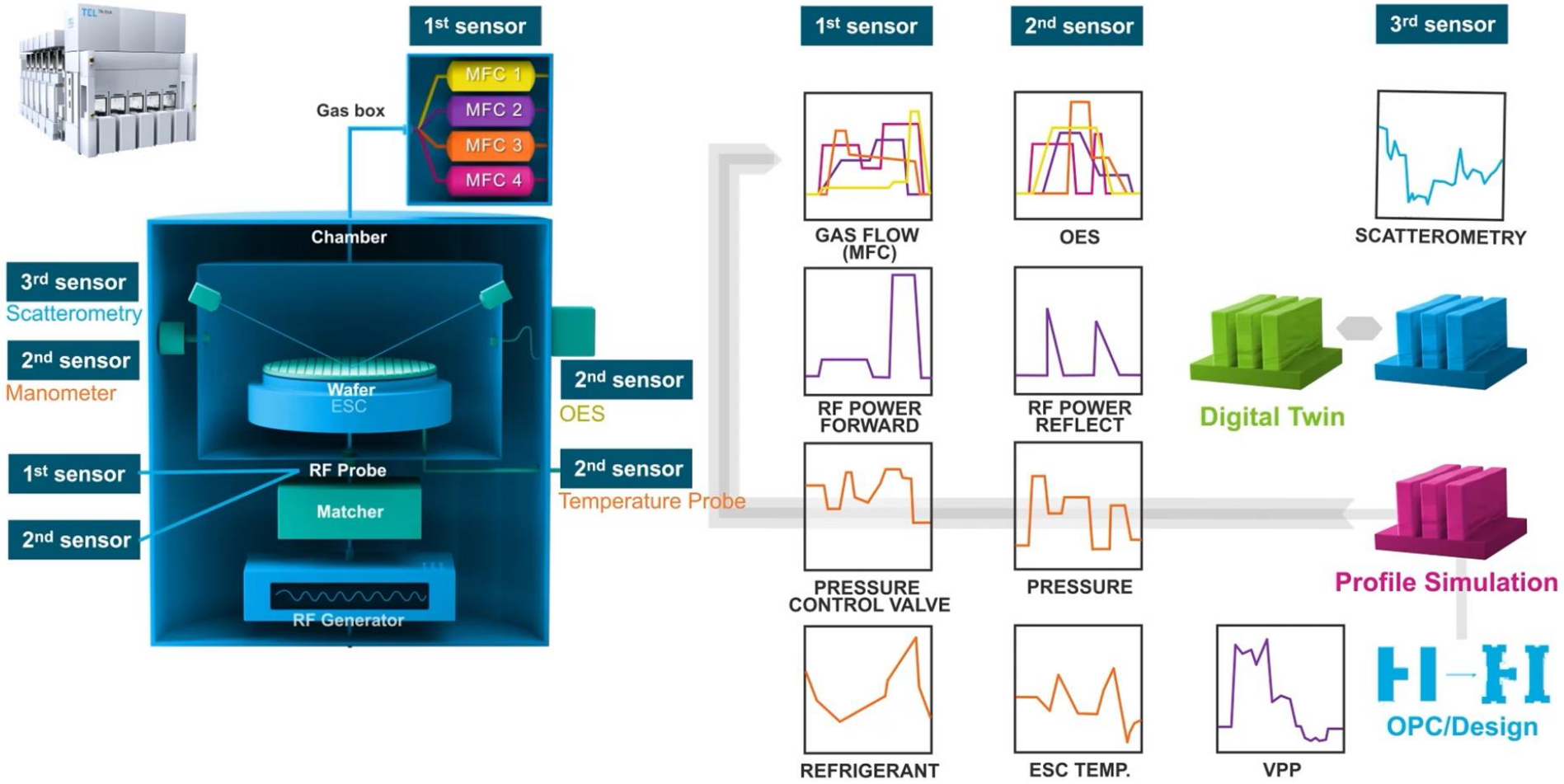
Employee

- Make it possible to ask questions any time without hesitation
- Clarify the departments responding to inquiries
- Reduce variability in answers based on the person in charge

Reduced the number of man-hours spent by employees answering questions with introducing chat-bots in multiple departments

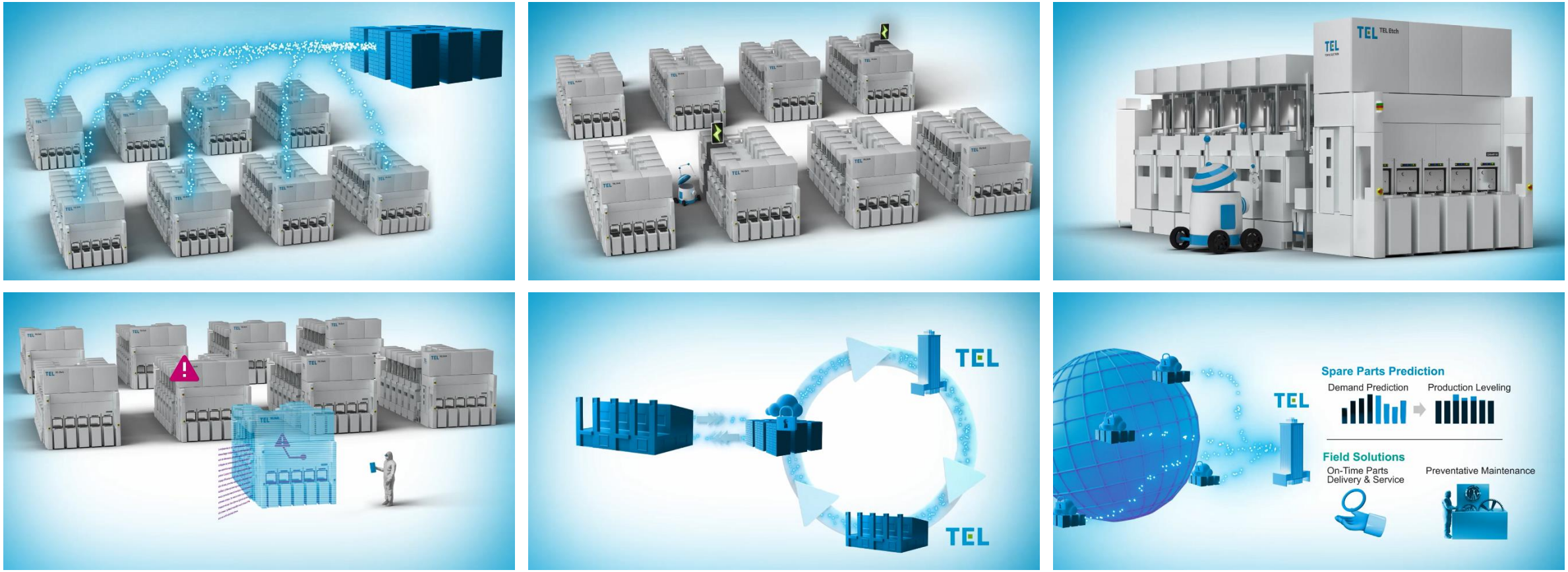
Digital Technologies to Increase Customer Value 1:

Example in Etch Equipment



Aiming to maximize customer value using all digital technologies

Digital Technologies to Increase Customer Value 2:
Example in Etch Equipment

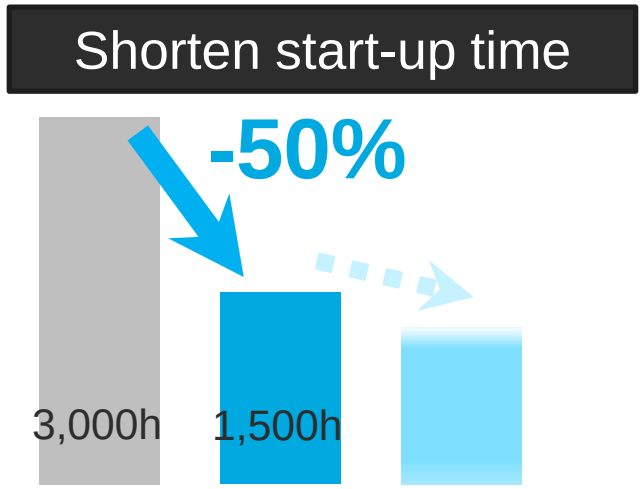


Aiming to maximize customer value using all digital technologies

10. Procurement and Manufacturing Strategy

Continuous Production Innovation in Pursuit of Safety, High Quality and High Reliability

- Build a production system able to quickly respond to market changes
- Shorten time from new product development to mass production
- Shorten production lead times: Achieve 100% module shipment
- Utilize DX and automation in manufacturing, and expand automated warehouse
- **Significantly reduce equipment start-up time (One-touch start-up)**
  - Reduce start-up time up to 75% (primary target), One-touch (final target)

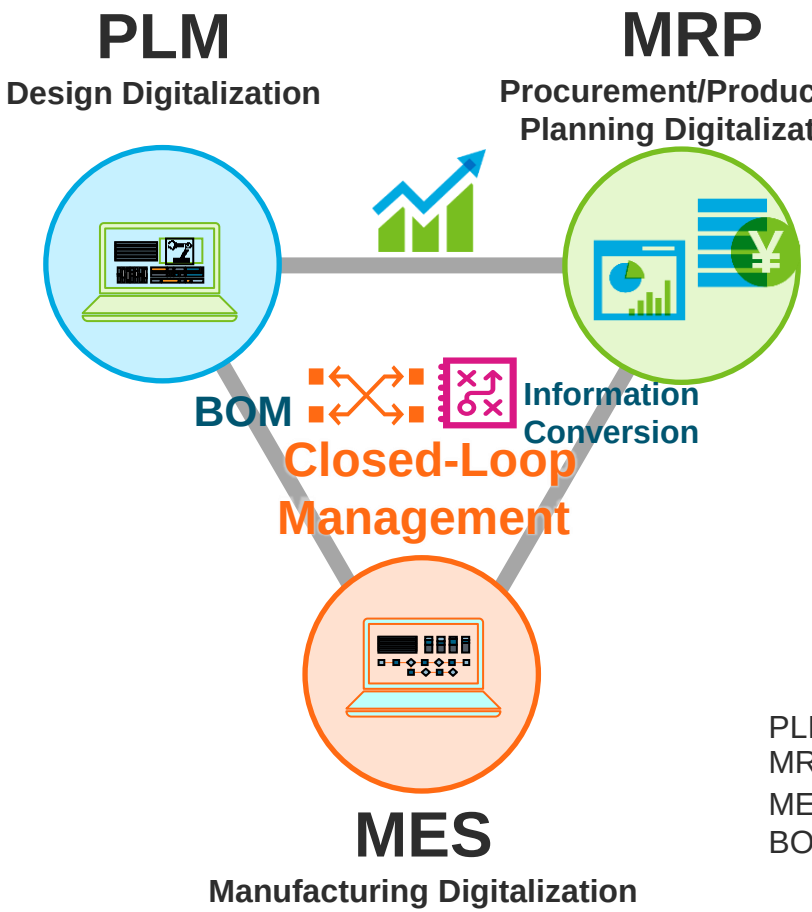


Conventional ➔ after production innovation

Expected outcome from shorten start-up time

- Enhance productivity and start-up quality
- Reduce accident risks
- Optimize resources and the work-life balance

Efforts to Utilize TEL PLM-DX and Improve Productivity and Efficiency



TEL PLM-DX

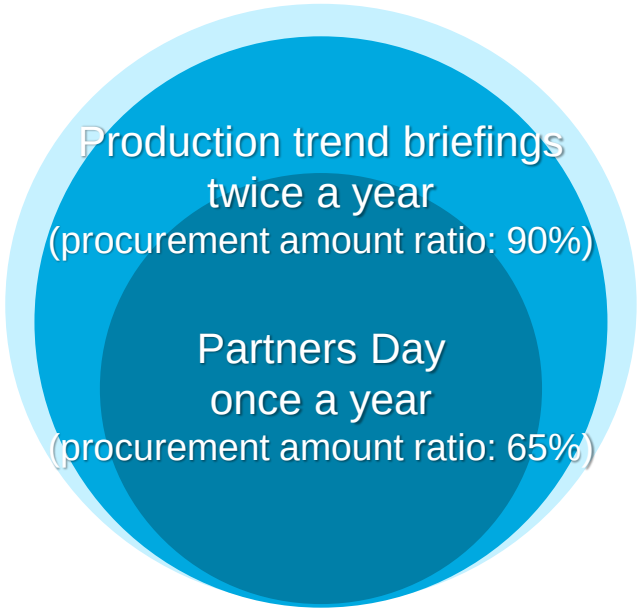
PLM: Product Lifecycle Management
MRP: Material Resource Planning
MES: Manufacturing Execution System
BOM: Bill of Material

- Improve core system
  - Production leveling < 12 months
  - MRP processing capability for procurement increased 10-fold
- Introduce PLM-DX and BOM concept
  - Enhance production capability up to 2 times within 3 years
  - Minimize manufacturing lead time
  - 3-fold increase in design efficiency
  - Reduce new product development period by half

"Shift Left" production plan toward the business scale of 1 trillion-yen procurement

Build a Sustainable Supply Chain

- Fair and transparent relationships and reliable trust relationship with our business partners
  - – Implement CSR/BCP assessments based on industry codes of conduct
  - – Share knowledge in such areas as safety, quality, the environment and compliance



E-COMPASS

Applaud environmental impact reduction activities, adding environmentally related items to assessment studies

- ✓ Reduce CO_2 emissions and the amount of energy usage
- ✓ Introduce renewable energy
- ✓ Promote resource conservation
- ✓ Promote waste reduction and recycling
- ✓ Promote activities for reducing the environmental impact of logistics

Procurement BCP and Proactive Procurement Activities

Mid- and long-term forecast
Promote “Shift Left” procurement strategy
Build BCP system resilient to procurement difficulty

Safety stock
Inventory liquidity

Oversee whole supply chain from upstream to downstream
Visualize and grasp risks

Visualize supply chain

Supply chain responsive to any kind of risks (Raw materials, parts, processing and assembly)
Strong and reliable supply chain

Risk management on business partners
Strengthen partnership

Measures for procurement BCP

Early procurement of parts

- Early procurement for long term
- Ensure inventory exchange flexibility among factories
- Inventory reductions in total

Secure semiconductor devices

- Secure semiconductor devices for our equipment
- Visualize and streamline distribution channel
- Collaborate with semiconductor makers

= TEL can be a customer of our customers

Parts and Suppliers

- Identify and analyze risk parts
- Multi sourcing of producing countries
- Standardization, centralization and decentralization of parts
- Measures to secure capacity for us

New Production Building Construction at Tokyo Electron Miyagi

- Total floor area: Approx. 88,600m^2 (planned; excluding the ancillary facility area)
- Structure: Steel frame structure with a base isolation system
- Number of floors: 5 above ground
- Construction cost: Approx. 104B yen
- Purpose: Manufacture of etch systems

New Production Building
(Completion scheduled for summer 2027)

Realize the Smart Production concept
by automating logistics functions and mechanizing manufacturing processes
to provide high production capacity/quality/efficiency production lines

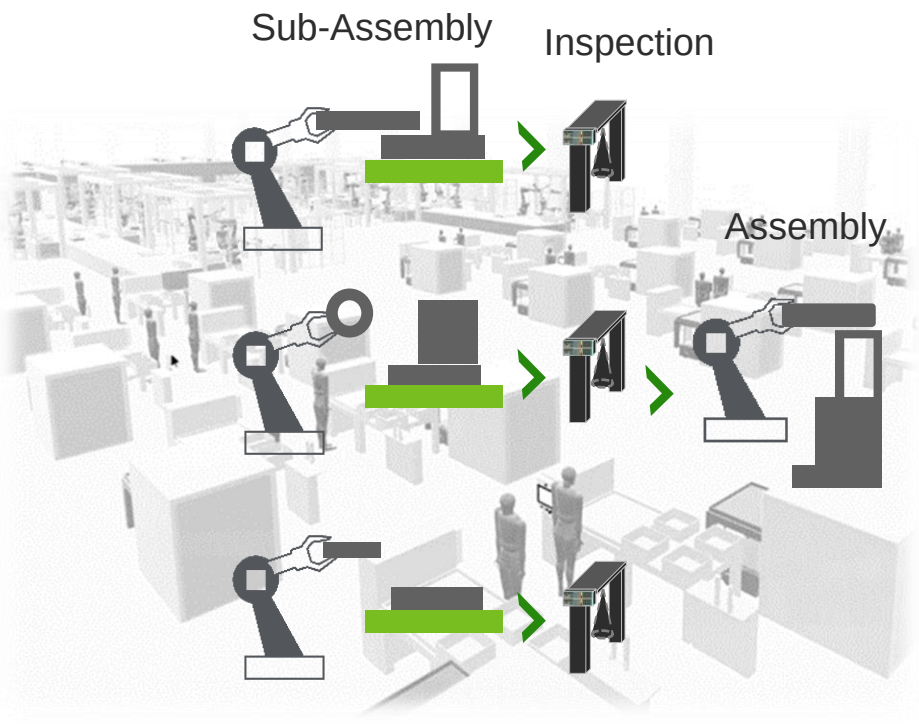
Smart Manufacturing to Achieve High Quality and Productivity

Development & Design

Feed Forward

Feedback

Smart Manufacturing



By centralizing development and production in TEL Miyagi,
we ensure continuous concurrent engineering and advanced manufacturing capabilities

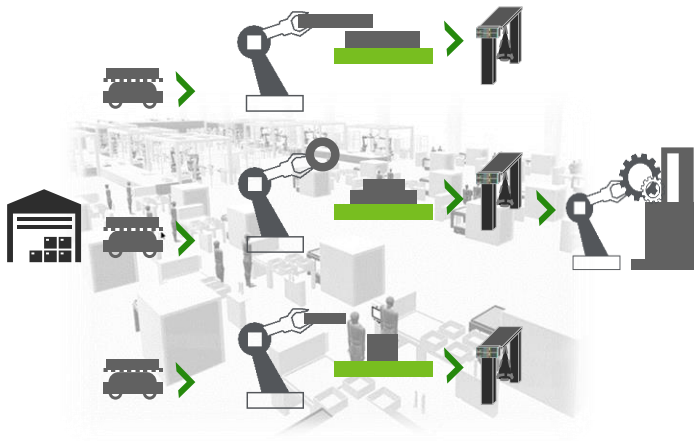
Vision for Smart Production

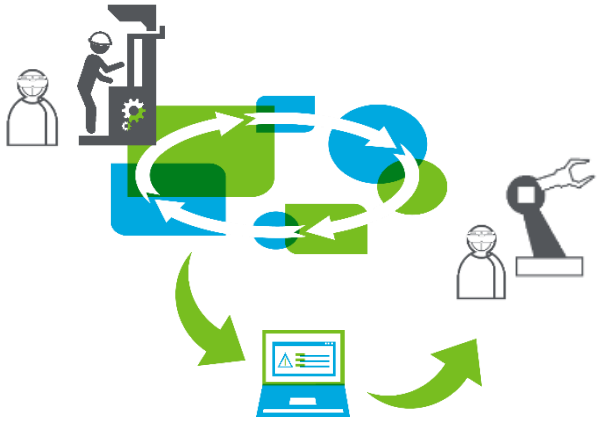
- Achieve sustainable manufacturing for the future

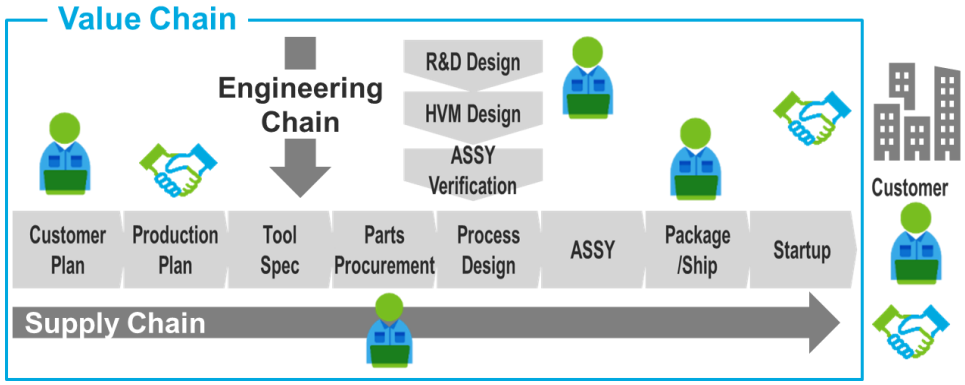
Overwhelming Efficiency
through automation and standardization

Enhancing Adaptability
to internal and external environmental changes

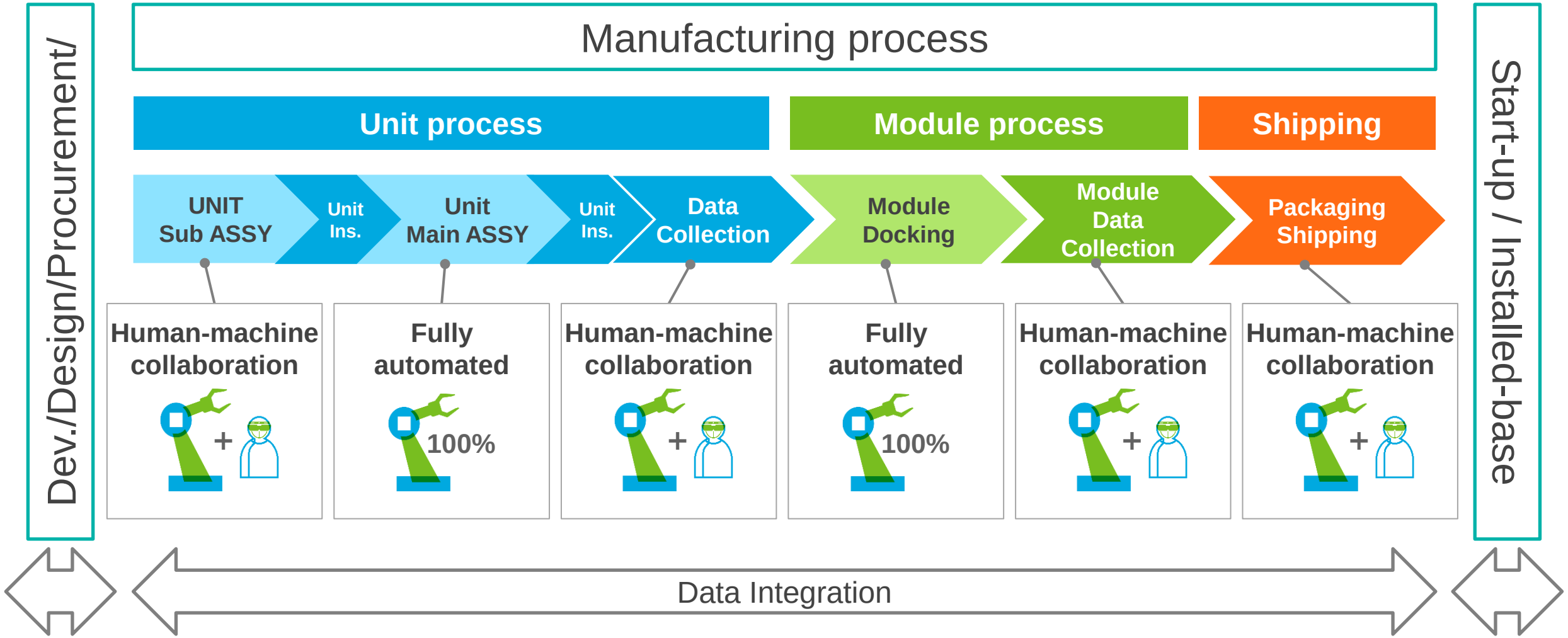
Product & Service Quality Improvement
through enhanced value chain







Concept of Smart Production



Appendix：Data Section

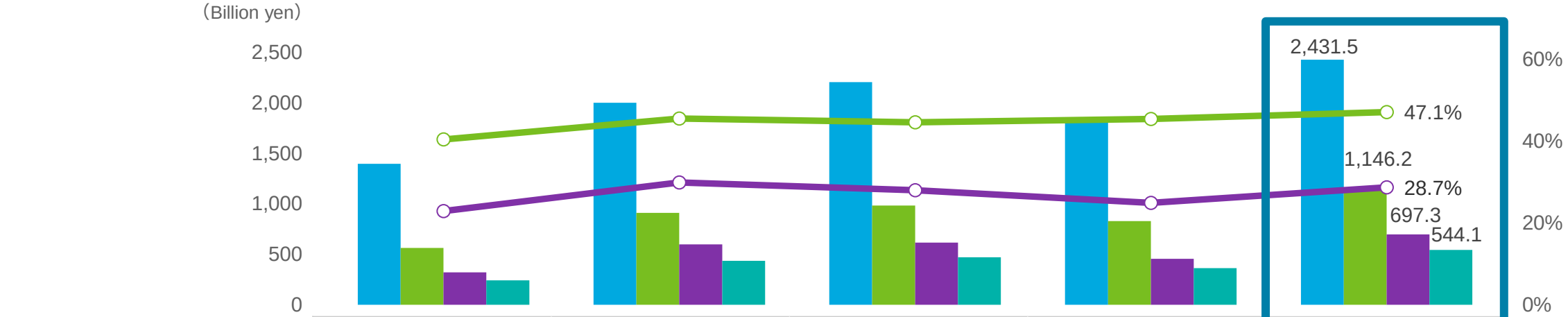
Financial Summary

(Billion yen)

	FY2024	FY2025	FY2025 vs FY2024	(Reference) FY2025 estimates announced on February 6, 2025
Net sales	1,830.5	**2,431.5**	+32.8%	2,400.0
Gross profit	830.2	**1,146.2**	+38.1%	1,129.0
Gross profit margin	45.4%	**47.1%**	+1.7pts	47.0%
SG&A expenses	374.0	**448.9**	+20.0%	449.0
Operating income	456.2	**697.3**	+52.8%	680.0
Operating margin	24.9%	**28.7%**	+3.8pts	28.3%
Income before income taxes	473.4	**706.1**	+49.1%	691.0
Net income attributable to owners of parent	363.9	**544.1**	+49.5%	526.0
EPS (Yen)	783.75	**1,182.40**	+50.9%	1,142.47
R&D expenses	202.8	**250.0**	+23.2%	254.0
Capital expenditures	121.8	**162.1**	+33.1%	170.0
Depreciation and amortization	52.3	**62.1**	+18.7%	63.0

1. In principle, export sales of Tokyo Electron's products is denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of foreign exchange rate fluctuations on profits is negligible, unless extreme fluctuations occur.
2. Profit ratios are calculated using full amounts, before rounding.

Financial Trend (FY2021~FY2025)

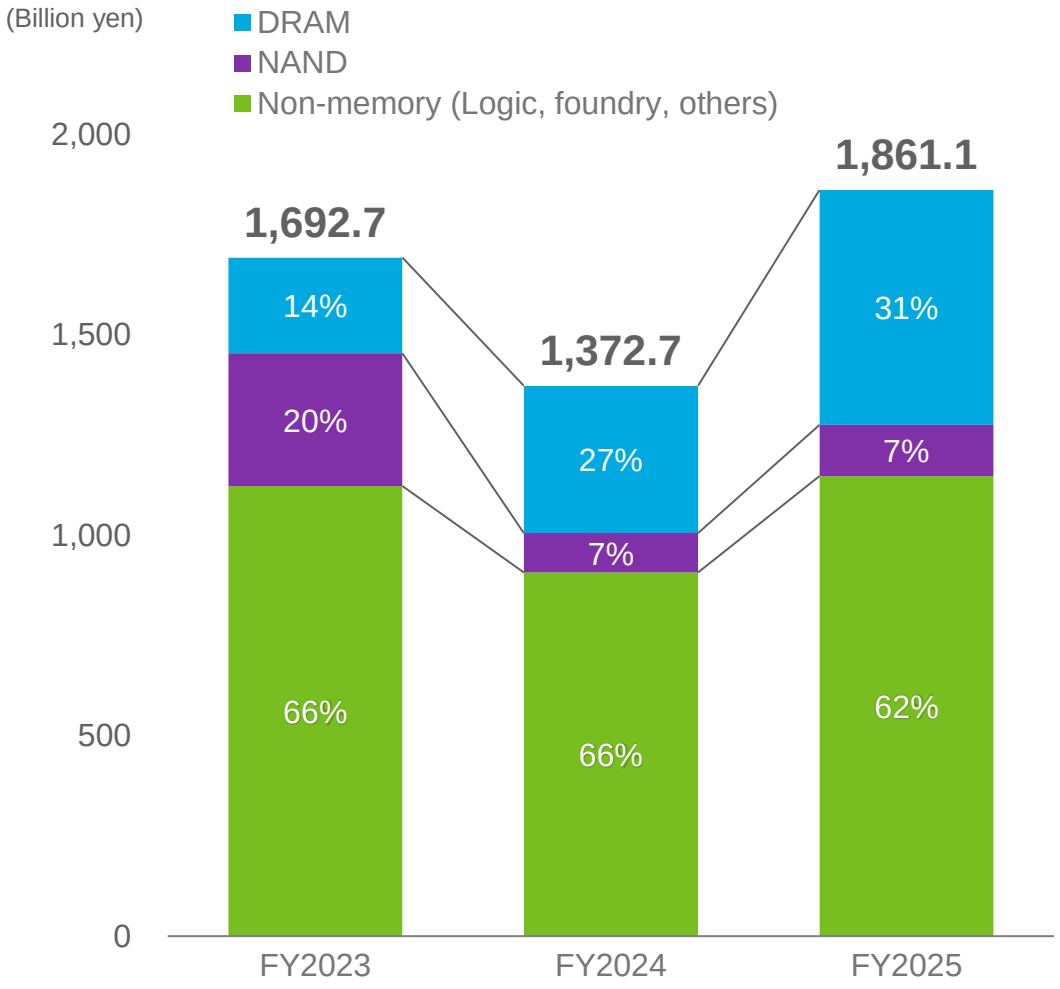


	FY2021	FY2022	FY2023	FY2024	FY2025
Net sales	1,399.1	2,003.8	2,209.0	1,830.5	**2,431.5**
Gross profit	564.9	911.8	984.4	830.2	**1,146.2**
Operating profit	320.6	599.2	617.7	456.2	**697.3**
Net income attributable to owners of parent	242.9	437.0	471.5	363.9	**544.1**
Gross profit margin	40.4%	45.5%	44.6%	45.4%	**47.1%**
Operating margin	22.9%	29.9%	28.0%	24.9%	**28.7%**
ROE	26.5%	37.2%	32.3%	21.8%	**30.3%**

From the beginning of FY2022, the Company applies “Accounting Standard for Revenue Recognition” (ASBJ Statement No. 29).

Net sales, gross profit, operating profit and net income reached record high

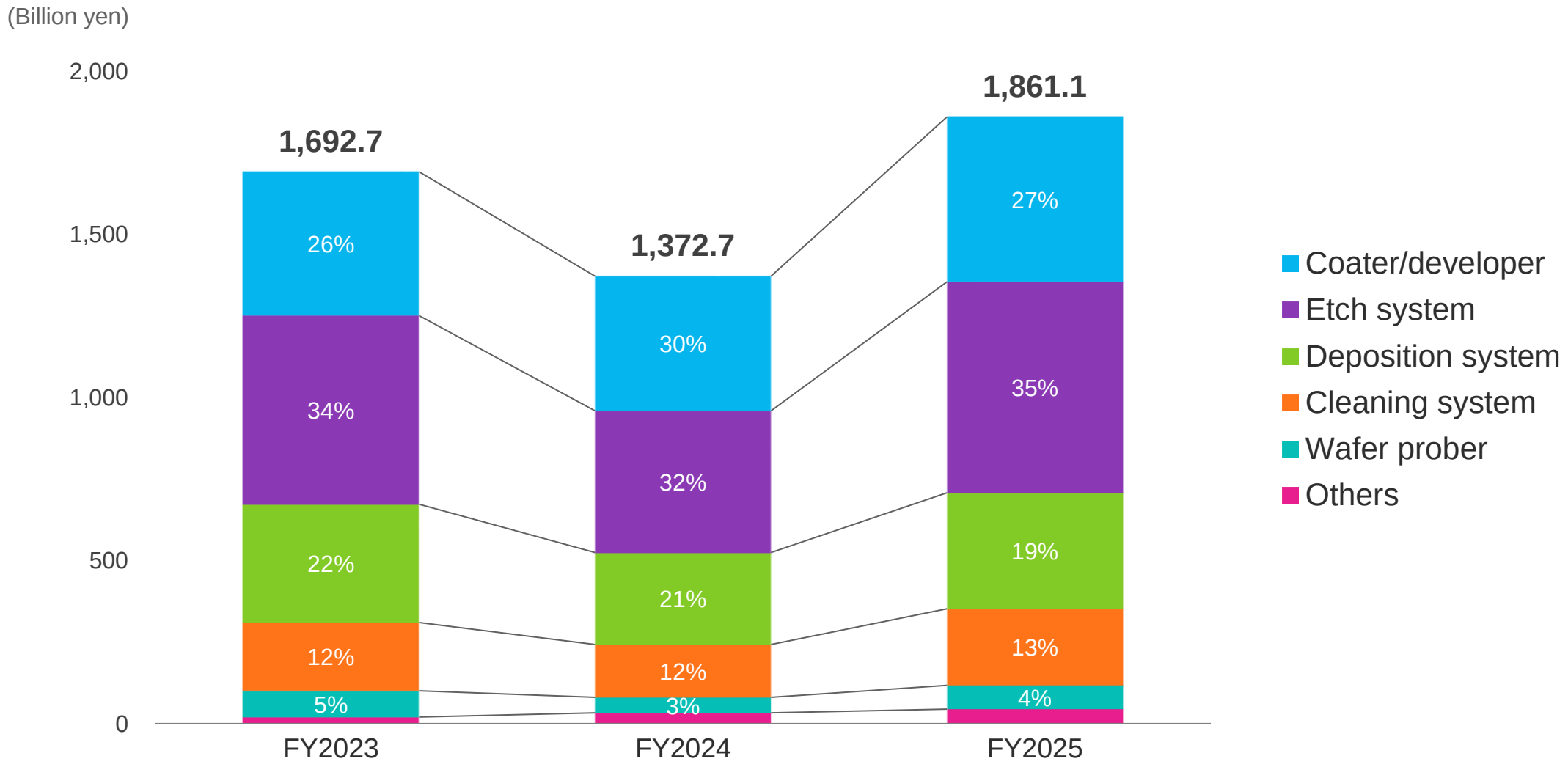
SPE New Equipment Sales by Application



- DRAM: Leading-edge investment (HBM etc.) was a significant contributor for higher sales and a larger composition ratio
- Non-volatile memory: Sales were on an upward trajectory despite the composition ratio remaining unchanged as customer investment eased towards a recovery
- Non-memory: Sales rose significantly on active investment in leading-edge nodes as well as demand for mature nodes

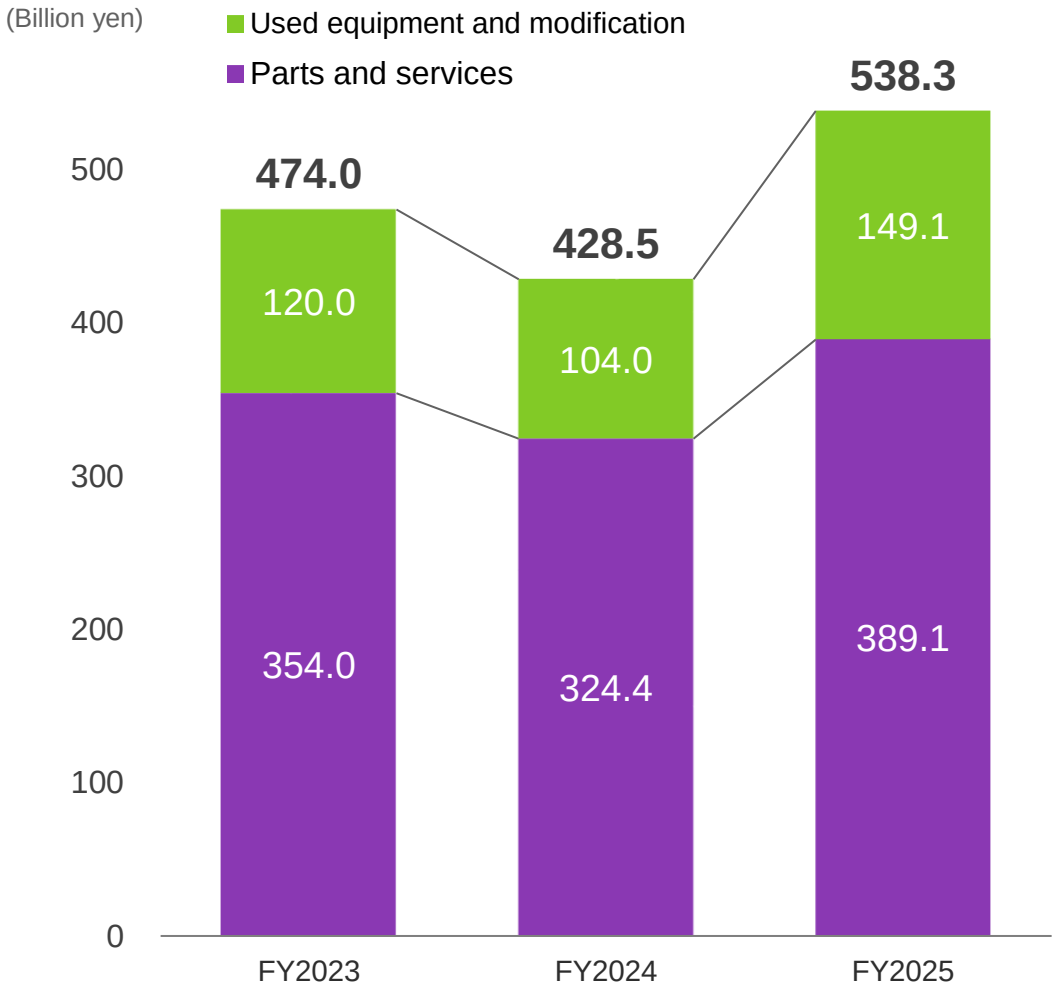
1. SPE: Semiconductor Production Equipment
2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

SPE New Equipment Sales by Product



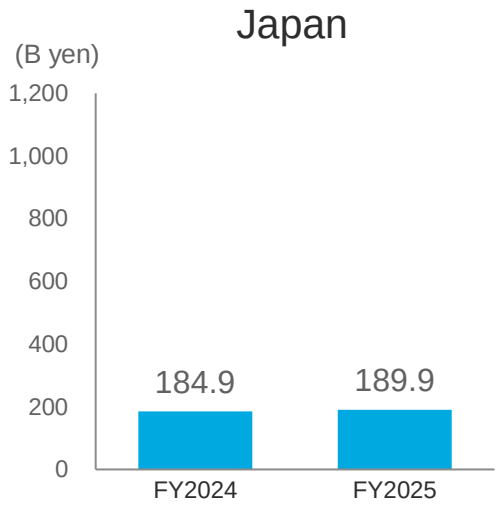
Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

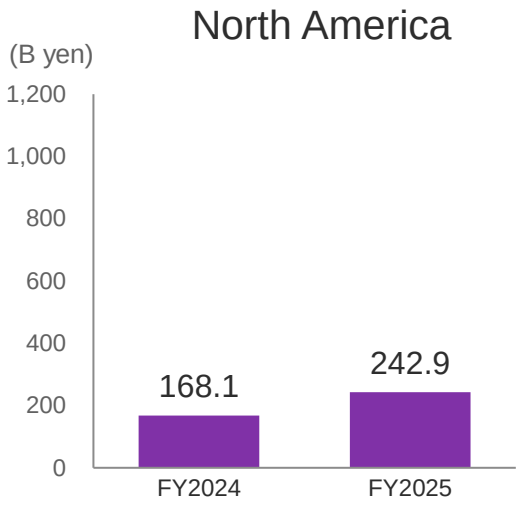
Field Solutions Sales

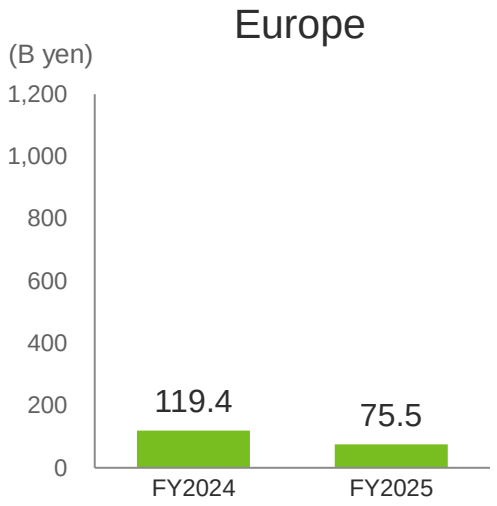


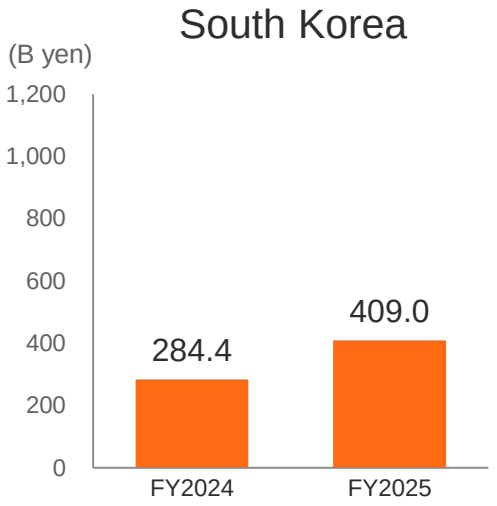
- Field Solutions sales in FY2025 were 538.3B yen, up 25.6% YoY
- Both parts and services and used equipment and modification sales were in good shape along with the recovery of customers' fab utilization rates

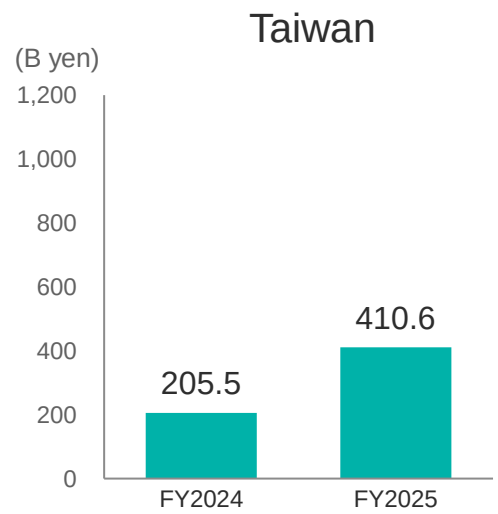
Sales by Region

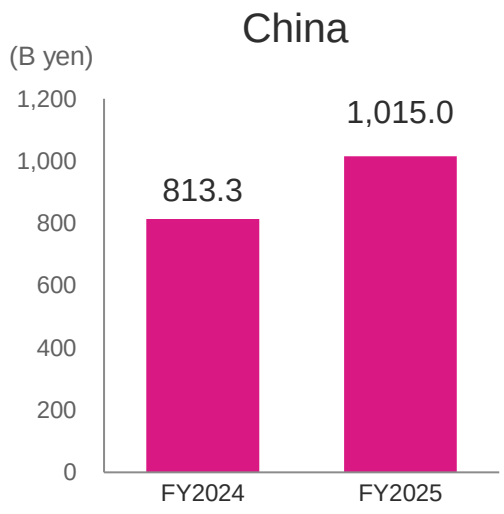


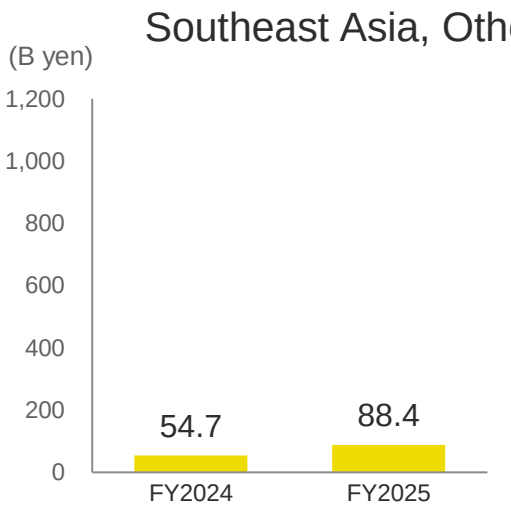


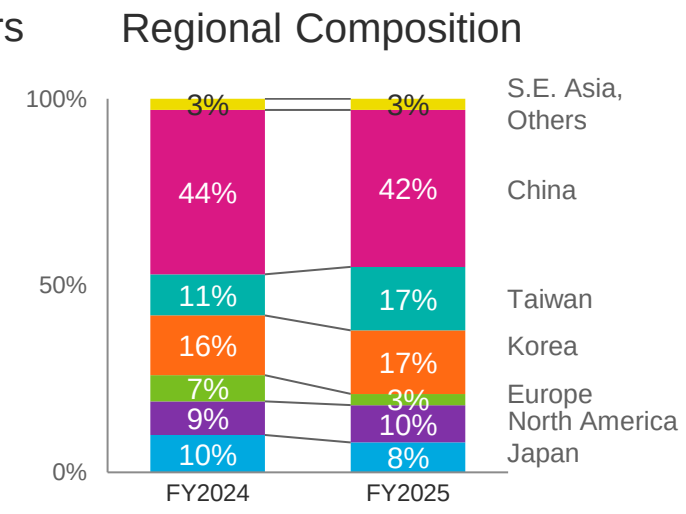












Financial Summary (Quarterly)

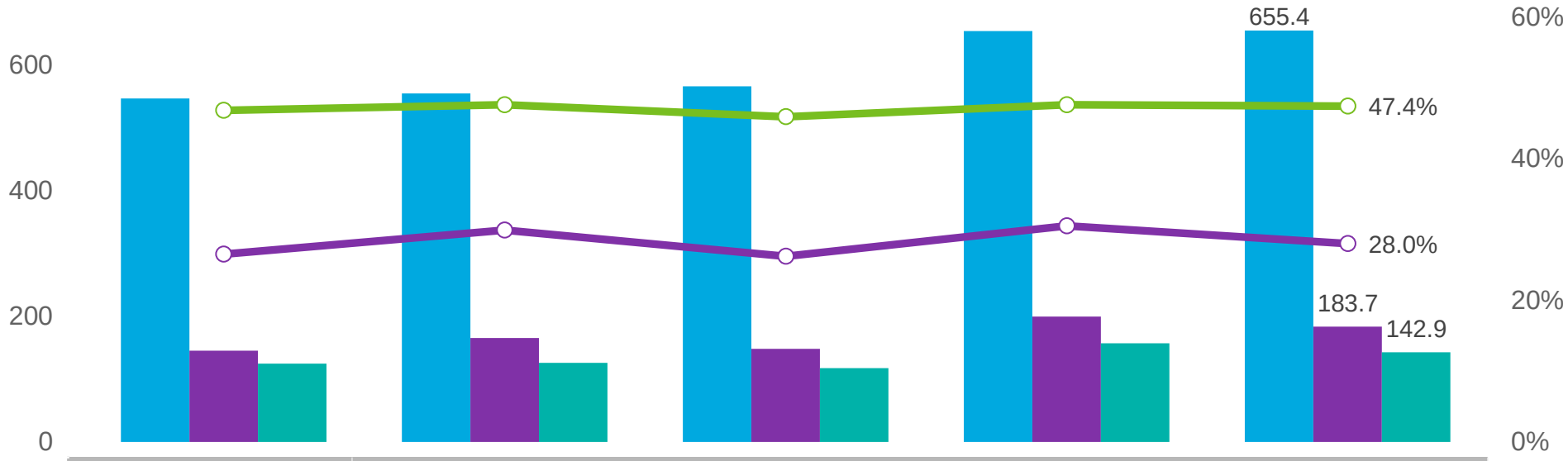
(Billion yen)

	FY2024	FY2025				vs. Q3 FY2025	vs. Q4 FY2024
	Q4	Q1	Q2	Q3	Q4		
Net sales	547.2	555.0	566.5	654.5	**655.4**	+0.1%	+19.8%
Gross profit	256.1	264.0	259.9	311.7	**310.5**	-0.4%	+21.3%
Gross profit margin	46.8%	47.6%	45.9%	47.6%	**47.4%**	-0.2pts	+0.6pts
SG&A expenses	110.8	98.2	111.7	112.1	**126.7**	+13.1%	+14.3%
Operating income	145.2	165.7	148.1	199.6	**183.7**	-7.9%	+26.6%
Operating margin	26.5%	29.9%	26.2%	30.5%	**28.0%**	-2.5pts	+1.5pts
Income before income taxes	157.8	167.2	153.6	200.1	**185.1**	-7.5%	+17.3%
Net income attributable to owners of parent	124.9	126.1	117.7	157.2	**142.9**	-9.1%	+14.4%
R&D expenses	58.4	53.4	62.0	61.8	**72.7**	+17.7%	+24.5%
Capital expenditures	32.9	23.9	53.3	50.2	**34.6**	-31.1%	+4.9%
Depreciation and amortization	15.3	13.2	14.5	16.0	**18.3**	+14.4%	+19.7%

1. In principle, export sales of Tokyo Electron's products is denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of foreign exchange rate fluctuations on profits is negligible, unless extreme fluctuations occur.
2. Profit ratios are calculated using full amounts, before rounding.

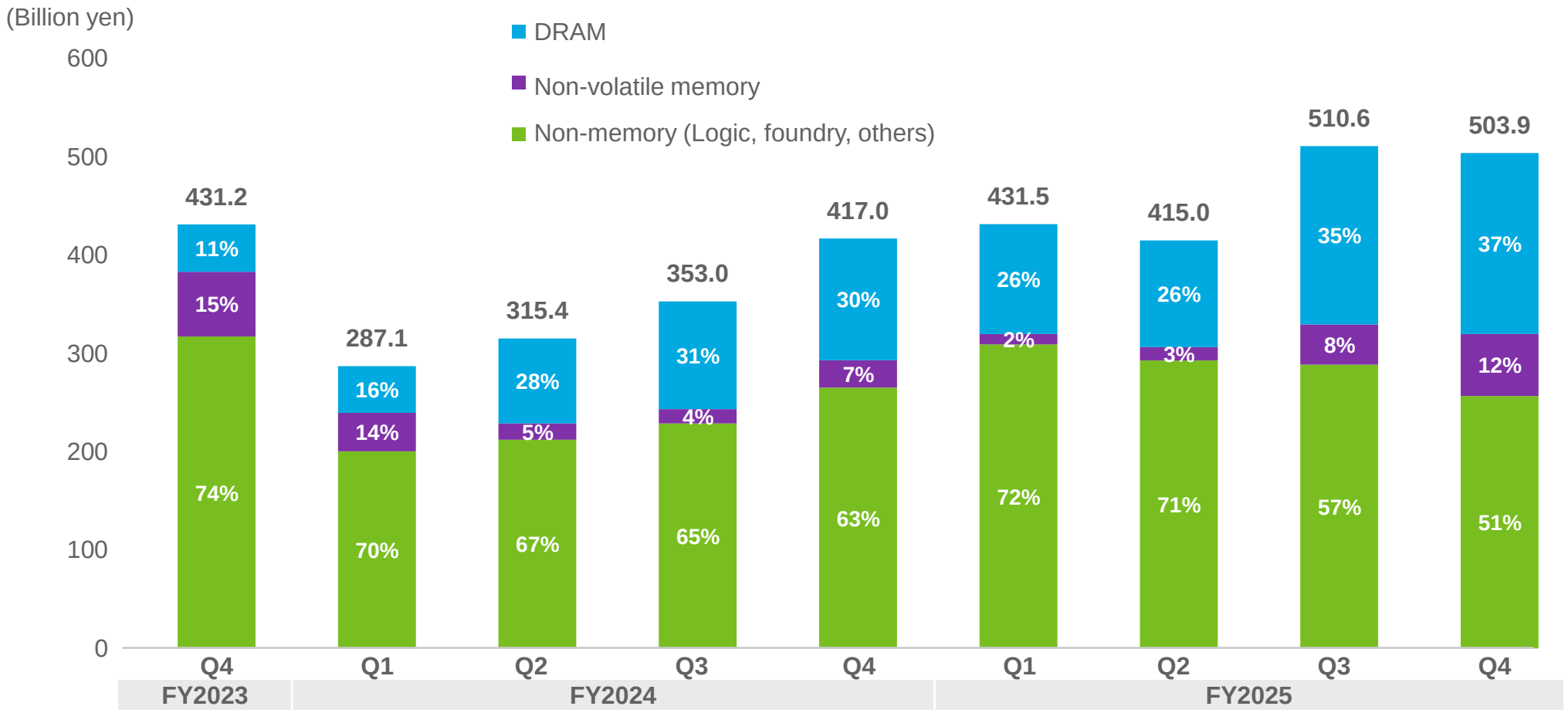
Financial Performance (Quarterly)

(Billion Yen)



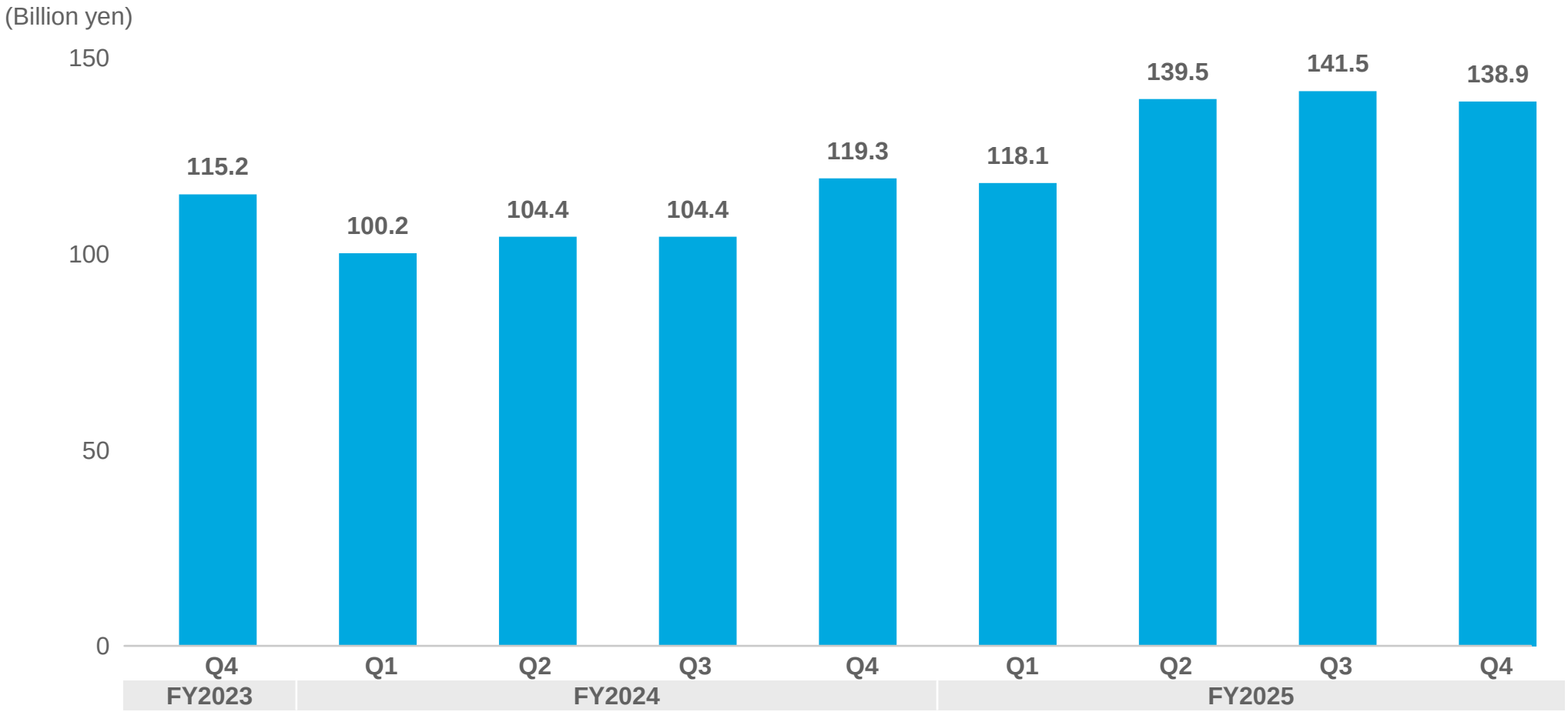
	FY2024	FY2025			
	Q4	Q1	Q2	Q4	Q4
Net sales	547.2	555.0	566.5	**654.5**	**655.4**
Operating income	145.2	165.7	148.1	**199.6**	**183.7**
Net income attributable to owners of parent	124.9	126.1	117.7	**157.2**	**142.9**
Gross profit margin	46.8%	47.6%	45.9%	**47.6%**	**47.4%**
Operating margin	26.5%	29.9%	26.2%	**30.5%**	**28.0%**

SPE New Equipment Sales by Application (Quarterly)

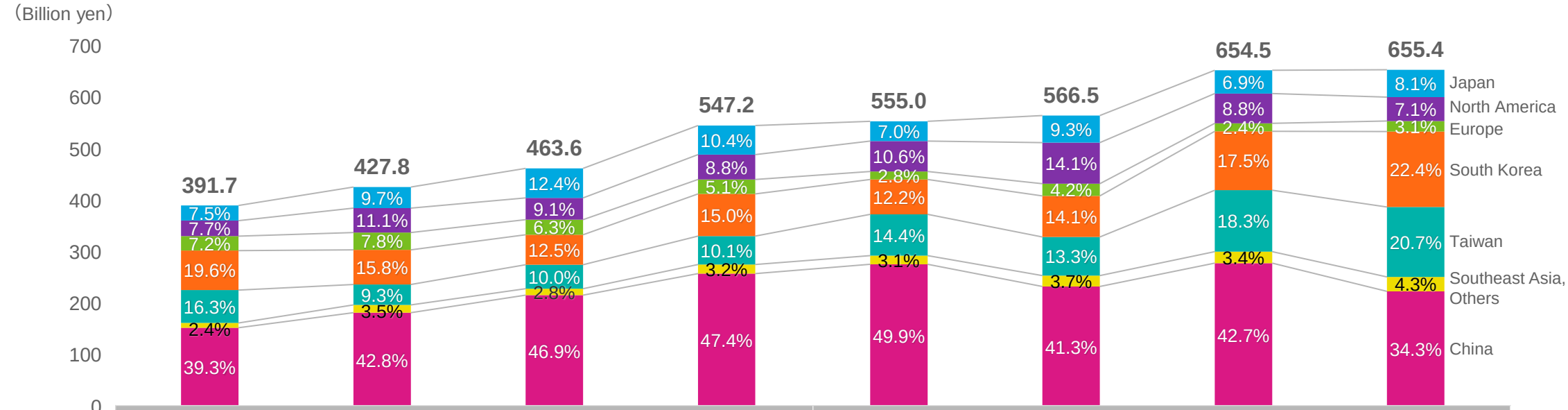


1. SPE: Semiconductor Production Equipment
2. Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

Field Solutions Sales (Quarterly)



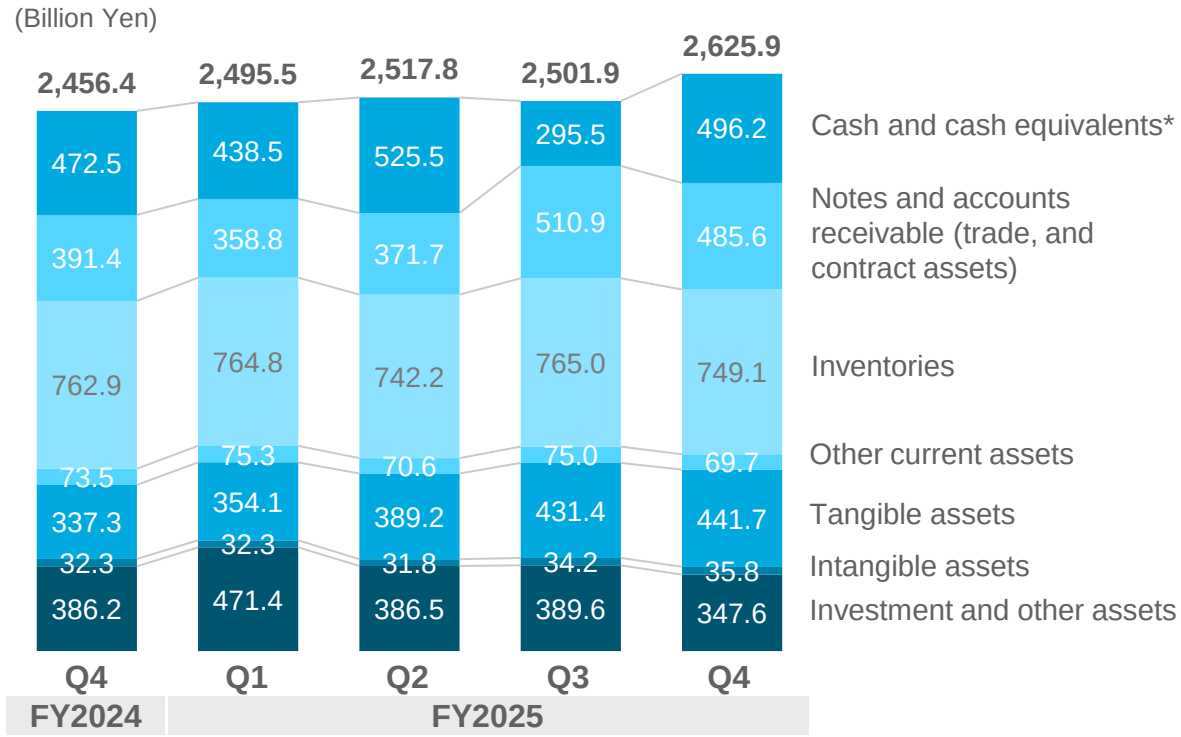
Composition of Net Sales by Region (Q1 FY2024 - Q4 FY2025)



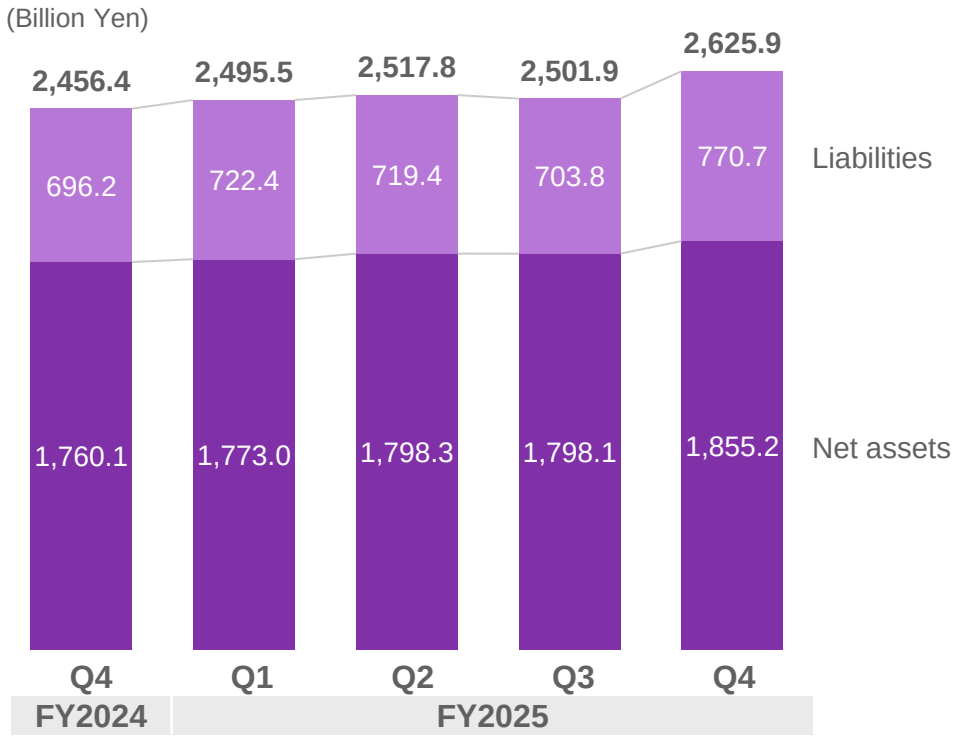
	FY2024				FY2025			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Japan	29.5	41.2	57.4	56.7	38.5	52.6	45.3	**53.4**
North America	30.1	47.4	42.1	48.3	59.0	79.9	57.7	**46.2**
Europe	28.1	33.5	29.4	28.1	15.5	23.8	15.7	**20.3**
South Korea	76.7	67.4	58.2	82.0	67.8	79.5	114.5	**147.0**
Taiwan	63.9	39.9	46.3	55.2	80.0	75.3	119.3	**135.8**
Southeast Asia, Others	9.2	15.1	12.7	17.5	17.0	21.2	22.3	**27.8**
China	153.9	182.9	217.2	259.1	277.0	233.9	279.4	**224.6**

Balance Sheet (Quarterly)

Assets

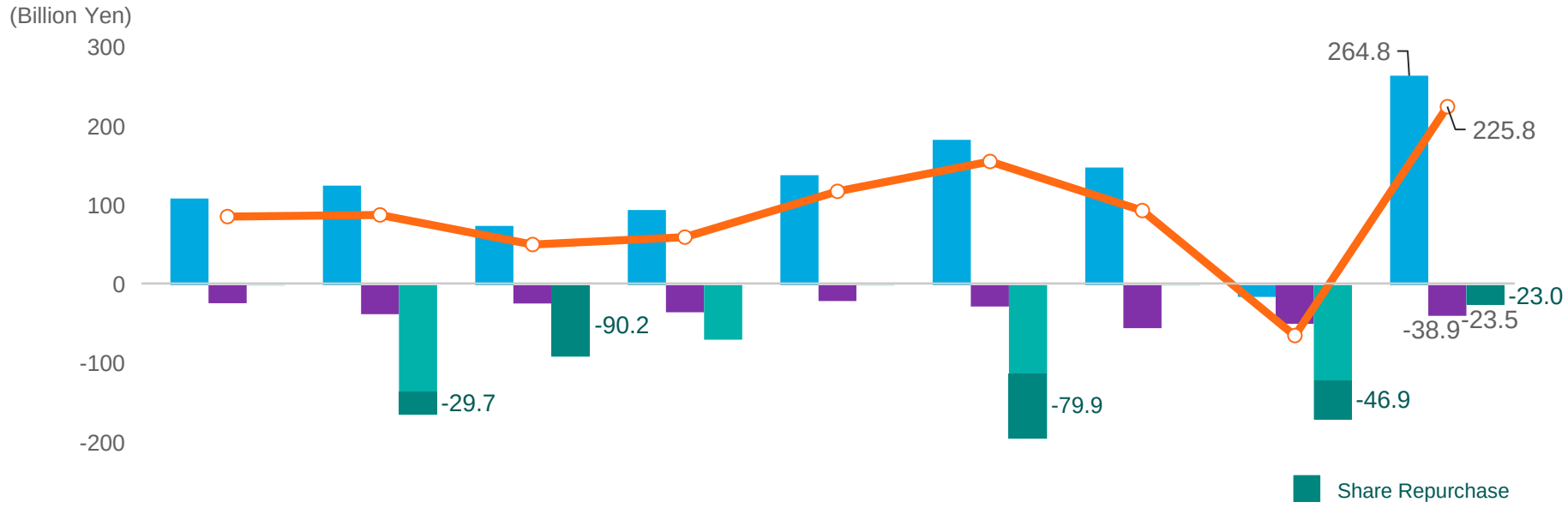


Liabilities and Net Assets



*Cash and cash equivalents: “Cash and deposits” + “Short-term investments”, etc. (“Securities” in Balance Sheet).

Cash Flow (Quarterly)



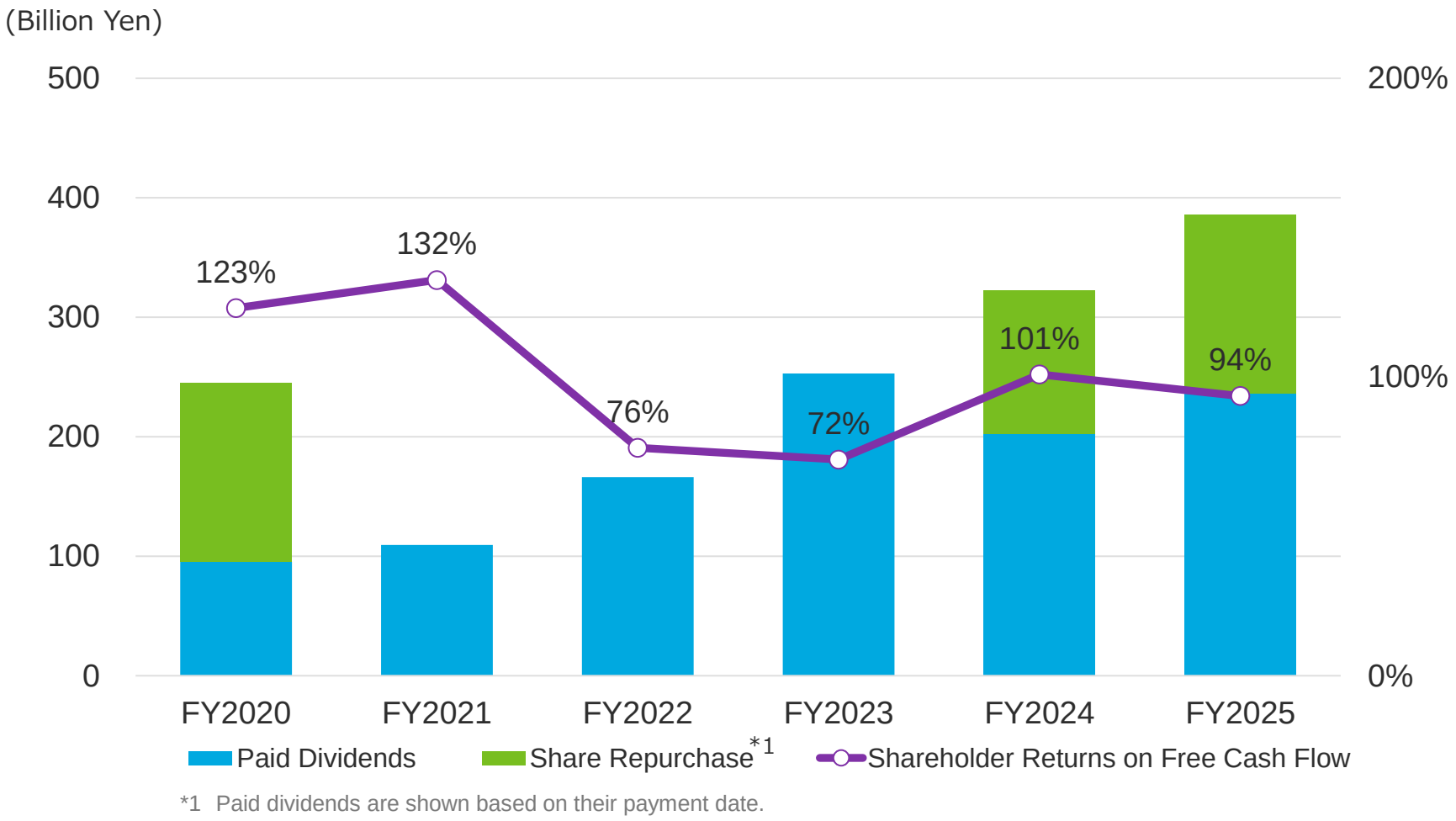
	FY2023	FY2024				FY2025			
	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Cash flow from operating activities	109.6	125.7	74.8	95.0	139.0	183.7	148.6	**-15.0**	**264.8**
Cash flow from investing activities*1	-23.1	-36.8	-23.4	-34.4	-20.3	-27.3	-54.4	**-49.0**	**-38.9**
Cash flow from financing activities	-0.5	-164.1	-90.8	-69.3	-0.6	-194.4	-0.6	**-170.1**	**-23.5**
Free cash flow*2	86.5	88.8	51.4	60.6	118.7	156.4	94.1	**-64.1**	**225.8**
Cash on hand*3	473.1	401.0	362.6	352.4	472.5	438.5	525.5	**295.5**	**496.2**

*1 Cash flow from investing activities excludes changes in time deposits and short-term investments.

*2 Free cash flow = “Cash flow from operating activities” + “Cash flow from investing activities” (excluding changes in “Time deposits” and “Short-term investments”).

*3 Cash on hand includes “Cash and cash equivalents” + “Time deposits and short-term investments” with original maturities of more than three months.

Shareholder Returns Trend



*1 Paid dividends are shown based on their payment date.

Aim for continuous high level of cash generation and shareholder returns

Consolidated 10-year Financial Summary

(Millions of yen)

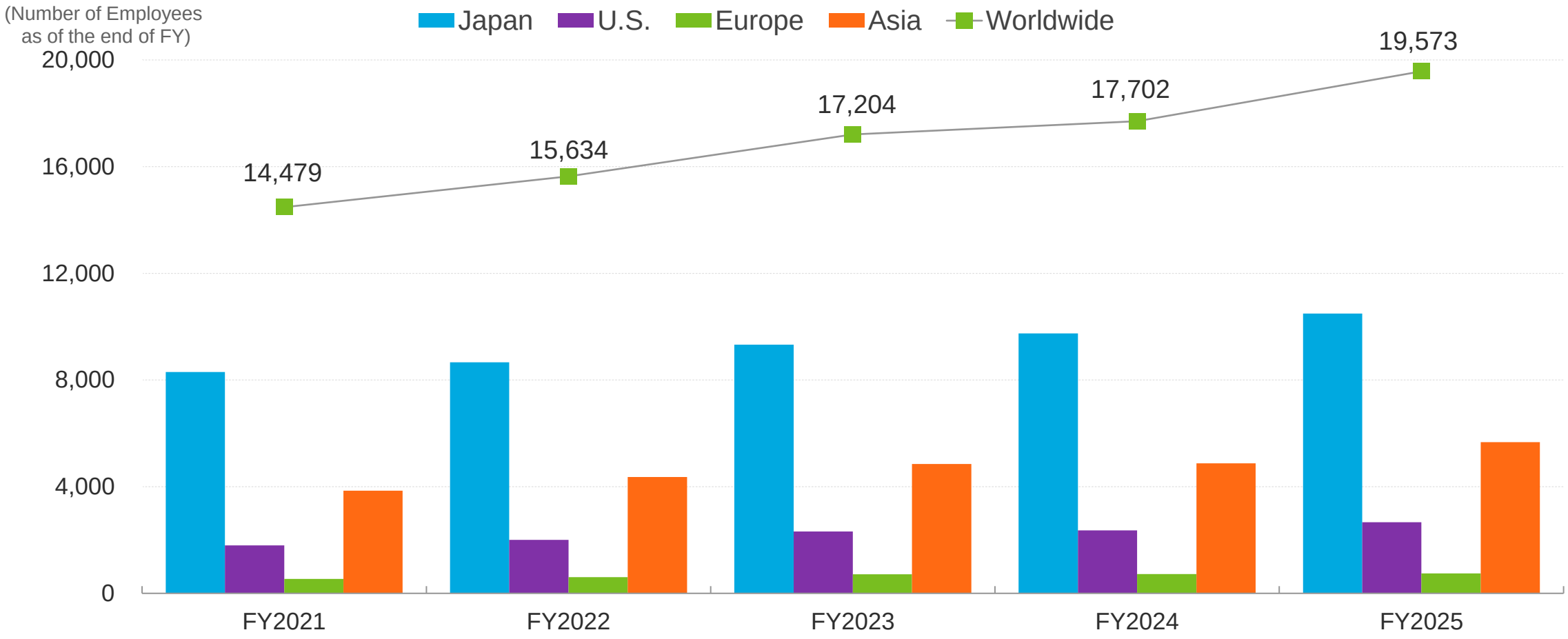
	FY2016	FY2017	FY2018	FY2019	FY2020	FY2021	FY2022	FY2023	FY2024	FY2025
Net sales	663,949	799,719	1,130,728	1,278,240	1,127,286	1,399,102	2,003,805	2,209,025	1,830,527	2,431,568
Gross profit	267,209	322,291	475,032	526,183	451,941	564,945	911,822	984,408	830,269	1,146,287
Gross profit margin	40.2%	40.3%	42.0%	41.2%	40.1%	40.4%	45.5%	44.6%	45.4%	47.1%
SG&A expenses	150,420	166,594	193,860	215,612	214,649	244,259	312,551	366,684	374,006	448,967
Operating income	116,789	155,697	281,172	310,571	237,292	320,685	599,271	617,723	456,263	697,319
Operating margin	17.6%	19.5%	24.9%	24.3%	21.0%	22.9%	29.9%	28.0%	24.9%	28.7%
Ordinary income	119,399	157,549	280,737	321,662	244,979	322,103	601,724	625,185	463,185	707,727
Income before income taxes	106,467	149,116	275,242	321,508	244,626	317,038	596,698	624,856	473,439	706,114
Net income attributable to oweners of parent	77,892	115,208	204,371	248,228	185,206	242,941	437,076	471,584	363,963	544,133
R&D expenses	76,287	83,800	97,103	113,980	120,268	136,648	158,256	191,196	202,873	250,017
Capital expenditures	13,341	20,697	45,603	49,754	54,666	53,868	57,288	74,432	121,841	162,171
Depreciation and amortization	19,257	17,872	20,619	24,323	29,107	33,843	36,727	42,927	52,339	62,148
Interest-bearing debt	-	-	-	-	-	-	-	-	-	-
Equity	562,369	643,094	767,146	880,748	819,301	1,012,977	1,335,152	1,587,595	1,746,835	1,839,929
Total assets	793,367	957,447	1,202,796	1,257,627	1,278,495	1,425,364	1,894,457	2,311,594	2,456,462	2,625,981
Debt-to-equity ratio	-	-	-	-	-	-	-	-	-	-
Equity ratio	70.9%	67.2%	63.8%	70.0%	64.1%	71.1%	70.5%	68.7%	71.1%	70.1%
ROE	13.0%	19.1%	29.0%	30.1%	21.8%	26.5%	37.2%	32.3%	21.8%	30.3%
Cash flow from operating activities	69,398	136,948	186,582	189,572	253,117	145,888	283,387	426,270	434,720	582,174
Cash flow from investing activities	-150,013	-28,893	-11,833	-84,033	15,951	-18,274	-55,632	-41,756	-125,148	-169,609
Cash flow from financing activities	-138,600	-39,380	-82,549	-129,761	-250,374	-114,525	-167,256	-256,534	-325,012	-388,836
Net income per share (Yen)	153.70	234.09	415.16	504.53	390.19	520.73	935.95	1,007.82	783.75	1,182.40
Cash dividends per share (Yen)	79.00	117.00	208.00	253.00	196.00	260.00	468.00	570.00	393.00	592.00
Number of employees	10,629	11,241	11,946	12,742	13,837	14,479	15,634	17,204	17,702	19,573

1: From FY2019, the Company adopts “Partial Amendments to Accounting Standard for Tax Effect Accounting” (ASBJ Statement No. 28, revision on February 16, 2018). “Total assets” and "equity ratio" for FY2018 have been restated in the table in accordance with the revised accounting standard.

2: From the beginning of FY2022, the Company applies “Accounting Standard for Revenue Recognition” (ASBJ Statement No. 29).

3:The Company implemented a 3-for-1 common stock split on April 1, 2023. Net income per share and dividend per share (yen) are the figures after the stock split.

Worldwide Employees



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- Processing of numbers
  For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.

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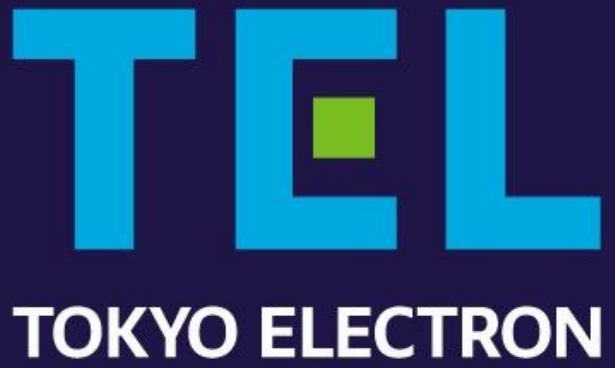
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