Tokyo Electron Corporate Update

February 15, 2024

Contents

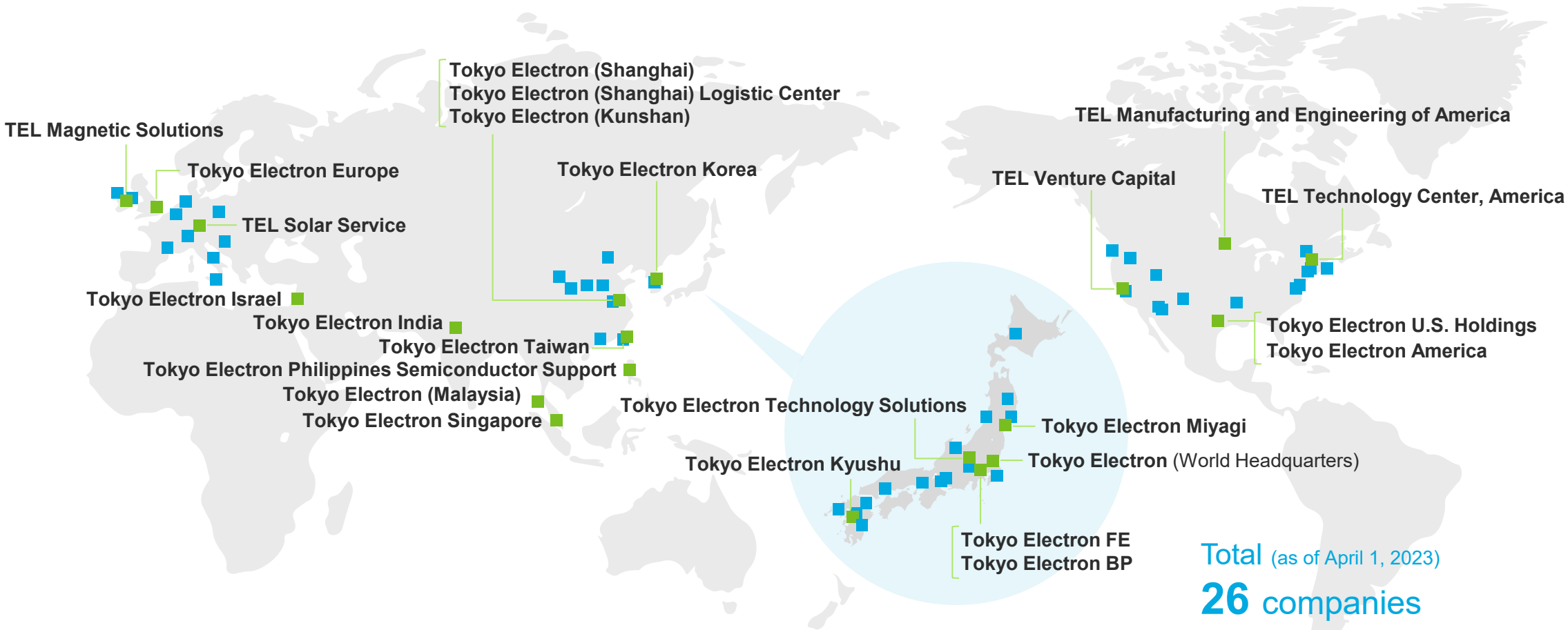
1. TEL Overview

Company Profile

Established	November 11, 1963
Major Products and Services	Semiconductor Production Equipment
Capital	54.9 Billion Yen
Sales/Profit	Net sales 2,209.0 Billion Yen / Operating income 617.7 Billion Yen / Operating margin 28.0% (Fiscal 2023)
Number of Employees	2,021 (non-consolidated) 17,522 (consolidated)
Global Network	Japan: 6 companies / 27 locations Overseas: 20 companies / 17 countries and regions / 56 locations Total: 26 companies / 18 countries and regions / 83 locations (consolidated) (as of April 1, 2023)

Worldwide Operations

(As of Nov. 14, 2023)



Total (as of April 1, 2023)

26 companies

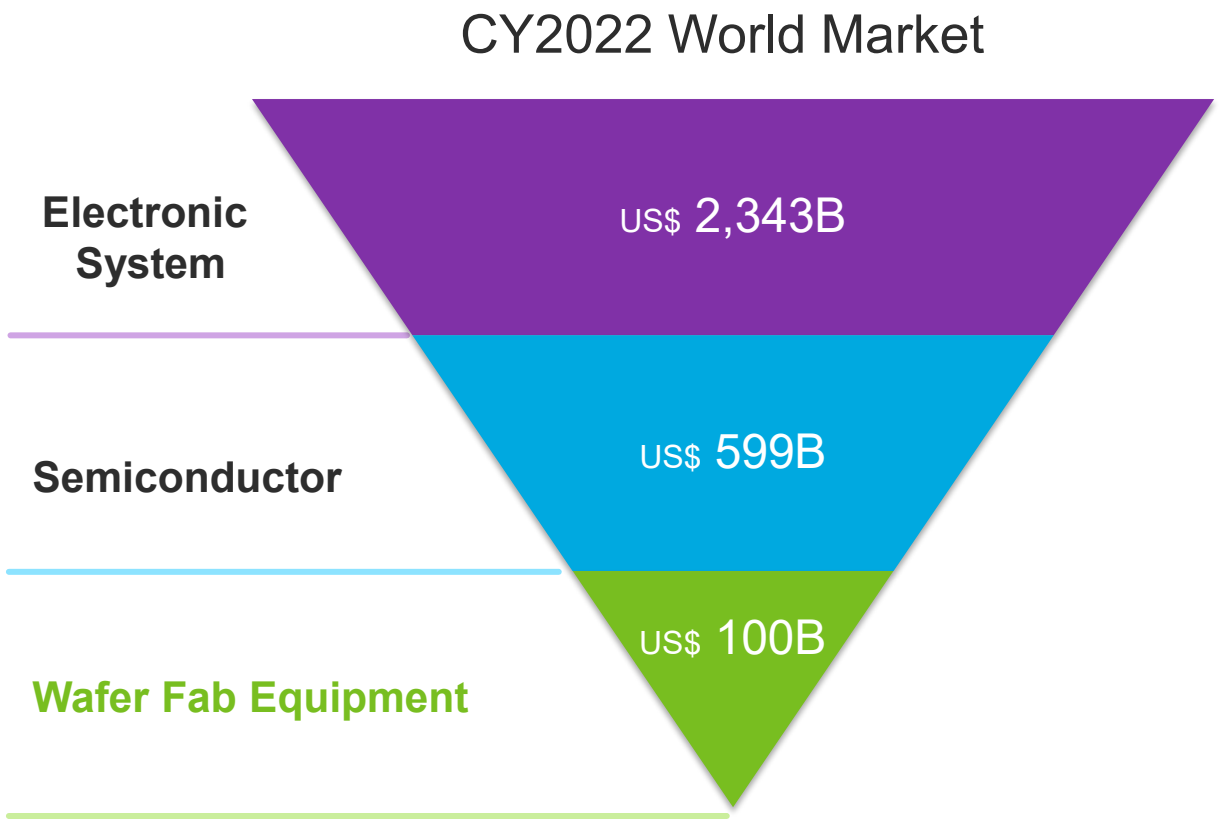
18 countries and regions

83 locations

- Head Office
- Branch, Office (including Field Service), Sales Office

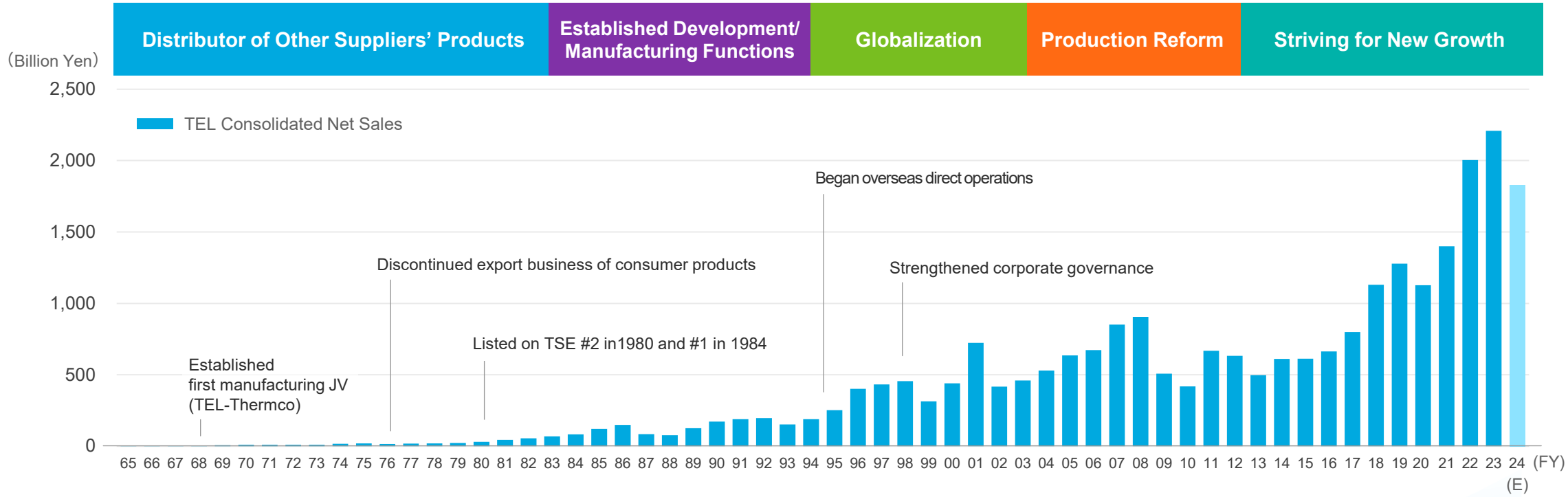
*Group companies in the process of being wound up are not shown on the map.

The Market TEL Participates in



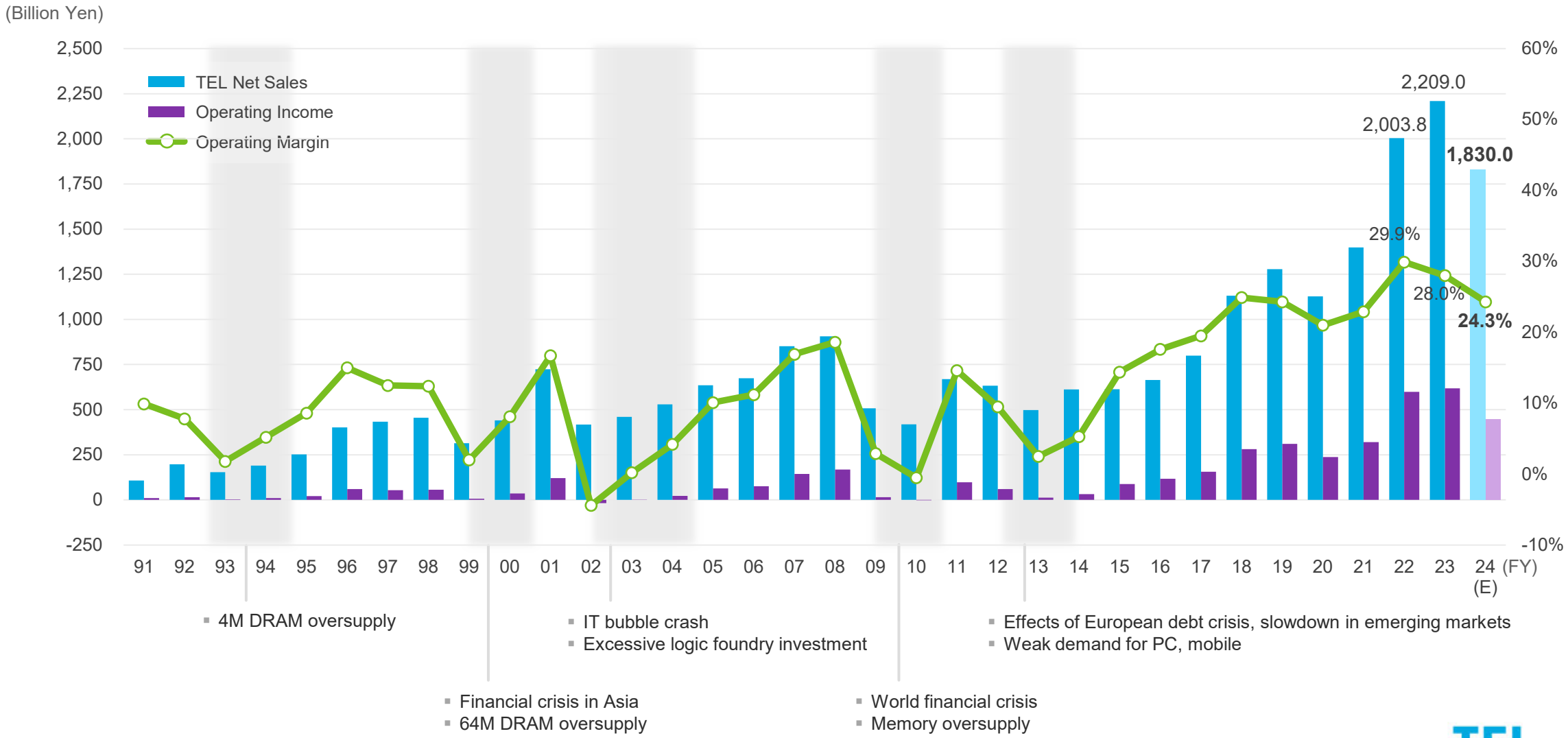
Source: Gartner®, "Forecast: Semiconductor Capital Spending, Wafer Fab Equipment and Capacity, Worldwide, 4Q23 Update", Bob Johnson, Gaurav Gupta, 22 December 2023
Charts/graphics created by Tokyo Electron based on Gartner research.
Electronic System＝Electronic Equipment Production/Semiconductor＝Semiconductor Revenue /Wafer Fab Equipment ＝Total Wafer Fab Equipment Revenue Basis.

TEL is Innovative and Flexible to Market Change

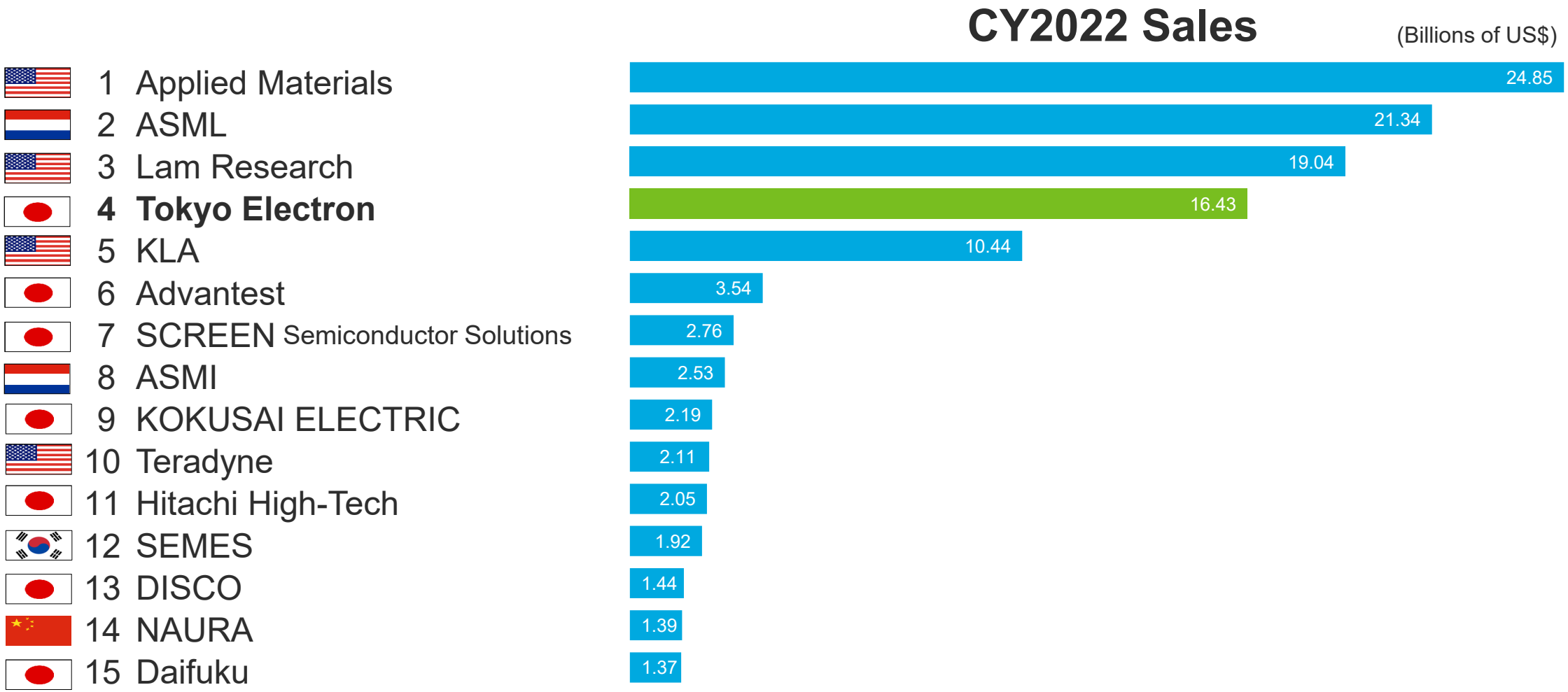


*The diagram is an image of the expanding use of semiconductors and does not indicate the actual number of semiconductors used.

Financial Performance: Sales and Operating Margin



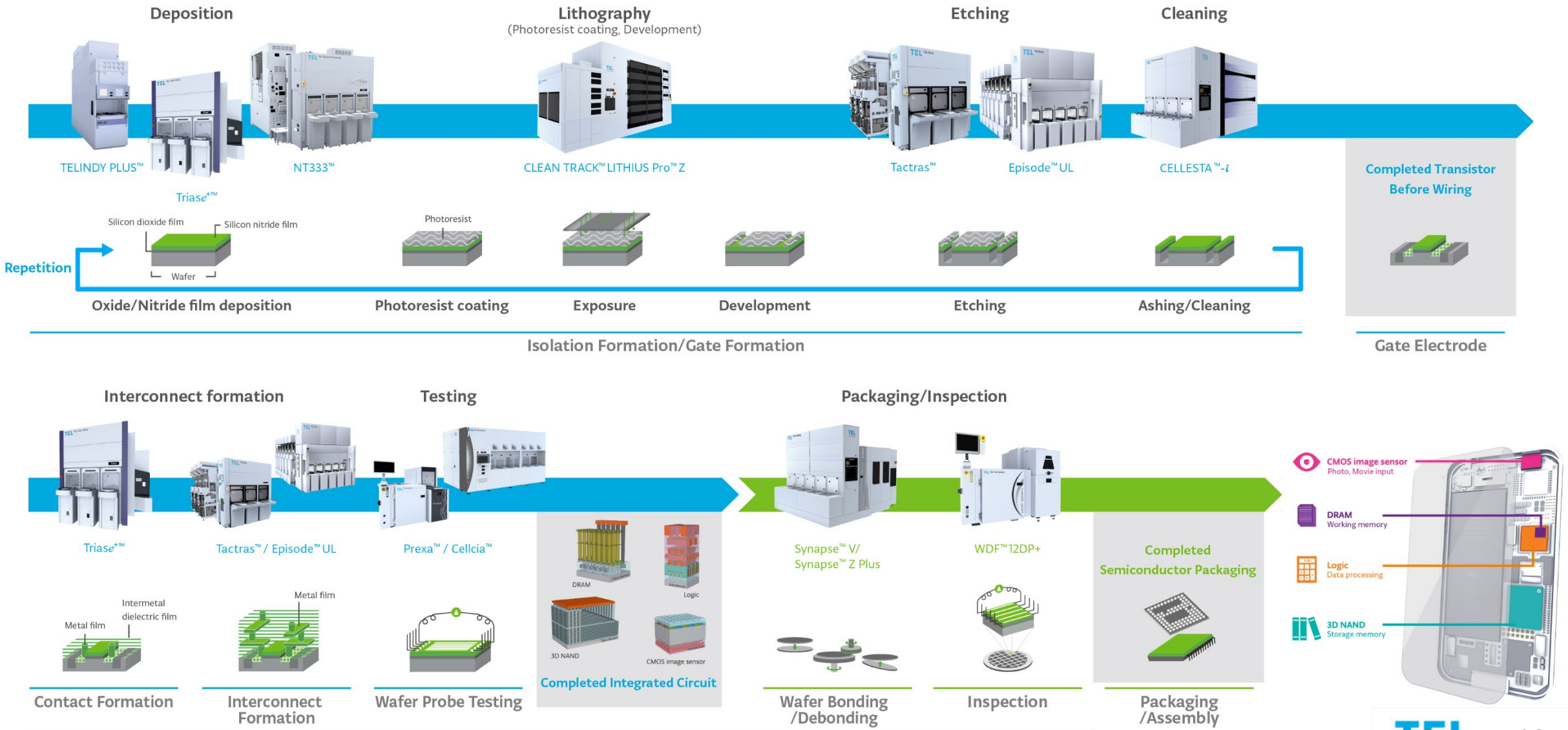
CY2022 SPE Makers Top 15



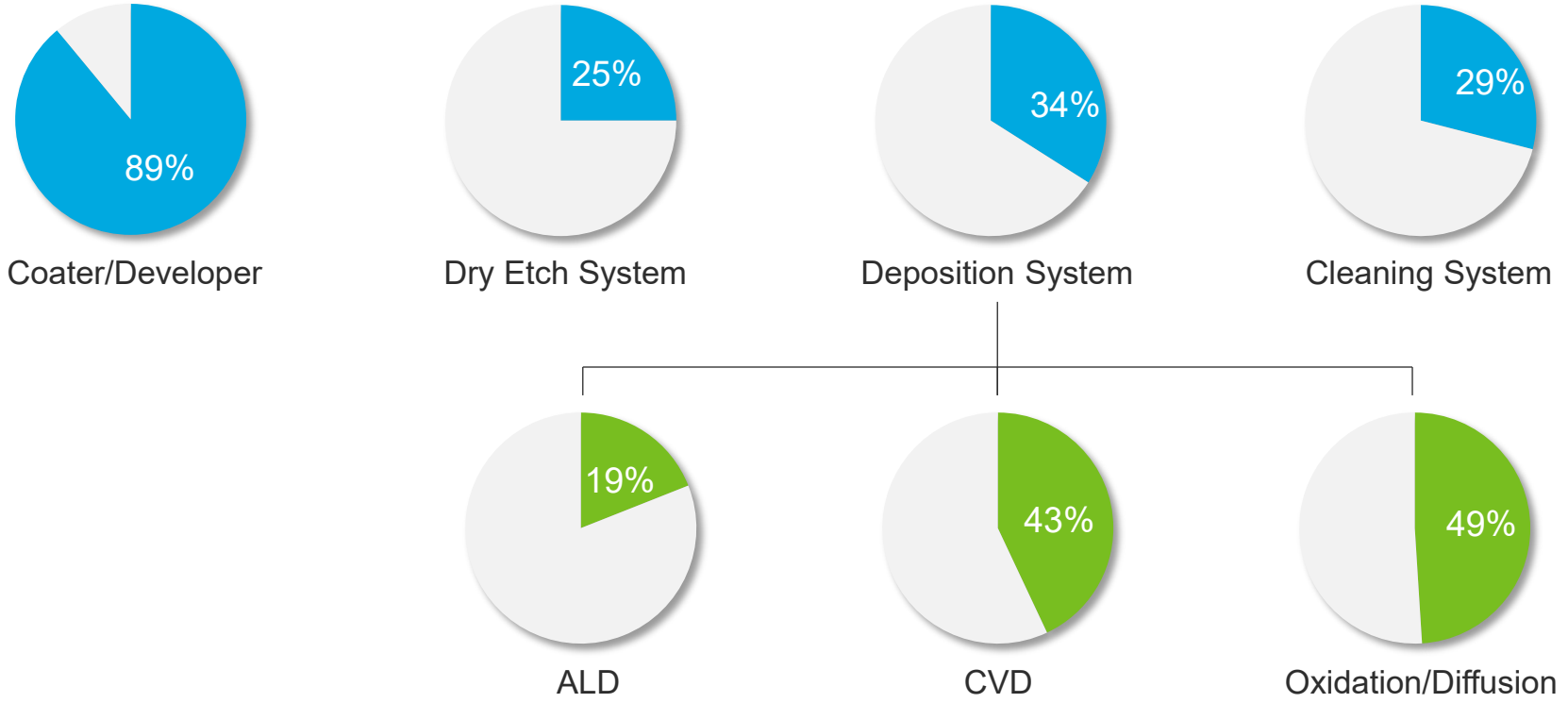
Source：TechInsights Manufacturing Analysis Inc., May 2023

Semiconductor Manufacturing Process

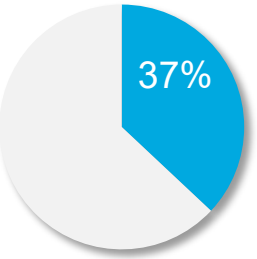
Wafer Process (Front-end)
Assembly and Test process (Back-end)



World Market Share of TEL's Main SPE* Products (CY2022)



Source
SPE (excluding Wafer Prober) : Gartner®, "Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2022", Bob Johnson, Gaurav Gupta, Menglin Cao, 17 April 2023
Graph/chart created by TEL based on Gartner research. Gartner research. Calculations performed by TEL.
Coater/Developer: Photoresist Processing (Track), Dry Etch System: Dry Etch, Deposition System: Tube CVD + Atomic Layer Deposition Tools + Oxidation/Diffusion Furnaces + Nontube LPCVD, ALD: Atomic Layer Deposition Tools, CVD: Tube CVD + Nontube LPCVD, Oxidation/Diffusion: Oxidation/diffusion Furnaces, Cleaning System: Single Wafer Processors + Wet Stations + Batch Spray Processors + Scrubbers + Other Clean Equipment



Source
SPE (Wafer Prober) :
TechInsights Manufacturing Analysis Inc., April 2023
Charts/graphics created by Tokyo Electron based on :
TechInsights Manufacturing Analysis Inc.

* SPE: Semiconductor production equipment

TEL's Strengths

Only One

Have products in 4 sequential processes

Deposition | Coater/ Developer | Etch | Cleaning

No.1/No.2

Products with the world's No. 1 or No.2 market share

Major Products & Market Position*

#1	#2	#2	#1	#1	#1	#2	#2
Coater/ Developer	Cleaning	Plasma Etch	Gas Chemical Etch	Diffusion Furnace	Batch Deposition	Metal Deposition	Prober

*TEL estimate

100%

Market share of coater/developer for EUVL

Coater/ Developer | EUV Lithography

No.1

Worldwide installed base

Annual increase by about 6,000 units*1

Industry's largest installed base 91,000 units*2

*1 As of Mar. 2023
*2 As of Dec. 2023

R&D Map

(As of Nov. 14, 2023)

TEL Magnetic Solutions (Ireland)

imec (Belgium)

CEA-Leti (France)

TEL Technology Center Korea (Korea)

TEL Technology Center, Taiwan (Taiwan)

IME (Singapore)

TEL Digital Design Square
Tokyo Electron Technology Solutions
Tokyo Electron Miyagi
Tokyo Electron Kyushu
(Japan)

National Institute of Advanced Industrial Science and Technology
(Japan)

TEL Manufacturing and Engineering of America (U.S.)

TEL Technology Center, America (U.S.)

SUNY Poly/NY CREATES (U.S.)

BRIDG (U.S.)

Tokyo Electron America (U.S.)

TEL R&D base
Consortium

Strengthen R&D Capabilities

Yamanashi R&D building

Deposition system, gas chemical etch system, corporate R&D
(Established in July 2023)

Miyagi R&D building

Etch system
(Completion scheduled for spring 2025)

Kumamoto R&D building

Coater/Developers, surface preparation system
(Completion scheduled for summer 2025)

Miyagi Technology Innovation Center

Etch system
(Began operation in Oct. 2021)

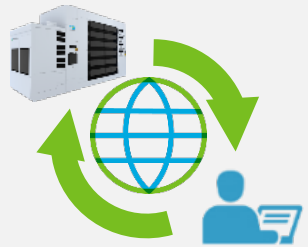
TEL Digital Design Square

DX, Software
(Began operation in Nov. 2020)

Continually Pursuing the Best Products and Best Service

Front-loading

Advanced field solutions



- Share roadmap for next several generations with customers
- Promote early engagement
- Realize maximum yield of customer devices and equipment availability from early stage of customers' mass production and reduce burden on the environment
- Further increase investment in human resources/R&D by raising operational efficiency and driving higher per-employee productivity

- Business development leveraging industry's largest installed base of 91,000 units*
- TELeMetrics™ remote maintenance
- Predictive maintenance with machine learning

* As of Dec. 2023

Maximize Utilization of TEL's Comprehensive Strengths

Sales

Customer trust

Broad product coverage

Market-ing

Advanced data collection and analysis abilities

FS

- **Largest installed base in industry: over 91,000 units***
- **Advanced FS**

* As of Dec. 2023

R&D

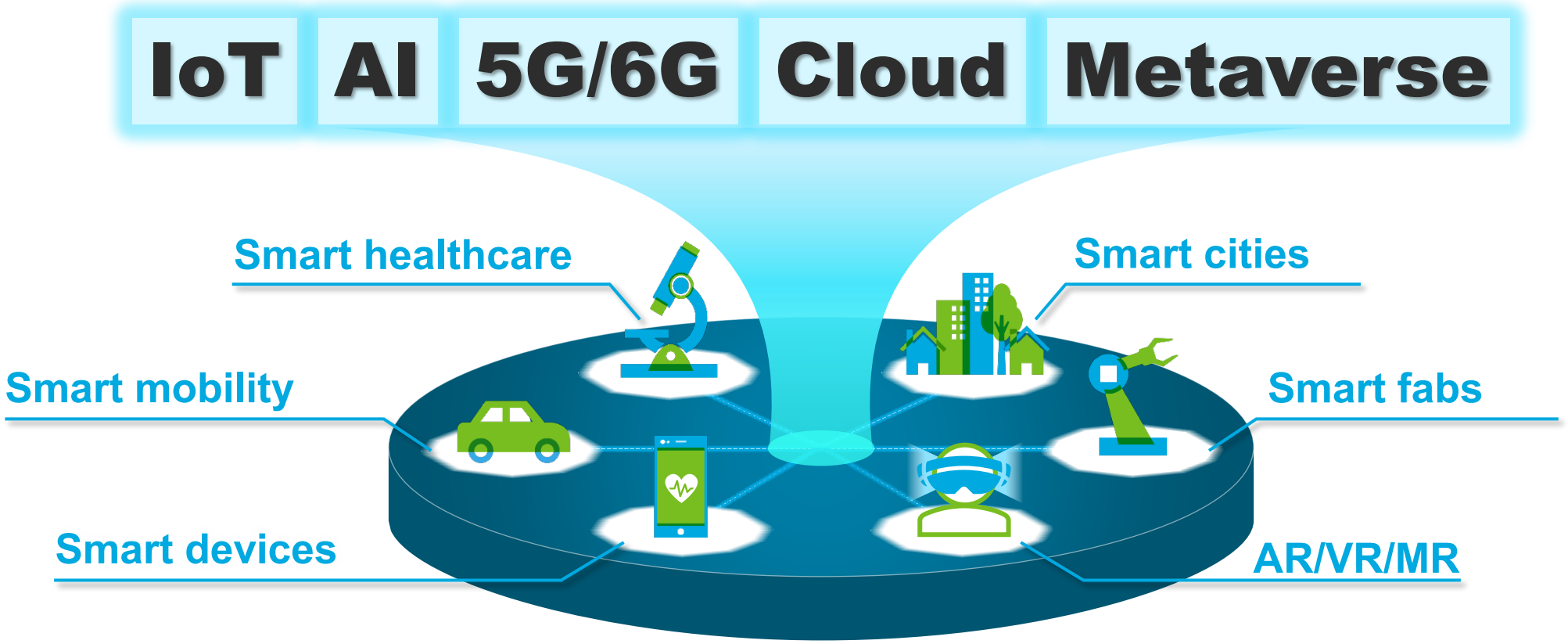
- **Strong next generation product development**
- **Process integration**

Manu-facturing

- **High quality**
- **Robust supply chain**

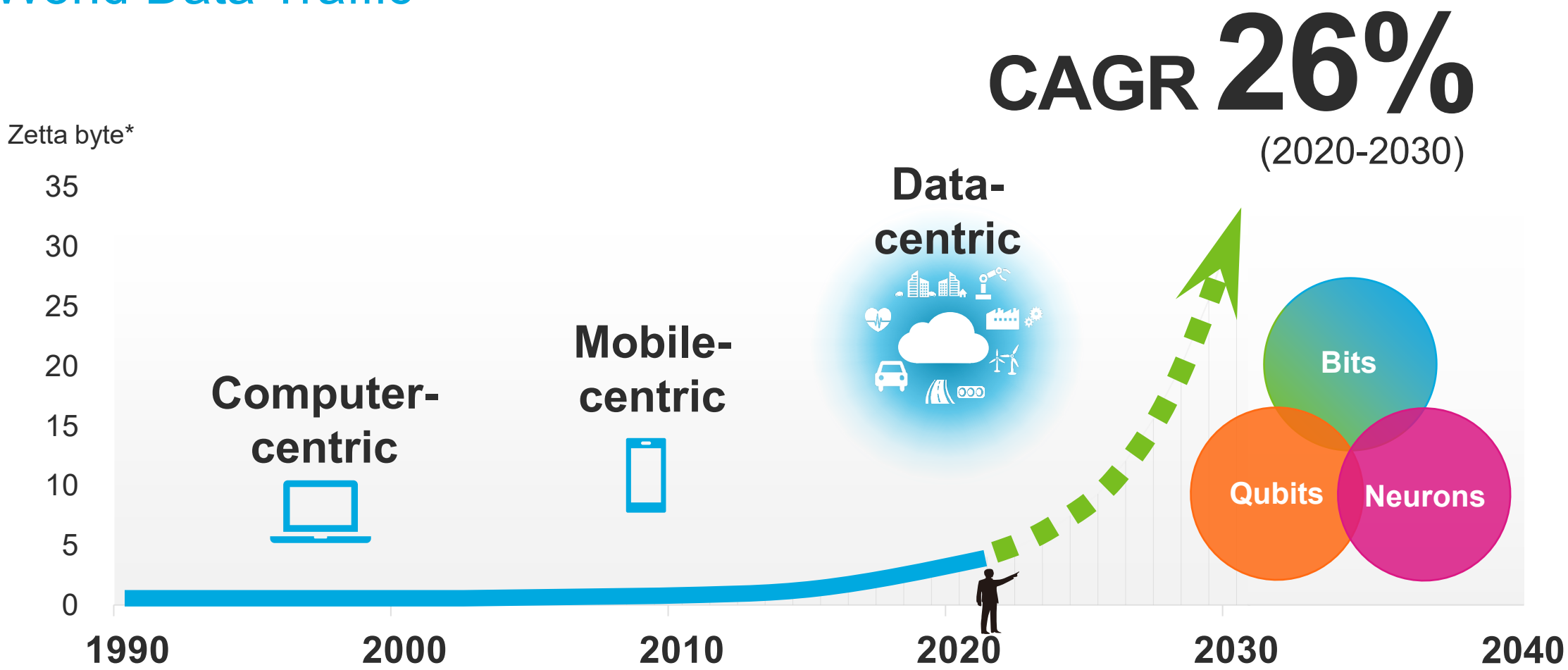
2. Semiconductor and SPE Market Outlook

Spread of IoT・AI・5G and Accelerating the Digital Shift



The world is currently pushing firmly ahead with implementing ICT and DX as well as taking action to realize a carbon-free society in order to build a strong and resilient society in which economic activities do not stop under any circumstances

World Data Traffic

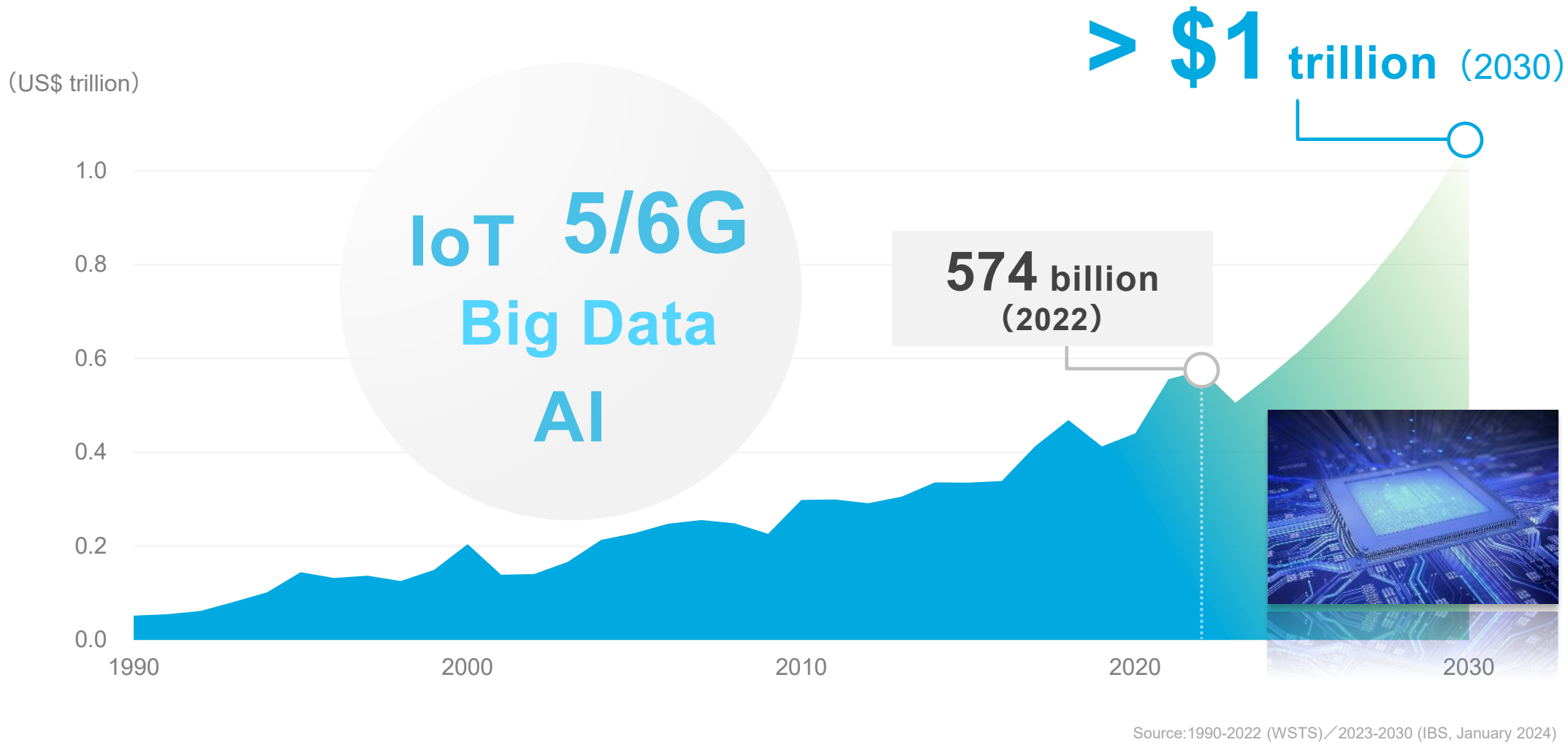


Source: Omdia

*Zettabyte: 1 Zettabyte = 10^{21}byte, 1 Zettabyte is said to be "the number of sand grains on sandy beaches around the world"

Explosive increase in data traffic

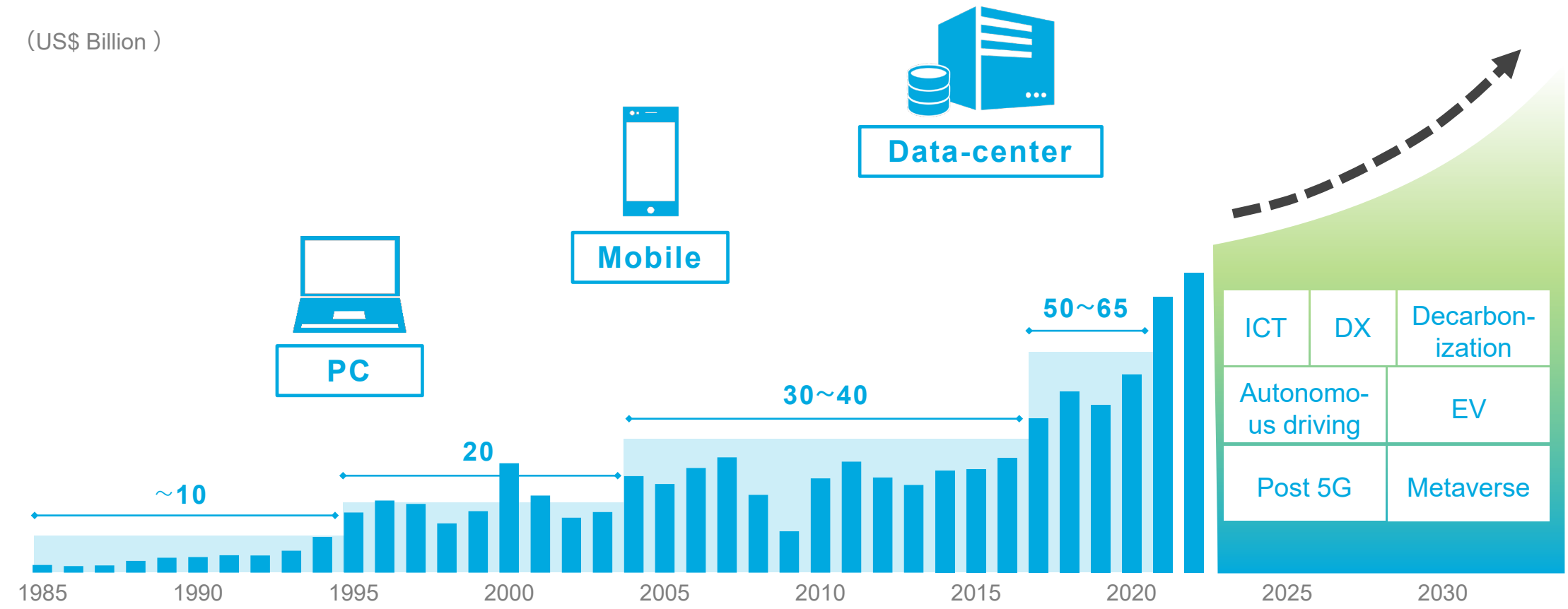
Outlook for the Semiconductor Market



Source:1990-2022 (WSTS)／2023-2030 (IBS, January 2024)

Expected to exceed US$1 trillion by 2030

WFE* Market



* WFE (Wafer fab equipment): The semiconductor production process is divided into front-end production, in which circuits are formed on wafers and inspected, and back-end production, in which wafers are cut into chips, assembled and inspected again. Wafer fab equipment refers to the production equipment used in front-end production and in wafer-level packaging production.

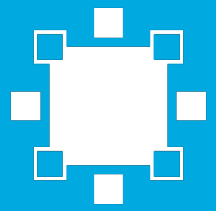
Source : TechInsights Manufacturing Analysis Inc. (VLSI) (1985~2022)

WFE Market will grow further with progress of digitalization and evolution of semiconductors

Investment for Future Growth (FY2025 to FY2029)

R&D Investment

1.5
trillion yen



Capex

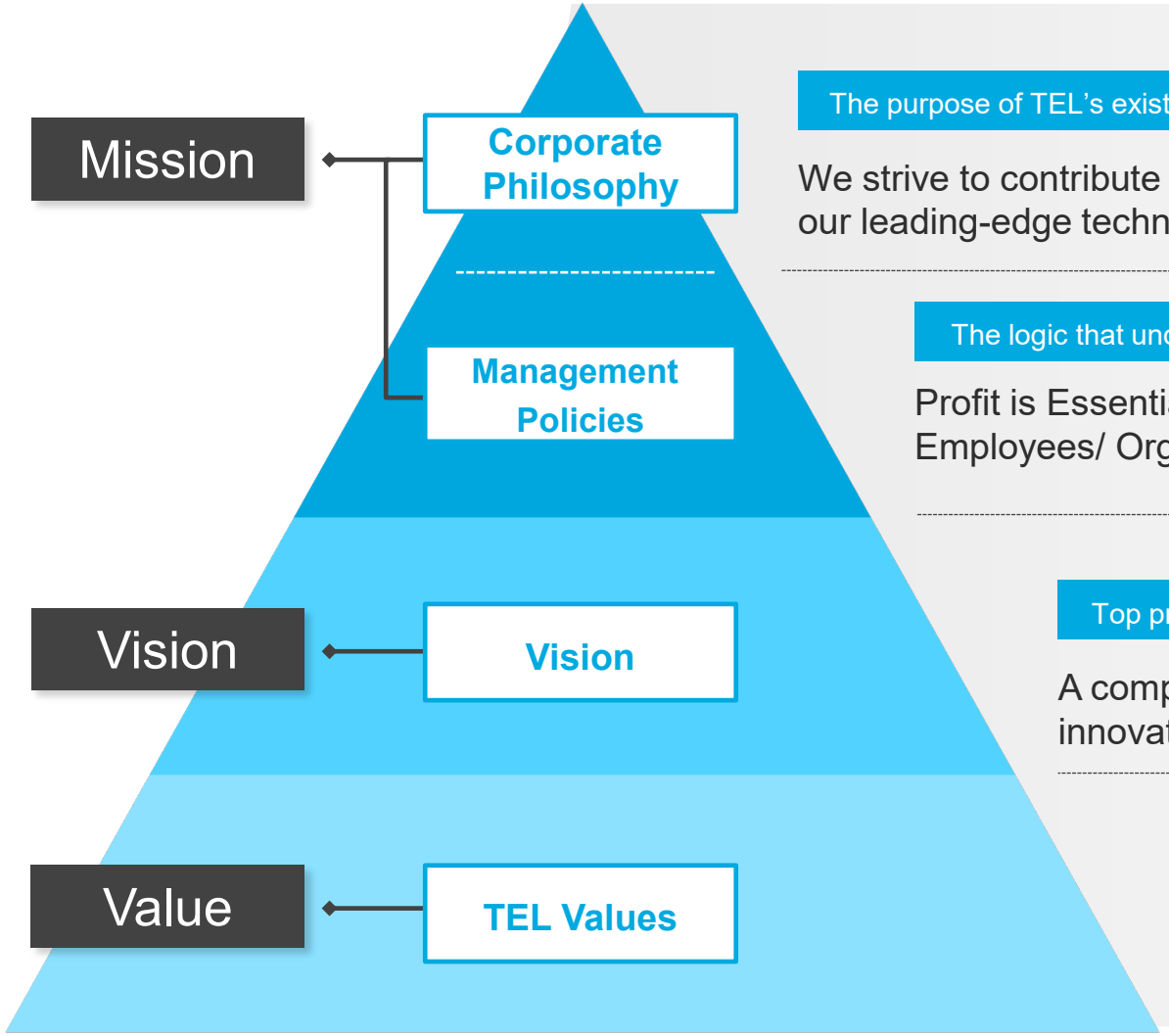
700
billion yen

Recruitment

10,000
people
2,000 people/year

3. Corporate Principles and New Medium-term Management Plan

Corporate Principles System



The purpose of TEL's existence and its mission in society

We strive to contribute to the development of a dream-inspiring society through our leading-edge technologies and reliable service and support

The logic that underscores general rules of management

Profit is Essential/Scope of Business/Growth Philosophy/Quality and Service/ Employees/ Organizations/Safety, Health, and the Environment/Social Responsibility

Top priorities to be addressed to realize the Corporate Philosophy

A company filled with dreams and vitality that contributes to technological innovation in semiconductors

Attitudes, codes of conduct, and values to be observed by each employee

Pride/Challenge/Ownership/Teamwork/Awareness

Vision

A company filled with dreams and vitality that contributes to technological innovation in semiconductors

Tokyo Electron pursues technological innovation in semiconductors that supports the sustainable development of the world.

We aim for medium- to long-term profit expansion and continuous corporate value enhancement by utilizing our expertise to continuously create high value-added leading-edge equipment and technical services.

Our corporate growth is enabled by people, and our employees both create and fulfill company values. We work to realize this vision through engagement with our stakeholders.

Technology Enabling Life

"Technology Enabling Life" is our corporate message that expresses the Corporate Principles which consist of our Corporate Philosophy, Management Policies, Vision and TEL Values.

CSV
(Creating Shared Value)

The concept is to create social and economic value by leveraging corporate expertise to solve social issues, hereby enhancing corporate value and achieving sustainable growth.

TSV
TEL's Shared Value

=

- Pursue technological innovation in semiconductors that supports the sustainable development of the world
- Continuously create high value-added leading-edge equipment and technical services
- Medium- to long-term profit expansion and continuous corporate value enhancement
- Engagement with our stakeholders

Realization of Vision = Creating Shared Value in TEL

Our Approaches to Social Issues

Sustainable development of the world / Diversification of values and happiness

Solutions

Online/Metaverse

AI diagnosis/Prevention/Robots

Smartification

EV/Autonomous driving/MaaS

Technologies

- Higher speed communication (5G/6G)
- Cloud/Edge Computing
- AI
- IoT
- AR/VR/MR

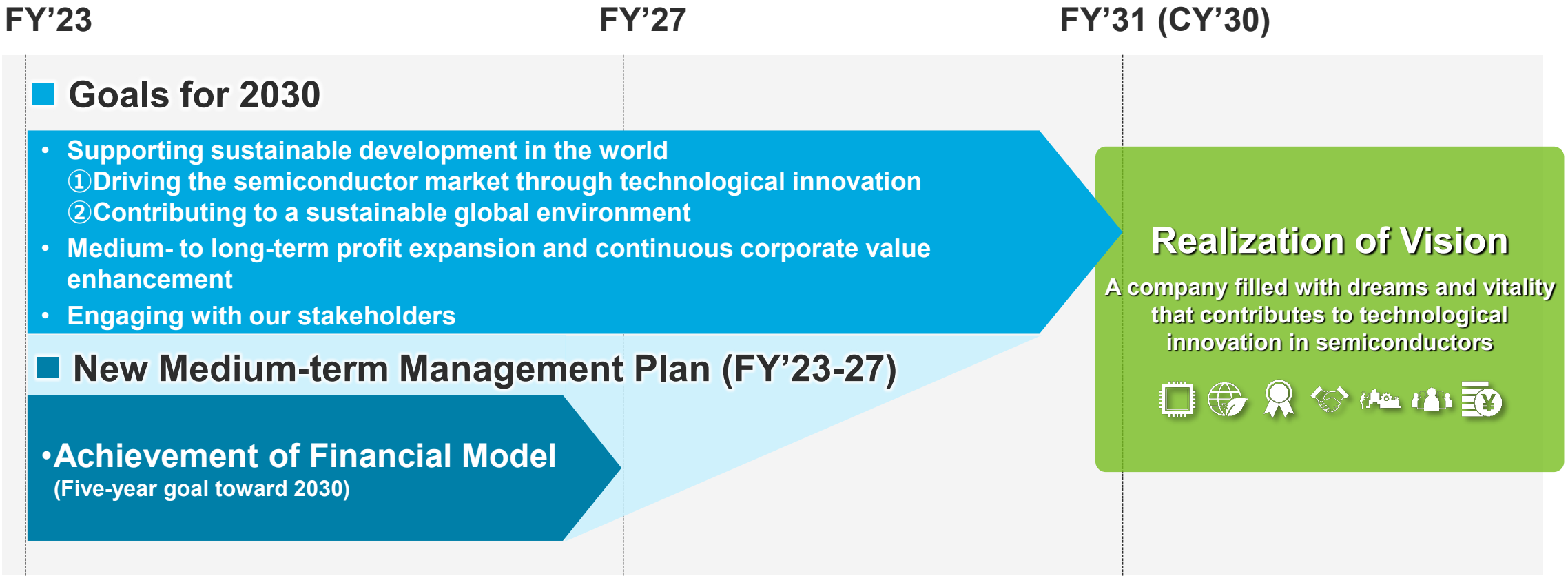
Semiconductors

- Logic
- Memory
- Power
- Analog
- Sensors
- Displays

Pursue technological innovation in semiconductors :
Larger capacity/Higher speed/Higher reliability/Lower power consumption

Higher definition/Flexible /Lower power consumption

Vision & Medium-term Management Plan



Aiming to achieve the Medium-term Management Plan
by FY'27 with a view to realizing Vision in 2030

Key Indicators for Continuous Corporate Value Enhancement

Material Issues

- **Net sales/Operating margin/ROE**

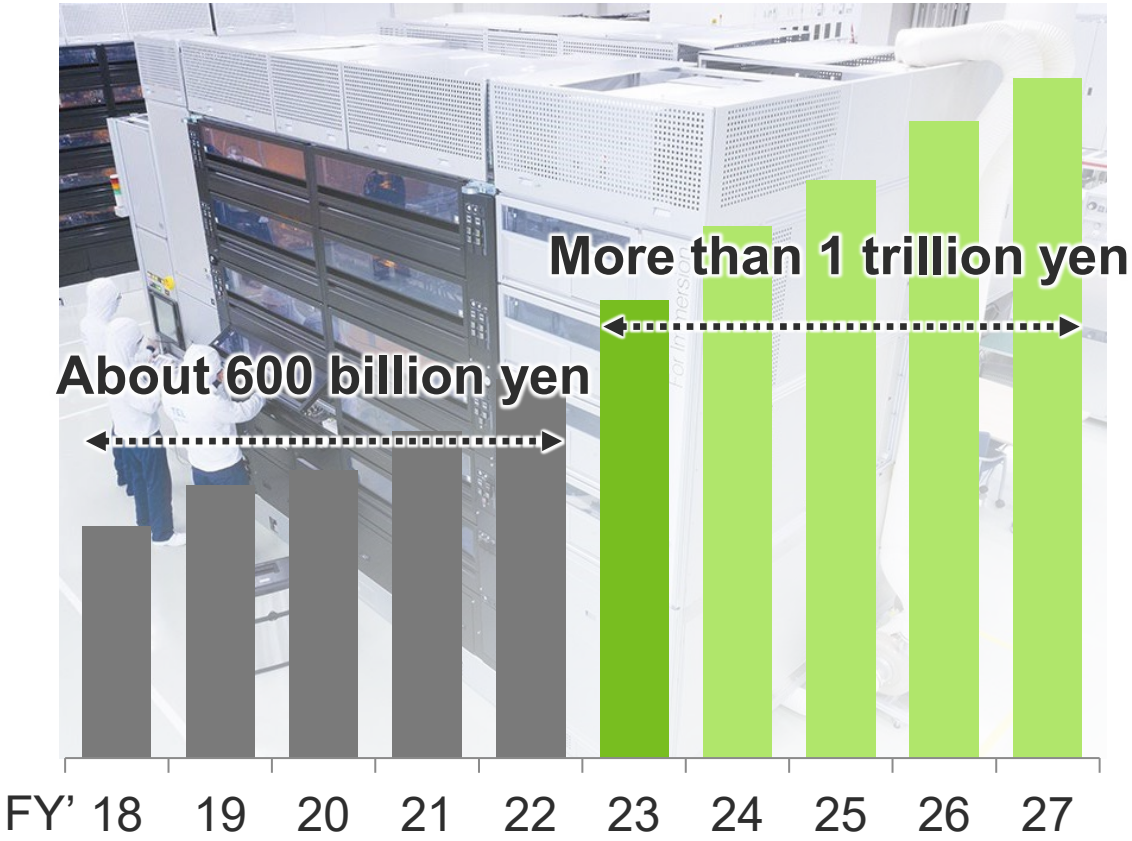
- **Initiatives for Net Zero**
  - ✓ Products/Plants and offices/ Reduction of CO_2 emissions from logistics, etc.
- **Stakeholder Engagement**
- **Safety**
- **Risk Management**
- **Governance**

Toward short- , medium- and long-term profit and continuous corporate value enhancement

The New Medium-term Management Plan : Financial Targets

Financial Targets (by FY'27)	
Net sales	≧ 3 trillion yen
OP margin	≧ 35%
ROE	≧ 30%

Continue to Invest Aggressively on R&D



More than 1 trillion yen planned for 5 years from FY'23

Continue active investment in growth to
create high value-added next-generation products

4. Business Environment and Financial Estimates

Business Environment (WFE Market Outlook as of February 2024)

- **CY2023: Estimated to be around $95B**
  - Upwardly revised estimate with increased investment by Chinese customers
- **CY2024: Forecasted to be around $100B**
  - Expect continued investment by Chinese customers and recovery in investment for leading-edge DRAM in H2
- **CY2025: Double-digit growth expected**
  - Continuing growth of AI servers (CAGR 2023-2027: +31%*)
  - Recovery in PC/smartphone demand
    - New functions, such as on-device AI, for new applications
    - Replacement of products purchased during COVID-19
    - Corporate IT investment

➔ These will drive recoveries forecasted for NAND and advanced logic/foundry capex following DRAM

*Source : Omdia

FY2024 Q3 Business Progress

- Both net sales and profits were firm and proceeded well
- Acquired PORs[*1] through strategic products and progressed development and evaluation towards future growth
  - Acquired PORs: Etching for DRAM HARC[*2], Si etching for advanced logic, backside bevel cleaning for advanced logic
  - Evaluation making good progress towards high-volume cryogenic etching
  - Wafer bonder/debonder: Sharp increase in high-volume orders, more than double expected
- Released new technologies/products contributing to innovation in semiconductor technology
  - Laser lift-off technology: Improved thinning process yield.
    A breakthrough technology that will significantly reduce burden on the environment
  - Ulucus™ G wafer thinning system: Achieved ultra-flat wafers for EUV process and high-density 3D integration utilizing our unique technologies. Will promote the innovation of semiconductor technology and enhance WFE market growth
- Advanced net zero target achievement year by 10 years to CY2040

*1 POR: Process of record
*2 HARC: High aspect ratio contact

FY2024 Financial Estimates

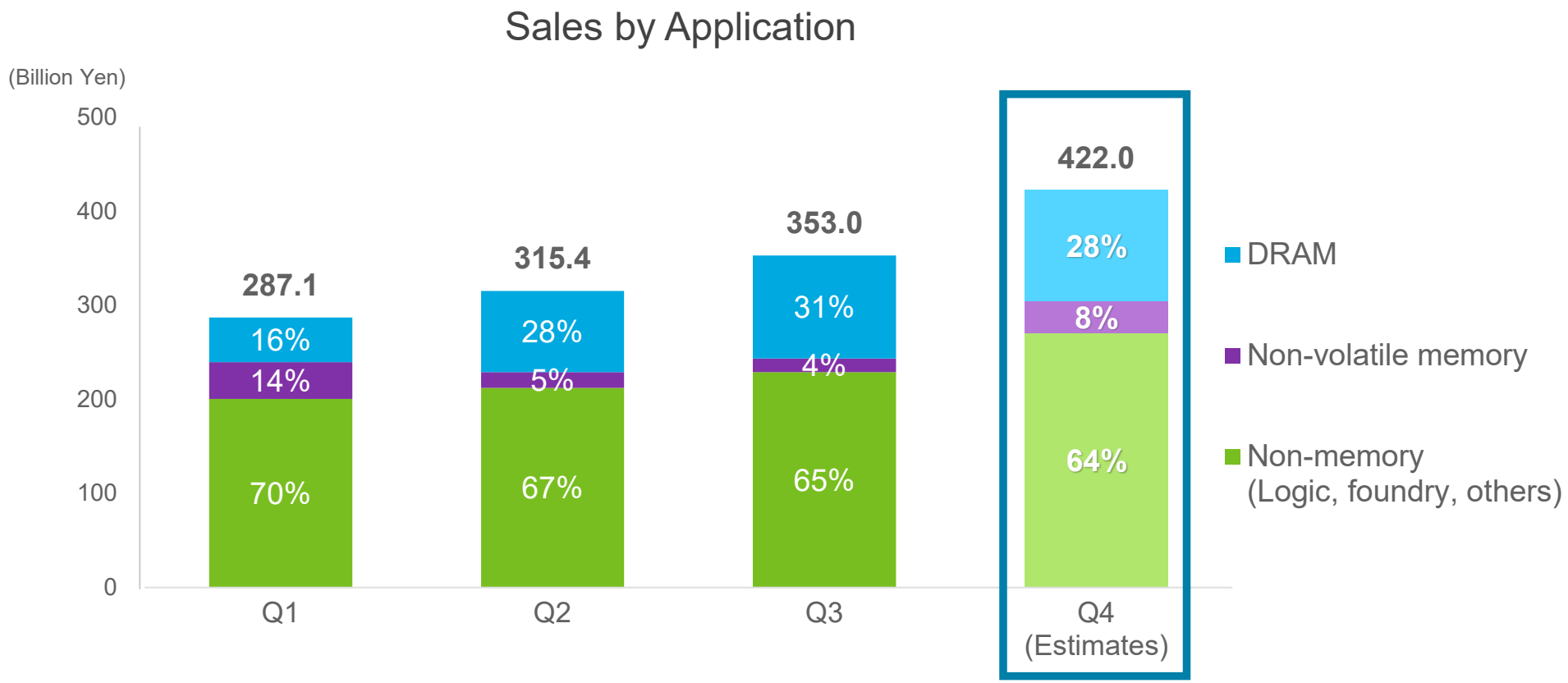
(Billion yen)

	FY2023 (Actual)	FY2024			
		Actual	New Estimates		Adjustments*1
		H1	H2	Full Year	Full Year
Net sales	2,209.0	819.5	1,010.4	1,830.0	+100.0
Gross profit	984.4	352.0	464.9	817.0	+54.0
Gross profit margin	44.6%	43.0%	46.0%	44.6%	+0.5pts
SG&A expenses	366.6	173.4	198.5	372.0	+10.0
R&D	191.1	94.6	110.3	205.0	+0.0
Other than R&D	175.4	78.7	88.2	167.0	+10.0
Operating income	617.7	178.5	266.4	445.0	+44.0
Operating margin	28.0%	21.8%	26.4%	24.3%	+1.1pts
Income before income taxes	624.8	181.1	268.8	450.0	+46.0
Net income attributable to owners of parent	471.5	137.4	202.5	340.0	+33.0
Net income per share (Yen)*2	1,007.82	295.13	-	732.16	+71.02

*1 Changes from the figures announced on November 10, 2023.
*2 The Company implemented a 3-for-1 common stock split on April 1, 2023. Net incomes per share are calculated on the assumption that stock split was implemented at the beginning of FY2023.

Revised financial estimates to reflect the results of Q3 and the estimate of Q4

FY2024 SPE New Equipment Sales Forecast



Percentages on the graph show the composition ratio of new equipment sales. Field solutions sales are not included.

Sales of new equipment are in transition to an upward trend

FY2024 R&D Expenses and Capex Plan

New Development Building
Deposition system, etch system, corporate R&D

Nirasaki-city, Yamanashi Prefecture
Established in July 2023

Tohoku Production and Logistics Center
Deposition system

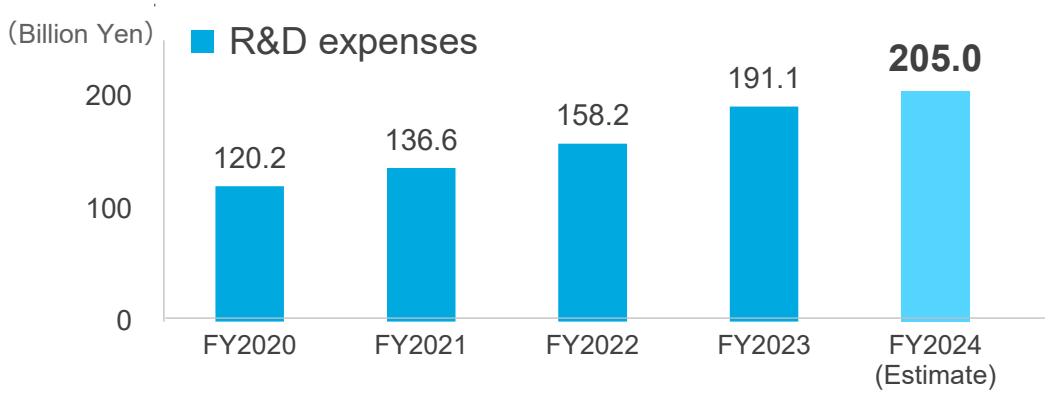
Oshu-city, Iwate Prefecture
Completion scheduled for autumn 2025

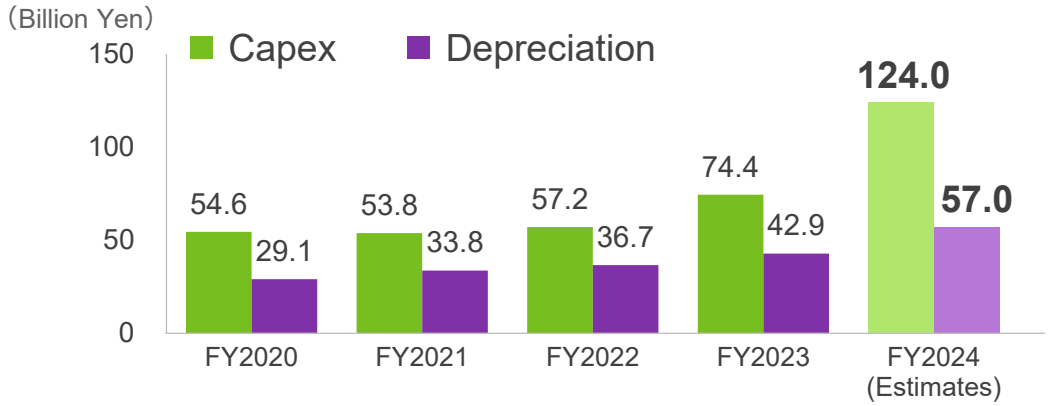
New Development Building
Coater/developer, cleaning system

Koshi-city, Kumamoto Prefecture
Completion scheduled for summer 2025

New Development Building
Etch system

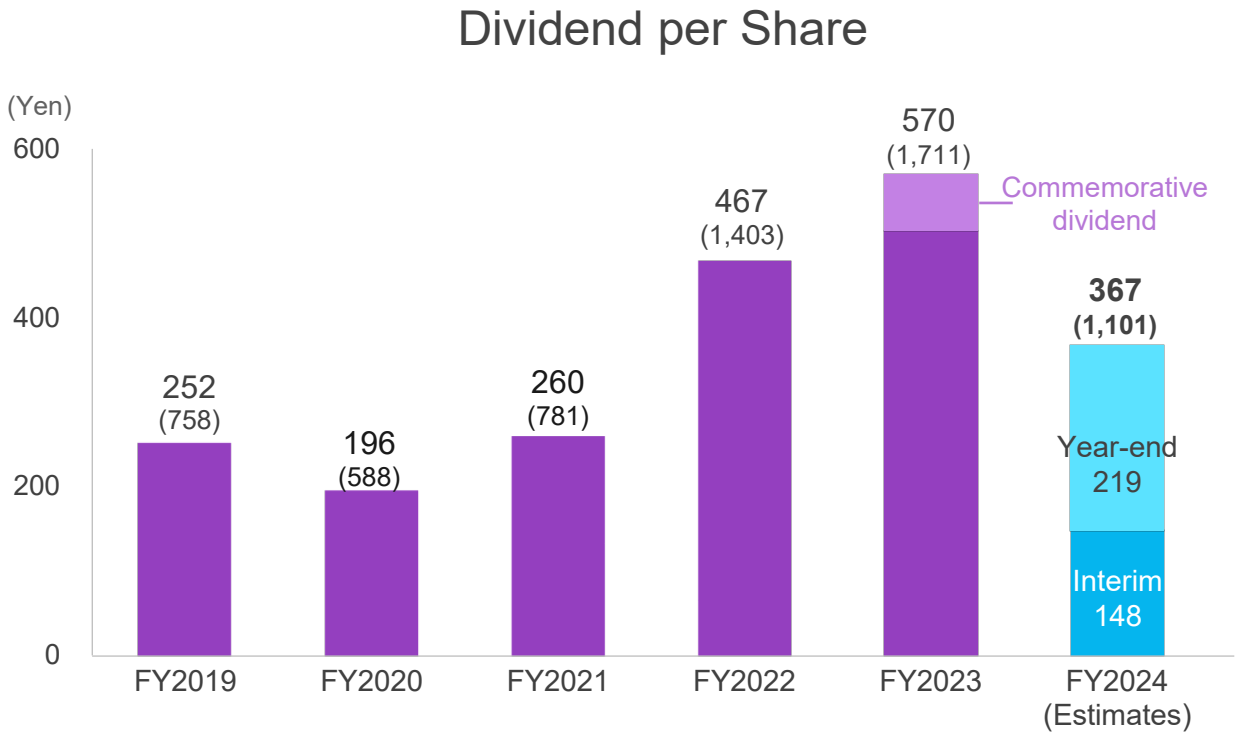
Kurokawa-gun, Miyagi Prefecture
Completion scheduled for spring 2025





Continue aggressive R&D and capital investments for sustainable growth

FY2024 Dividend Forecast



TEL shareholder return policy

Dividend payout ratio: 50%

Annual DPS of not less than 50 yen*

We will review our dividend policy if the company does not generate net income for two consecutive fiscal years

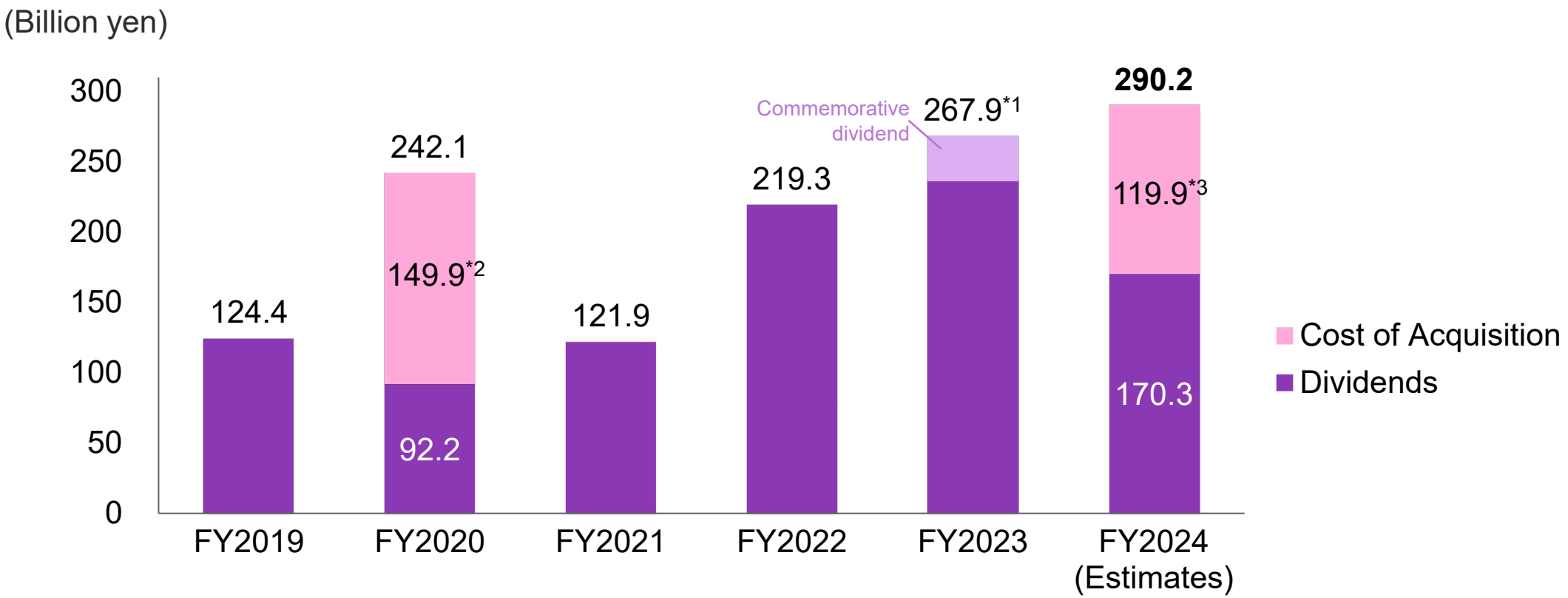
We will flexibly consider share buybacks

*Due to the stock split on April 1, 2023, the amount has been changed from 150 yen to 50 yen.

- Dividends per share from FY2019 to FY2023 are calculated on the assumption that the stock split was conducted at the beginning of FY2019.
- FY2023 includes the 60th anniversary commemorative dividends.
- Amounts before the stock split are shown in parentheses.

Implemented a 3-for-1 common stock split on April 1, 2023.
Full-year dividends are expected to be 367 yen per share

Total Return Amount



*1 FY2023 dividend payment of 267.9 billion yen includes commemorative dividend (31.3 billion yen).
*2 https://www.tel.com/news/ir/2020/20200106_001.html
*3 https://www.tel.com/news/ir/2023/de4nhu0000000045-att/20231002_001_e.pdf

Combined with share buyback, total return amount is expected to be record high

5. Corporate Sustainability

Sustainability Initiatives

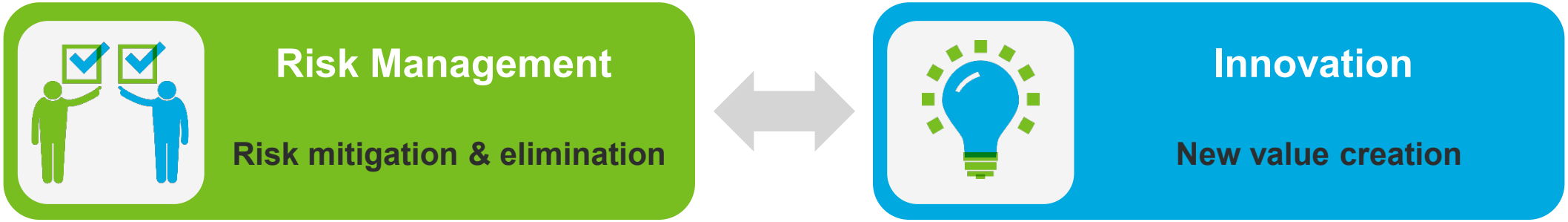
The four material issues (key issues) that require prioritized attention and actions are identified to implement sustainability initiatives through our business operation and contribute to the resolution of industrial and social issues.

SUSTAINABLE DEVELOPMENT GOALS

ESG Activities

Environment	Social	Governance
▪ Pursuing higher device performance and lower power consumption ▪ Achieving both high process performance and environmental performance of the equipment ▪ Reduction of CO_2 emissions in all business activities	▪ Human Rights ▪ Human Capital Management ▪ Health and Safety ▪ Customer Satisfaction ▪ Supply Chain Management	▪ Corporate Governance ▪ Compliance ▪ Risk Management ▪ Information Security

Risk Management



TCFD | TASK FORCE ON CLIMATE-RELATED FINANCIAL DISCLOSURES

Sustainability-focused management aiming to remain a company that is loved and trusted by all stakeholders. Promotion of technological innovation of semiconductors and reduction of environmental impact in supply chain

Environmental Approaches

Net Zero

New target **Scope 1, 2 & 3** **by 2040**

Scope 1&2: CO2 Emissions from energy use such as electricity in business activities
Scope 3 : CO2 Emissions from the use and disposal of sold equipment, material purchases and logistics, etc.

E-COMPASS

Environmental Co-Creation by Material, Process and Subcomponent Solutions

Semiconductors	Products	Business activities
Higher device performance and lower power consumption	Compatibility of equipment process performance and environmental performance	Reduction of CO2 emissions in all business activities

Promoting technological innovation of semiconductors and reducing environmental impact throughout the supply chain

Safety & Quality

Safety

Under the “Safety First” slogan, everyone at Tokyo Electron, from top management to field representative, is actively and continuously improving safety and promoting health, giving safety and health the highest priority when carrying out different types of operations such as development, manufacturing, transportation, installation and maintenance.

(FY2023)

Safety Goals
(by FY’27)
TCIR ≤ 0.1

TCIR: Total Case Incident Rate（Number of workplace injuries per 200,000 work hours）

Incident Prevention Initiatives

- Experiential training and VR (Virtual Reality)
- Comprehensive safety inspections
- Feedback on safety specifications
- Safety activities for suppliers

Quality

The Tokyo Electron Group seeks to provide the highest-quality products and services. This pursuit of quality begins at development and continues through all manufacturing, installation, maintenance, sales and support processes. Our employees must work to deliver quality products, quality services and innovative solutions that enable customer success.

Quality Policy

1 Quality Focus

2 Quality Design and Assurance

3 Quality and Trust

4 Continual Improvement

5 Stakeholder Communication

TEL Values as codes of conduct

Engagement

Career

Corporate growth is enabled by people, and our employees both create and fulfill company values

Retention

Work-life balance

Diversity, Equity and Inclusion

3Gs

Global・Generation・Gender

Human Rights Policy and Due Diligence

The five focus areas in human rights (Tokyo Electron Group Human Rights Policy)

- Freedom, equality & non-discrimination
- Freely chosen employment
- Product safety & workplace health and safety
- Freedom of association
- Appropriate working hours & breaks/ holidays/vacations

Commitment

Commitment to respecting human rights

- Revision of Tokyo Electron Group Human Rights Policy
- Awareness and implementation
- Education

Assessment

Assessment of human rights risks in business and supply chains

- Human rights risk assessment
- Human rights impact assessment

Remediation

Actions to reduce risks based on assessment results

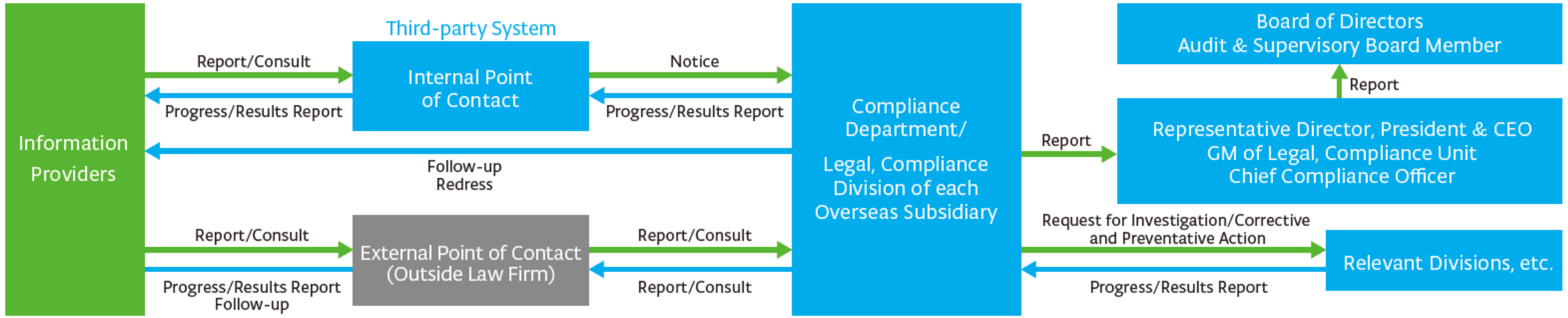
- Feedback sheet publication
- Program development and review according to issues

Report

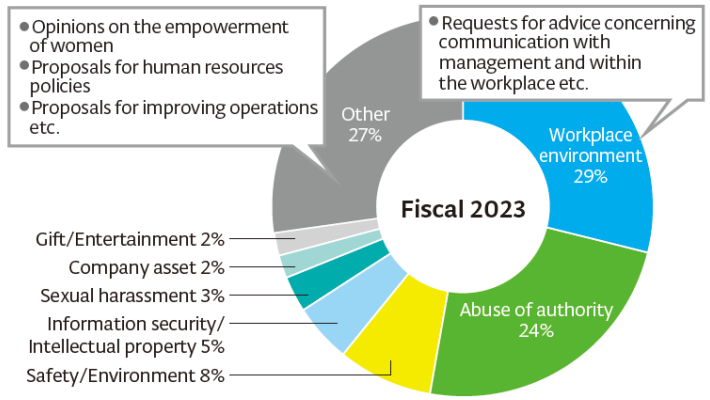
Regular disclosure of information

- Publication of the Integrated Report
- Postings on the website

Internal Reporting System



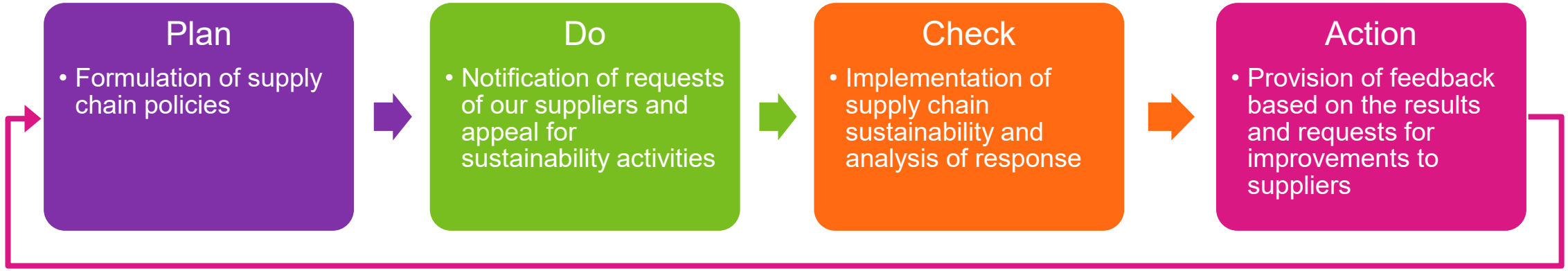
Breakdown of Consultation/Report Contents



Respect for human rights with a strong sense of integrity

Supply Chain Management

Supply chain sustainability process

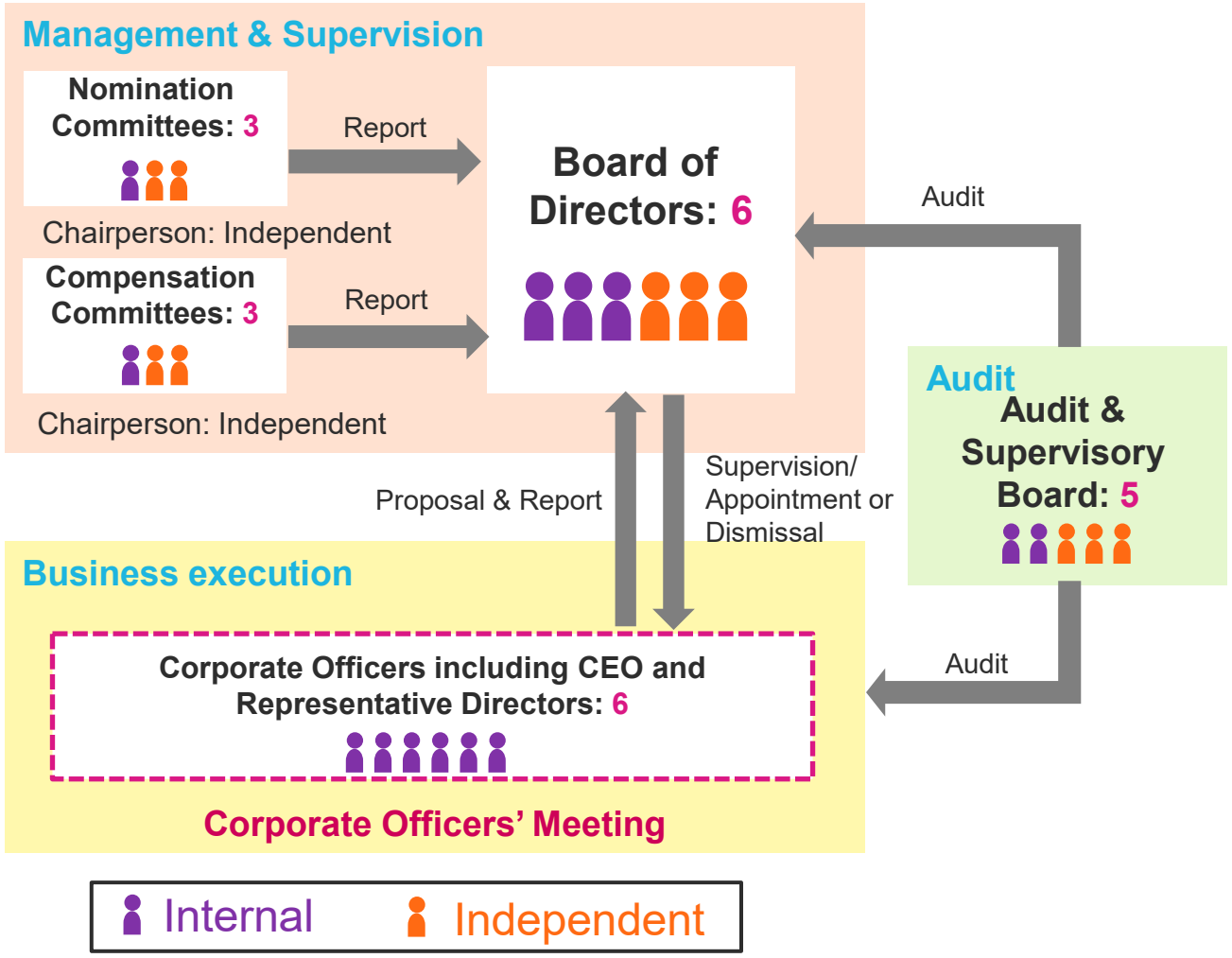


- Annual Sustainability Assessment
  - Assessment base on RBA code of conduct
  - Corrective Action Plans
- RBA Audit
  - At primary manufacturing sites
  - Continuous improvement in respective operations

Pursuit of sustainability conscious operations throughout the supply chain

Corporate Governance Framework (Audit & Supervisory Board System)

<Framework (Excerpt)>



The era of ultra VUCA

↓

Sharp growth of the semiconductor market

↓

Need to improve the **quality** and **speed** of decision making in both "**Management & Supervision**" and "**Business execution**"

↓

Strengthen and optimize 3 functions:

1) In-depth discussion of mid- to long-term growth strategies
2) Supervision of business execution
3) Decision-making on business execution

Accelerate "proactive management"

Growth of short-/mid-/long-term profits

Increase corporate value continually

Evaluation of the Effectiveness of the Board of Directors

Internal and external experts analyze and evaluate the effectiveness of the Board of Directors

Global Initiatives

Sustainable Development Goals (SDGs)

Clarify initiatives through business by materiality and deploy company-wide

Tokyo Electron supports the SDGs

Participation in International Initiatives

Signed the UN Global Compact, joined the Responsible Business Alliance (RBA), endorsed the Task Force on Climate-related Financial Disclosures (TCFD)

WE SUPPORT UN GLOBAL COMPACT

Responsible Business Alliance
Affiliate Member

TCFD TASK FORCE ON CLIMATE-RELATED FINANCIAL DISCLOSURES

External Evaluation on our ESG Initiatives

Highly rated by evaluation organizations around the world

Member of Dow Jones Sustainability Indices
Powered by the S&P Global CSA

FTSE4Good

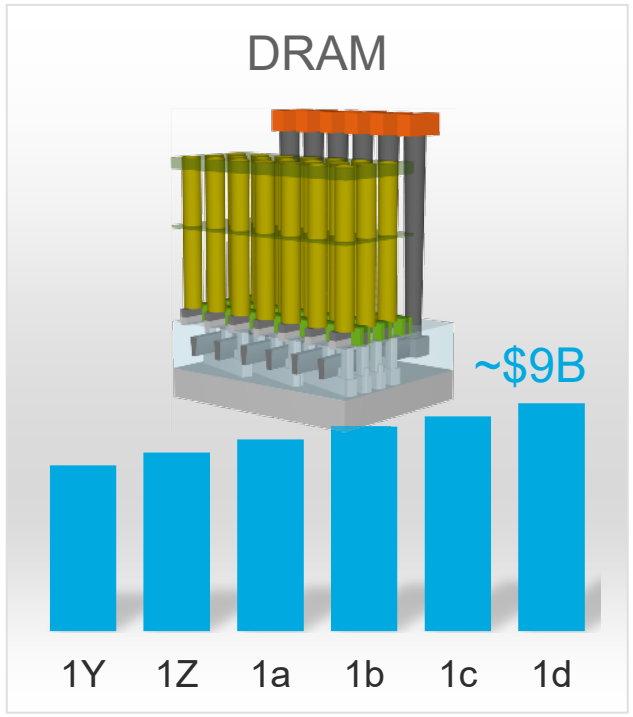
2023 MSCI ESG Leaders Indexes Constituent

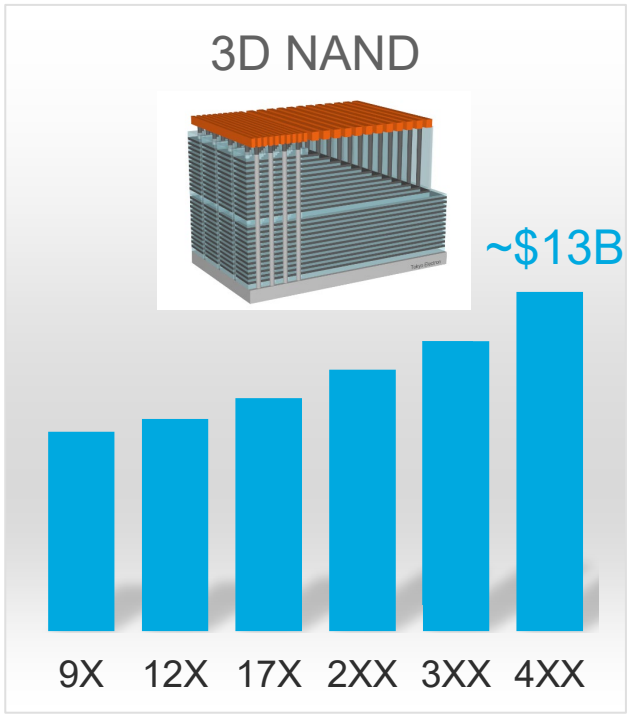
6. Diversity of Semiconductor Technology

6-1 : Technology Roadmap

Raising Added-value in SPE

WFE investment (100k WSPM*, greenfield/TEL estimates)

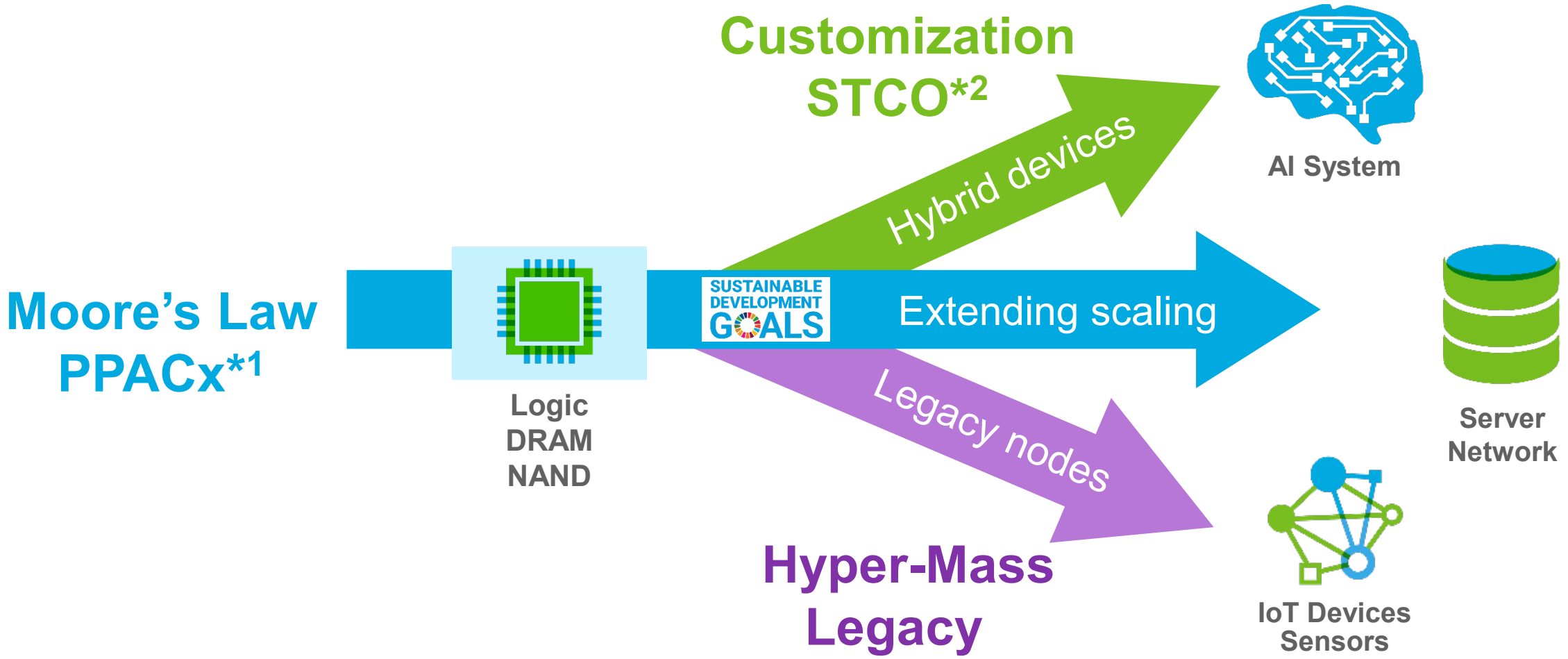




Expanding business opportunities for SPE manufacturers on arrival of new applications and rising level of technological difficulty

* WSPM: Wafer starts per month

Roadmap for the Next 10 Years

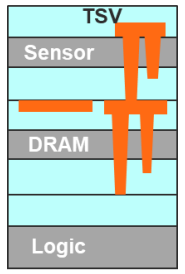
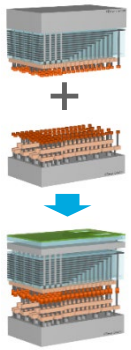
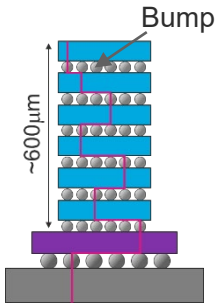
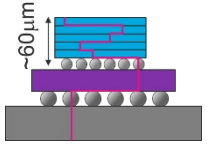
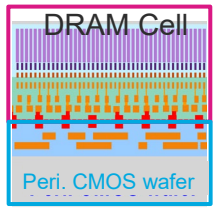
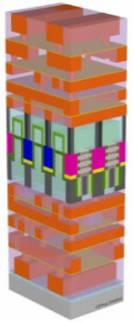
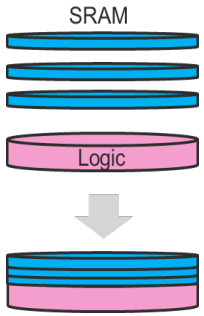
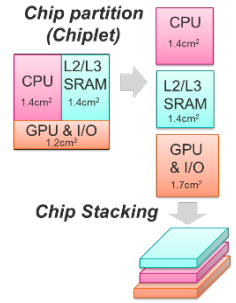


Development of SDGs-compatible technology for incorporation into diversifying applications

*1 PPACx: Power Performance Area Cost, x
*2 STCO: System Technology Co-Optimization

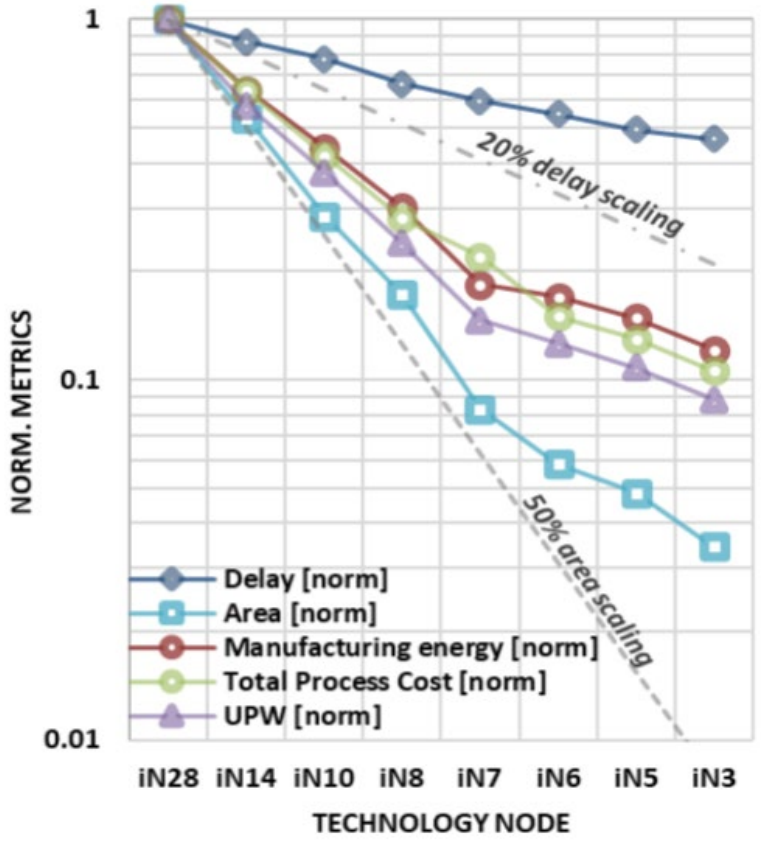
Advances in System Integration: More Options

Source: TEL estimates

Device	CIS	3D NAND	DRAM			Logic		
Stacking	Sensor+ DRAM + Logic	Cell + Peri	HBM (w/ Bump)	HBM (Bump-less)	Cell + Peri	Backside PDN	Logic + SRAM Cell	3D Hybrid Logic + I/O + RF
Bonder Type	W-W	W-W	D-W	W-W		W-W	W-W/D-W	D-W
	Fusion (Permanent)	Fusion (Permanent)	Temporary (Bonding / De-bonding)	Fusion (Permanent)		Fusion (Permanent)		Temporary & Fusion
	Cu to Cu Hybrid	Cu to Cu Hybrid		Cu to Cu Hybrid		Ox to Ox	Cu to Cu Hybrid	
Wafer THK	3μm	4μm	10μm	3μm	2μm	1μm	2μm~1μm	2μm
Structure	 Source: H. Tsugawa, Sony (IEDM2017)		 Source: Sakui, TIT (CICC2019)	 Source: Sakui, TIT (CICC2019)				
Status	HVM	R&D~MP	HVM	R&D	R&D	R&D	R&D	R&D

System integration techniques also optimized via PPACx

Correlation b/w Environmental KPIs and Technology Node Migration



Graph courtesy of imec

Observations

- Performance is still improving node-over-node but at a reduced rate (delay)
- Area scaling is being achieved but slowing beyond IN7 (~ Foundry 5nm)
- Technology node still drives reduction in manufacturing energy per device
- Cost of manufacturing is still declining
- Water usage is still declining

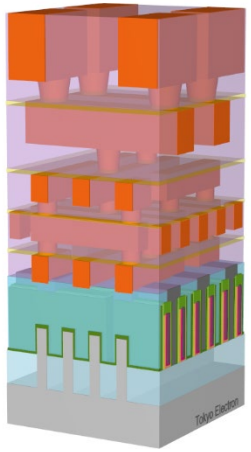
Conclusion

- Advancing technology nodes contributes towards SDGs
- But slowing pace of reduction implies that further innovation is needed
- Working on advanced node devices contributes to SDGs

Advanced technology development is directly linked to the SDGs

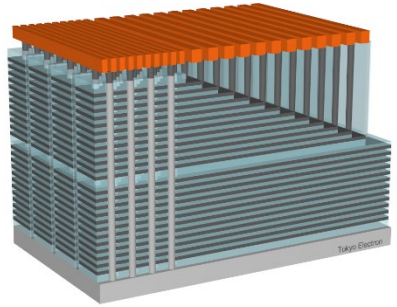
Semiconductor Devices: Direction of Development

Logic



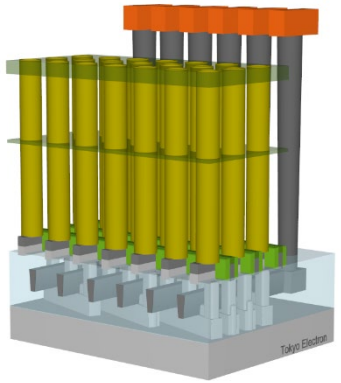
Through miniaturization with structural changes
- Lowered cost per transistor
- Lower power consumption
- Higher speed

NAND



Through high stacking
- Lower cost per bit

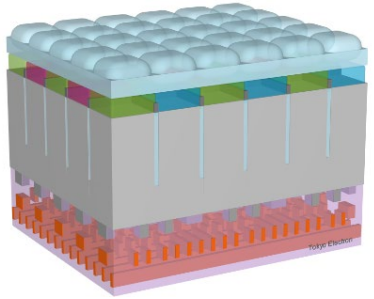
DRAM



Through miniaturization
- Lower cost per bit
- Lower power consumption
- Higher speed

Through new structures
- Lower cost per bit

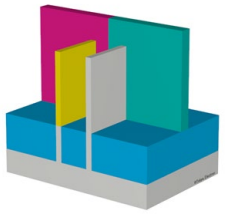
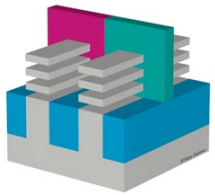
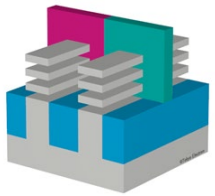
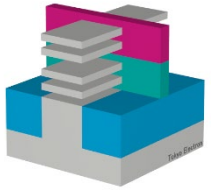
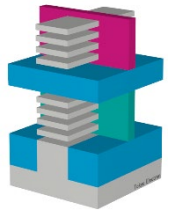
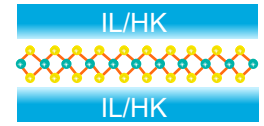
CIS



Through miniaturization
- Increased number of pixels
- Higher speed

Through new structures, new materials
- Greater image quality

Logic Technology Roadmap: Generic

Year of HVM (20k/month)	2022~23	2024~2025	2027~28	2029	2031	2033	2035
Node	**3nm**	**2nm**	**14A**	**10A**	**7A**	**5A**	**3A**
Transistor	2~1 Fin 	GAA NS 	GAA NS scaling 	CFET 	2nd Gen. CFET 	3rd Gen. CFET 	 2D material: TMDC MoS_2, WS_2, $MoSe_2$, WSe_2 etc.
Poly Pitch [nm]	45 [1]		42		39		36
Min. Metal Pitch [nm]	23 [2]		20	18	16	14	12
Interconnect booster	Cu Barrier/Seed CIP Backside PDN			Subtractive Ru + Ru via fill AR>2, k<3 fill / AR>3, Airgap		New alloy AR>5, Airgap	AR>7, Airgap
EUV Patterning Technology	EUV MP, SE			EUV MP, SE High NA SE		High NA MP, SE EUV MP, SE	
Resist	CAR	CAR (+MOR)	CAR+MOR				

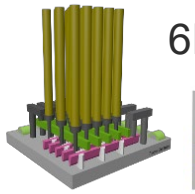
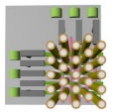
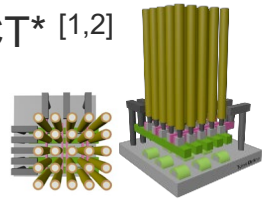
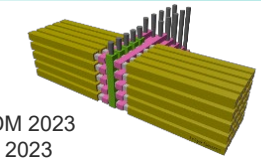
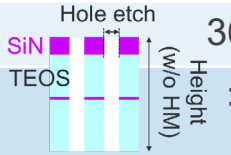
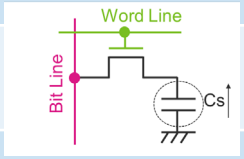
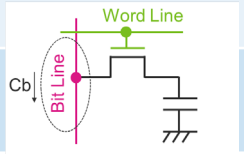
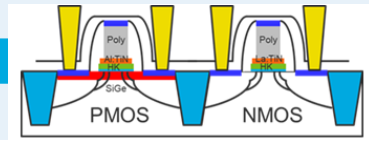
[1] Chih-Hao Chang (TSMC) et al., IEDM 2022
[2] Shien-Yang Wu (TSMC) et al., IEDM 2022

MP: Multi-Patterning, SE: Single-Exposure, CAR: Chemically Amplified Resist, MOR: Metal Oxide Resist

Logic scaling will go with transistor structure and material evolution.

DRAM Technology Roadmap: Generic

Source: TEL estimates

Year of HVM (20k/month)	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Node	1b		1c		1d		0a		0b	0c	0d
Cell layout / Structure	2D										
	 6F² 					4F² VCT* [1,2] 			3D 		
F [nm] in 6F²	13		12~11		11~10		10~9		8	7	
Cap. pitch [nm]	39		36~33		33~30		30~27		24	21	
Cap. A.R.	>50 		>55		>65		>70		>75	>80	
Cap. Mat.	ZrAlHfO						Alternative (HfZrO Anti Ferro, STO etc.)				
BL	W LK spacer						Low R metal				
Peri. CMOS	HKMG 										

* Vertical Channel Transistor
[1] Seokhan Park (Samsung) et al., IEDM 2023
[2] Daewon Ha (Samsung) et al., IEDM 2023

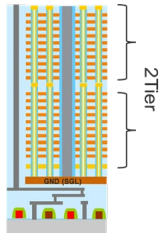
NAND Technology Roadmap: Generic

Source: TEL estimates

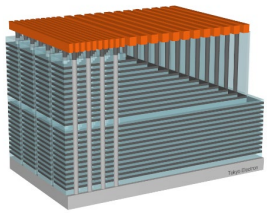
Year of HVM (20k/month)	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Stack (~1.3x/1.5years)	**2xxL (238)**		**3xxL (328)**		**4xxL (424)**		**5xxL (552)**		**7xxL (728)**	**9xxL (966)**	**1xxx (1294)**
Tier	2		2 or 3		3 or 4		3 or 4		3 or 4	4 or 5	4 or 5
Vertical pitch [nm]	42		40		38		37		36	35	34
Memory height[1] [μm]	10.79		13.88		16.83		21.13		26.89	34.48	44.64
Charge trap (CT)	CT isolation										
Channel	Poly Si grain CIP						incl. MILC[4]/MIC[5] Si				
WL metal	W		W or Mo		Mo		Mo		Mo	Mo	Mo
Width btw. Slits[2] [nm] (#holes[3])	1270~2700 (9~20)		1920~3220 (14~24)		2570~3220 (19~24)		2570~4260 (19~32)		> 4260 (> 32)	> 4260 (> 32)	> 4260 (> 32)
Peri. CMOS	Under array or Bonding		Under array or Bonding		Bonding		Bonding		Bonding	Bonding	Bonding

Re/Fe NAND

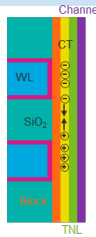
[1] Vertical pitch x (active layer# + 19)
[2] 130 nm x #holes + 100 nm
[3] #of memory holes b/w slits
[4] Metal induced lateral crystallization
[5] Metal induced crystallization



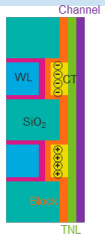
Tier



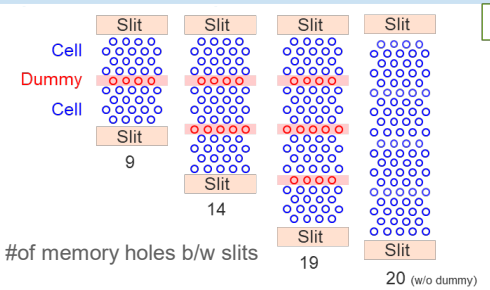
Vertical pitch



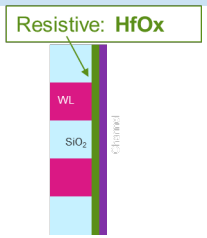
Current



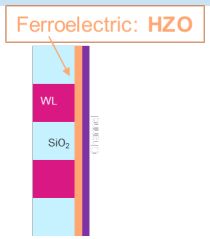
CT isolation



#of memory holes b/w slits



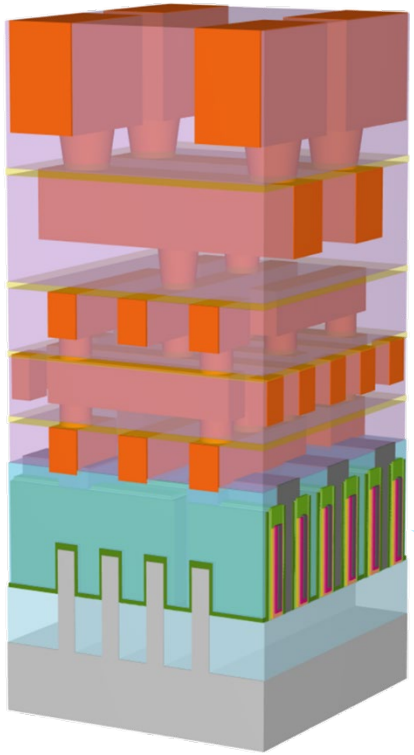
ReNAND



FeNAND

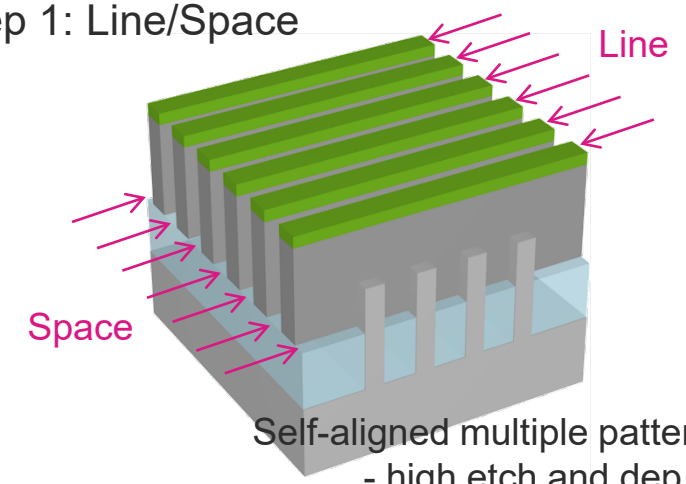
6-2 : Effects of EUV Lithography Adoption and Technology Trends

Logic: Overcoming Technological Hurdles (Placement Errors) with EUV



Cross section of a logic structure

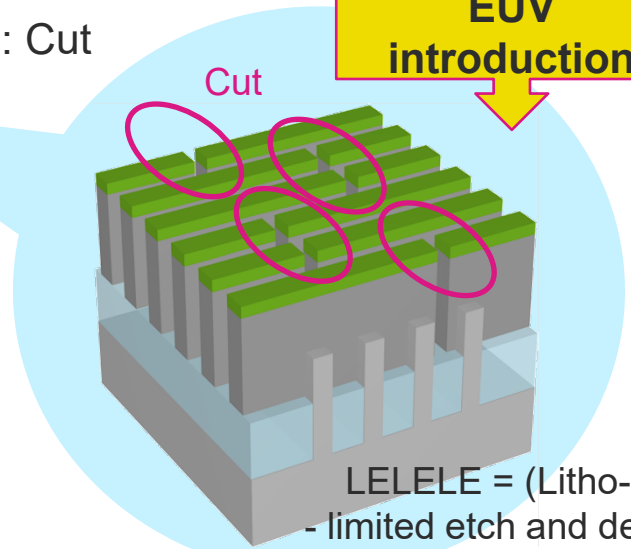
Step 1: Line/Space



Self-aligned multiple patterning (SAMP)
- high etch and dep usage

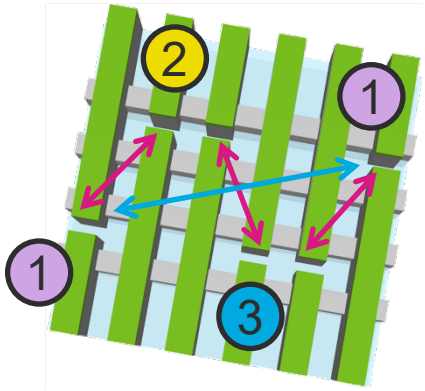
Step 2: Cut

EUV introduction



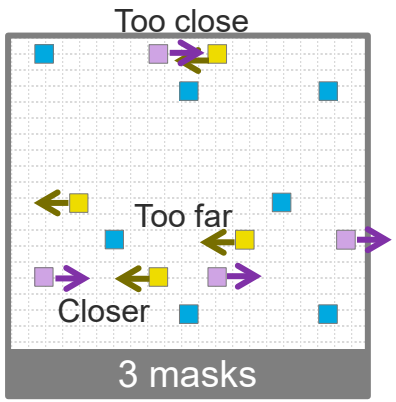
LELELE = $(Litho\text{-}Etch)_3$
- limited etch and dep usage

Conventional exposure



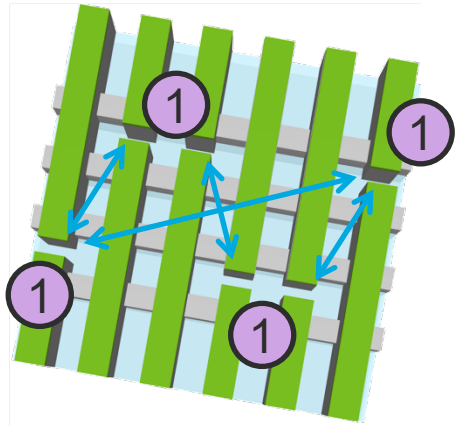
Three exposures: (Litho + Etch) x 3

Each exposure process creates placement errors



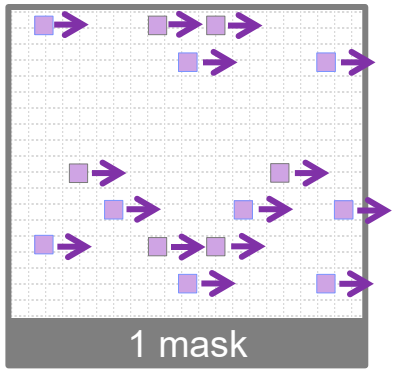
Lower yield

Exposure using EUV



One exposure: (Litho + Etch) x 1

Placement errors reduced



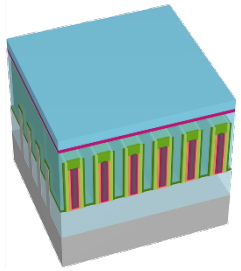
Increased yield

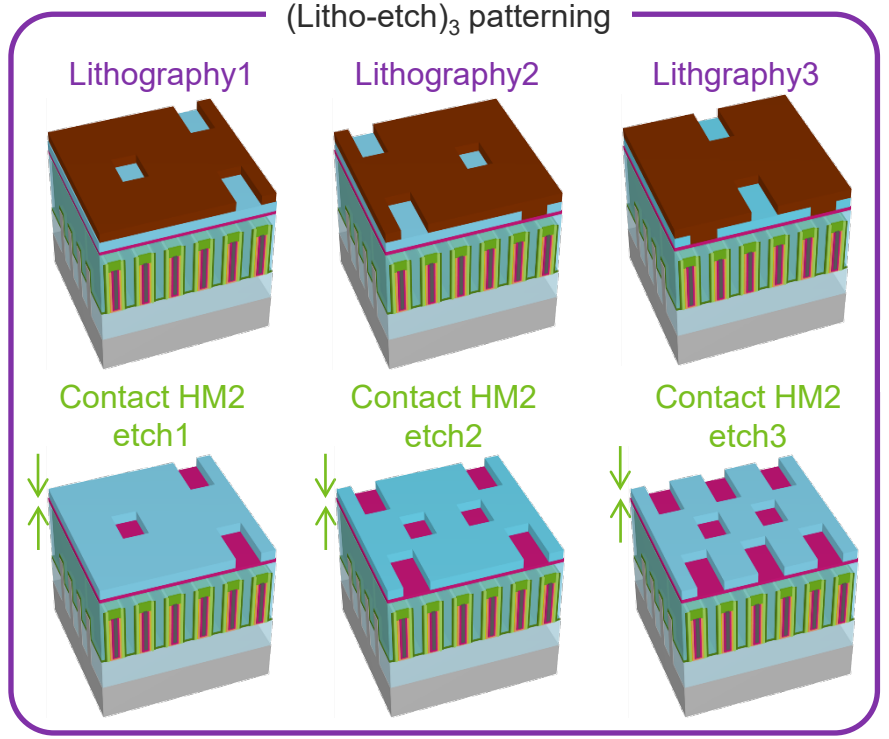
$(\text{Litho-etch})_n$ Patterning for Logic MOL Contact/Cut Module

- PMD dep
- Hard mask1 dep
- Hard mask2 dep
- Lithography1
- Contact HM2 etch1 ← short etch time
- Lithography2
- Contact HM2 etch2 ← short etch time
- Lithography3
- Contact HM2 etch3 ← short etch time
- Contact HM1 etch ← short etch time
- Contact PMD etch ← long etch time
- Post etch clean
- Barrier metal Ti/TiN dep
- Contact plug W dep
- Contact plug W CMP

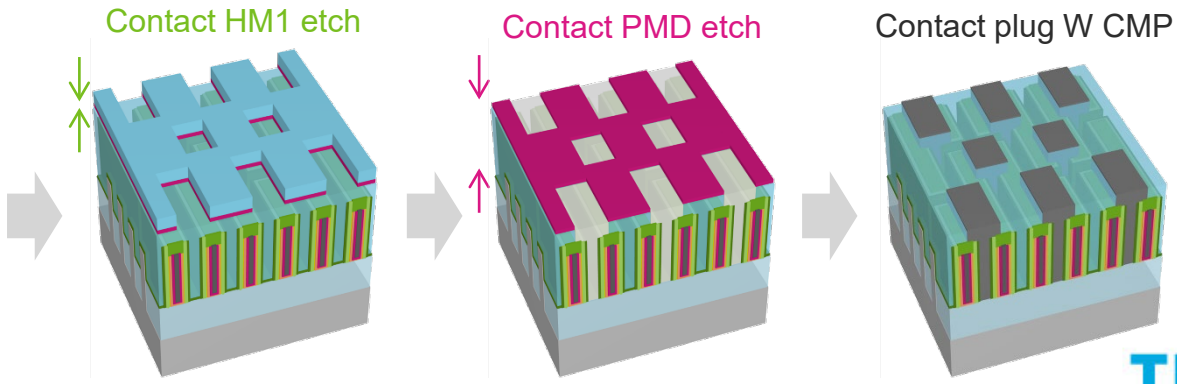
$(\text{Litho-etch})_n$ patterning

✓ Thicker layer
✓ Higher etch selectivity





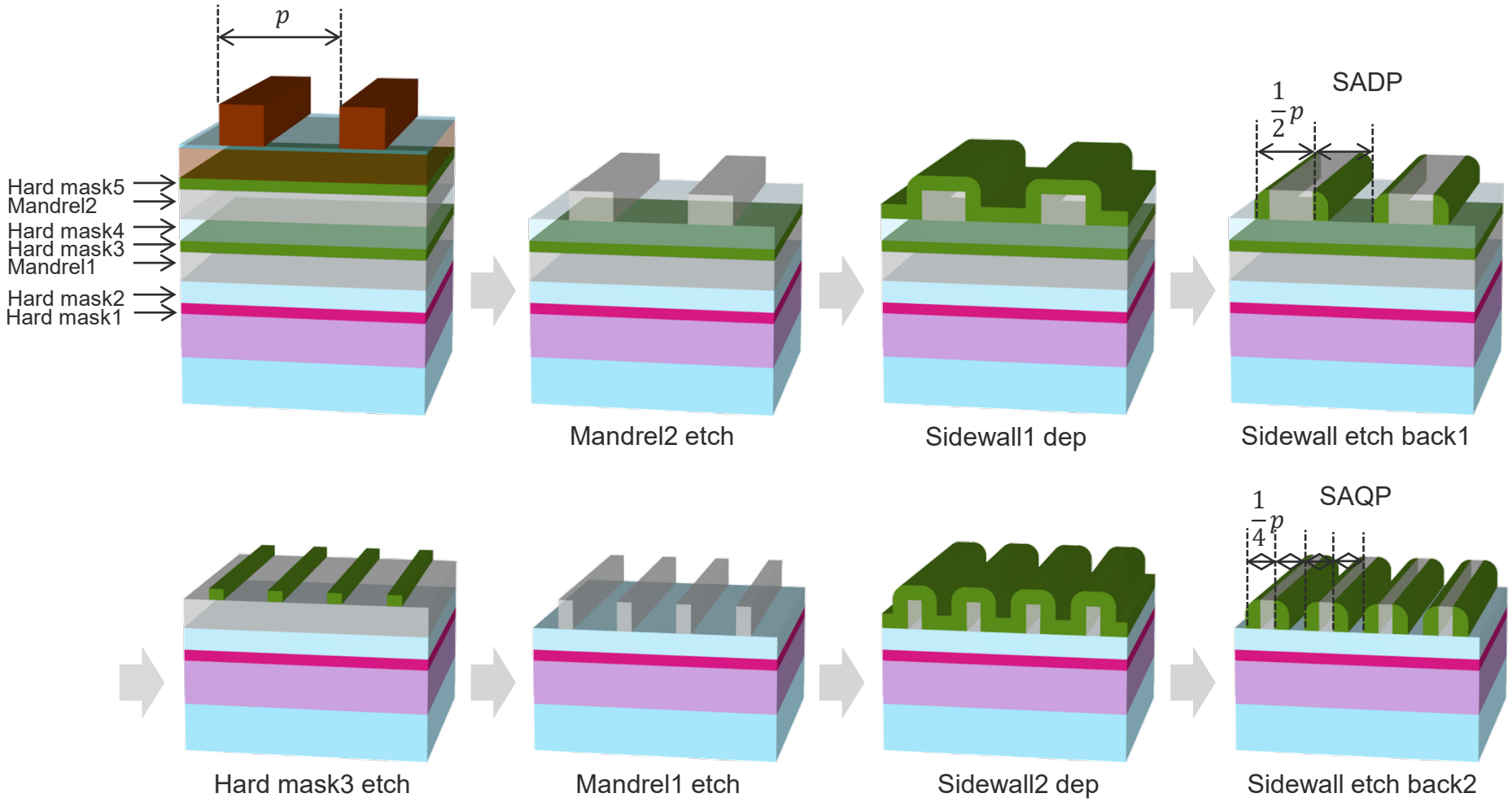
or



Self-aligned Multiple Patterning for Line/Space

- Had mask1 dep
- Hard mask2 dep
- Mandrel1 dep
- Hard mask3 dep
- Hard mask4 dep
- Mandrel2 dep
- Hard mask5 dep
- Lithography
- Hard mask5 etch
- Mandrel2 etch
- Sidewall1 dep
- Sidewall1 etch back
- Mandrel2 pull
- Hard mask4 etch
- Hard mask3 etch
- Mandrel1 etch
- Sidewall2 dep
- Sidewall2 etch back

Lithography
Deposition
Etch



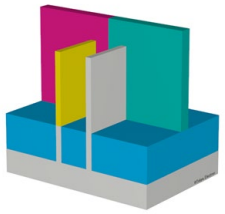
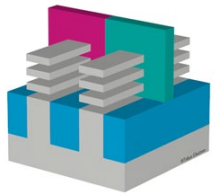
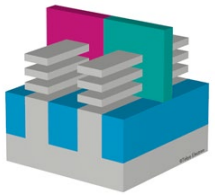
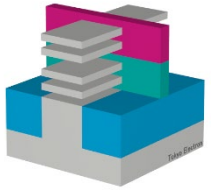
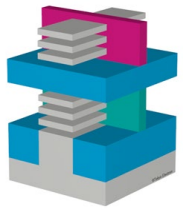
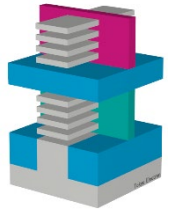
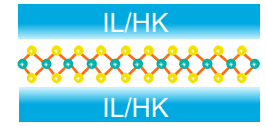
SADP: Self-aligned double patterning
SAQP: Self-aligned quadruple patterning

Effects of EUV Lithography Adoption

- EUV adoption will solve sophisticated technological hurdles our customers face (i.e. placement errors), bringing about quite positive effects on semiconductor and SPE industries
  - Advance miniaturization
  - Accelerate customers' investment in next generation technologies by enhancing the yield
- Further miniaturization led by EUV will create more differentiation of our products and business opportunities
  - Increase our coater/developer market share even further
  - Expand demand for etch, deposition and cleaning equipment
  - Differentiate our product through advancing self-aligned patterning technology
  - Expand business with process integration, leveraging our robust product lineup

EUV Lithography Technology Roadmap in Logic

Source: TEL estimates

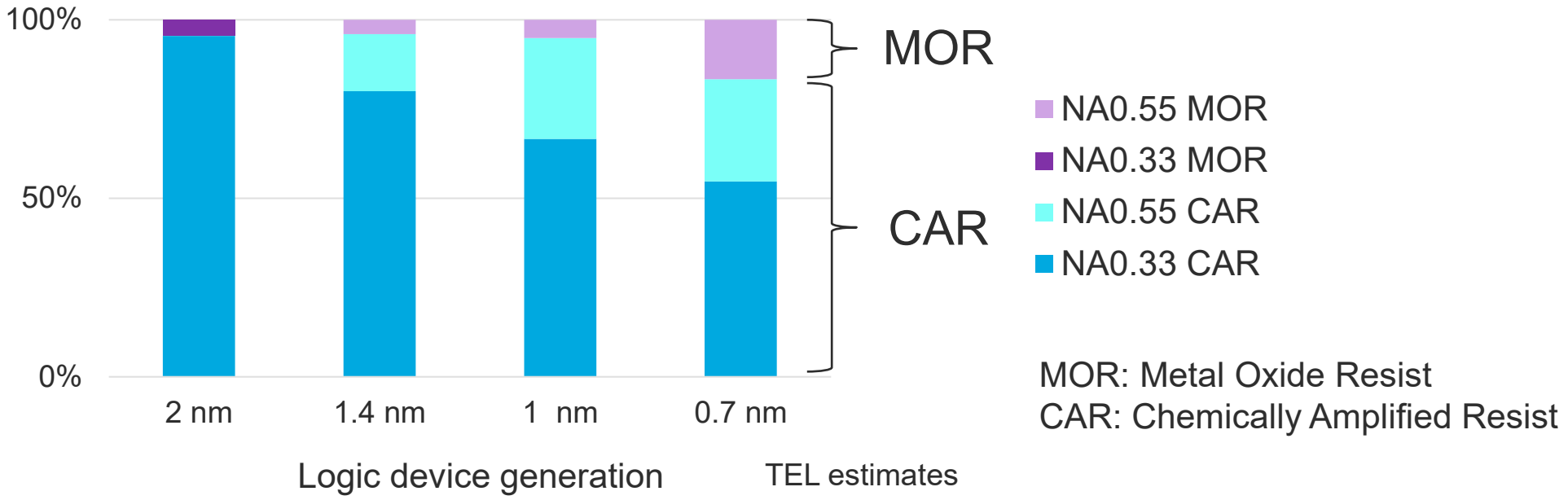
Year of HVM (20k/month)	2022~23	2024~2025	2027~28	2029	2031	2033	2035
Node	**3nm**	**2nm**	**14A**	**10A**	**7A**	**5A**	**3A**
Device	2~1 Fin 	GAA NS 	GAA NS scaling 	CFET 	2nd Gen. CFET 	3rd Gen. CFET 	 2D material: TMDC MoS_2, WS_2, $MoSe_2$, WSe_2 etc.
Poly pitch (PP)	45[1]		42		39		36
Min. MP [nm]	23[2]		20	18	16	14	12
EUV patterning technology	EUV MP			EUV MP **High-NA EUV**		EUV MP **High-NA EUV MP**	
Resist	**CAR**	**CAR (+MOR)**	**CAR+MOR**	**CAR+MOR**	**CAR+MOR**	**CAR+MOR**	**CAR+MOR**

[1] Chih-Hao Chang (TSMC) et al., IEDM 2022
[2] Shien-Yang Wu (TSMC) et al., IEDM 2022

CAR: Chemically Amplified Resist, MOR: Metal Oxide Resist, MP: Multi-patterning

Enhancing versatility of coater/developer to respond to future EUV lithography technologies including MOR and high-NA EUV

Forecast of EUV CAR/MOR Application Layer Counts in Logic Device

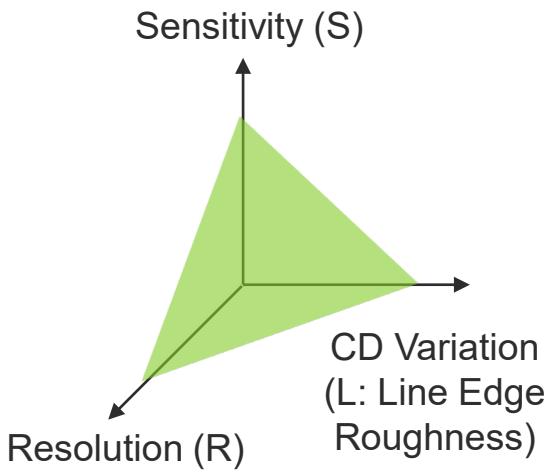


MOR ratio is gradually rising, but CAR ratio remains high.
Our coater/developer achieves high versatility by handling MOR and CAR in one system.
Technologies for high-NA (NA0.55) lithography are under development as it is expected to increase application

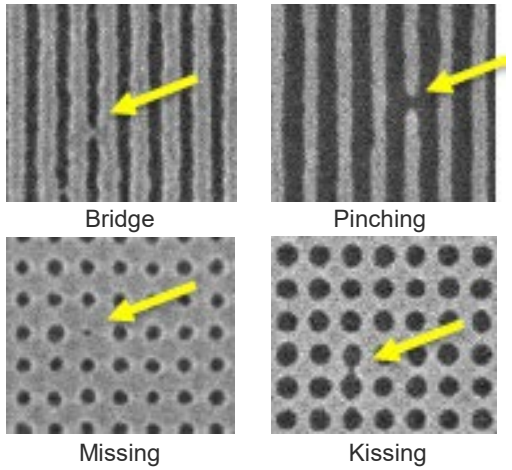
EUV Lithography Process Roadmap and Challenges

Line pitch (nm)	34	32	30	28	26	24	22	20
Hole pitch (nm)	42	40	38	36	34	32	30	22
Trend of EUV exposure equipment and resist technology	0.33 NA EUV				0.55 NA EUV (High-NA EUV: Higher resolution)			
	Chemically Amplified Resist (CAR)							
			Metal Oxide Resist (MOR)					

RLS trade off

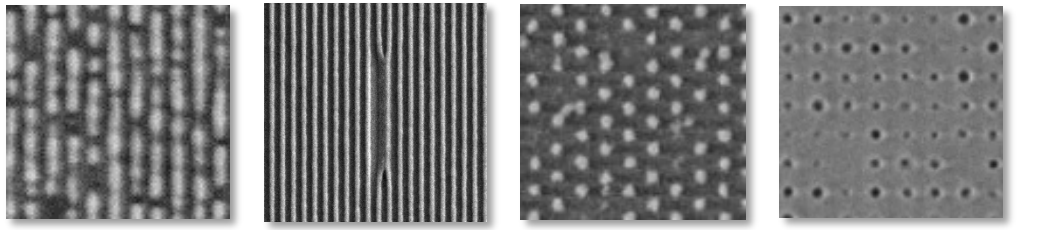


Defects induced by variation in EUV lithography



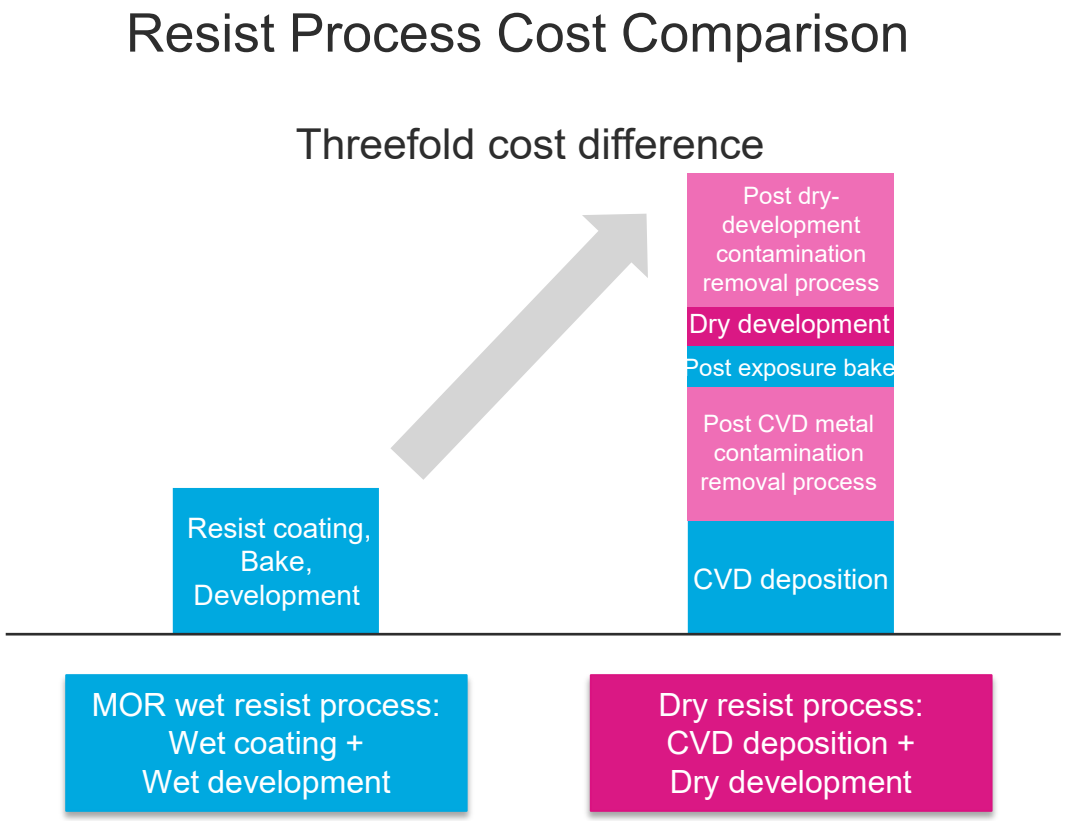
P. De Bisschop, Proc. SPIE, 10957-10 (2019)

Issue of securing required resist film thickness



Challenges for Thinning Resist Film ⟷ Challenges for Thickening Resist Film

MOR Wet Resist Process and Dry Resist Process Cost Comparison



Dry film deposition and dry development process CoO is around three times higher than for wet coating and development

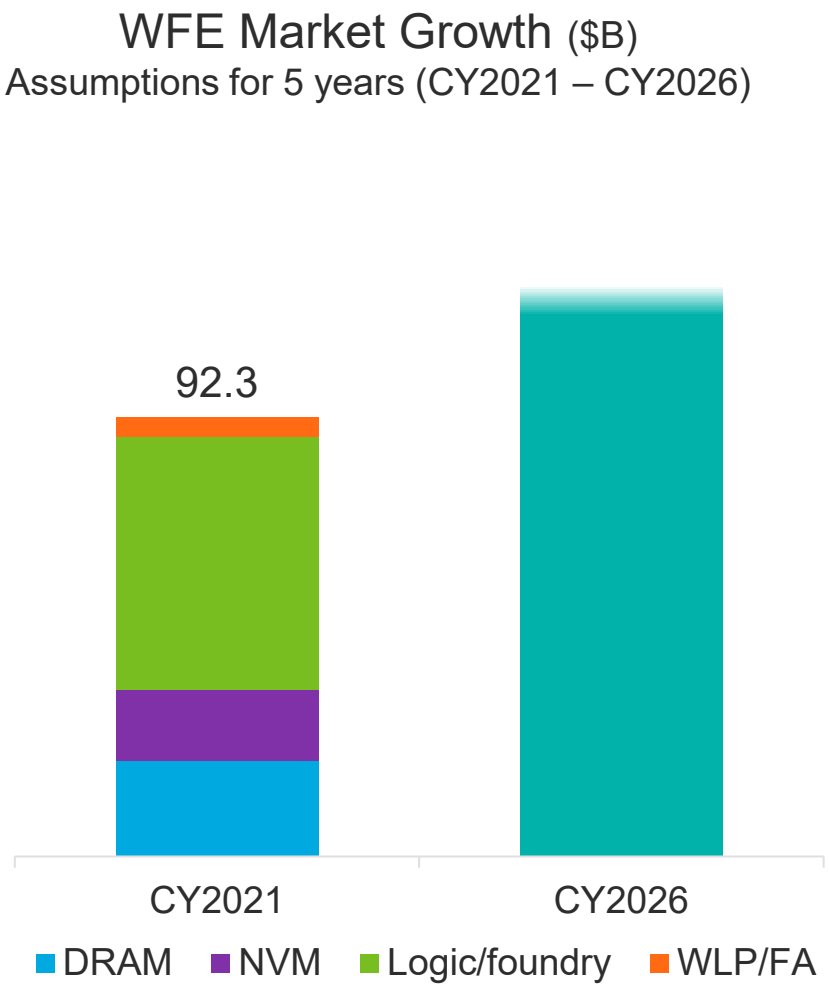
TEL estimates

MOR wet resist process is superior to dry resist process (CVD + dry development) not only in terms of operational advantages including cost, TAT, queue time management, equipment footprint and power consumption, but the wet process also demonstrates superior data in terms of process performance

7. TEL’s strategy

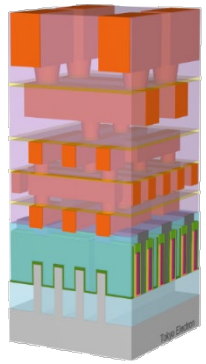
7-1 : SPE Business Initiatives

WFE Market and Technological Requirements by Application

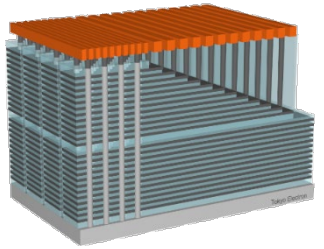


Technological Requirements

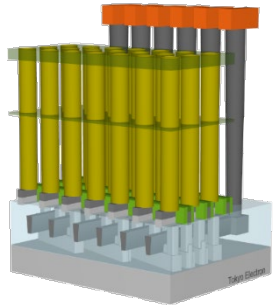
- Logic/foundry：
  - Scaling along with structural changes
    - Reduction in manufacturing cost per transistor
    - Lowering power consumption
    - Higher performance



- NAND
  - Increasing the layer counts
    - Reduction in manufacturing cost per bit

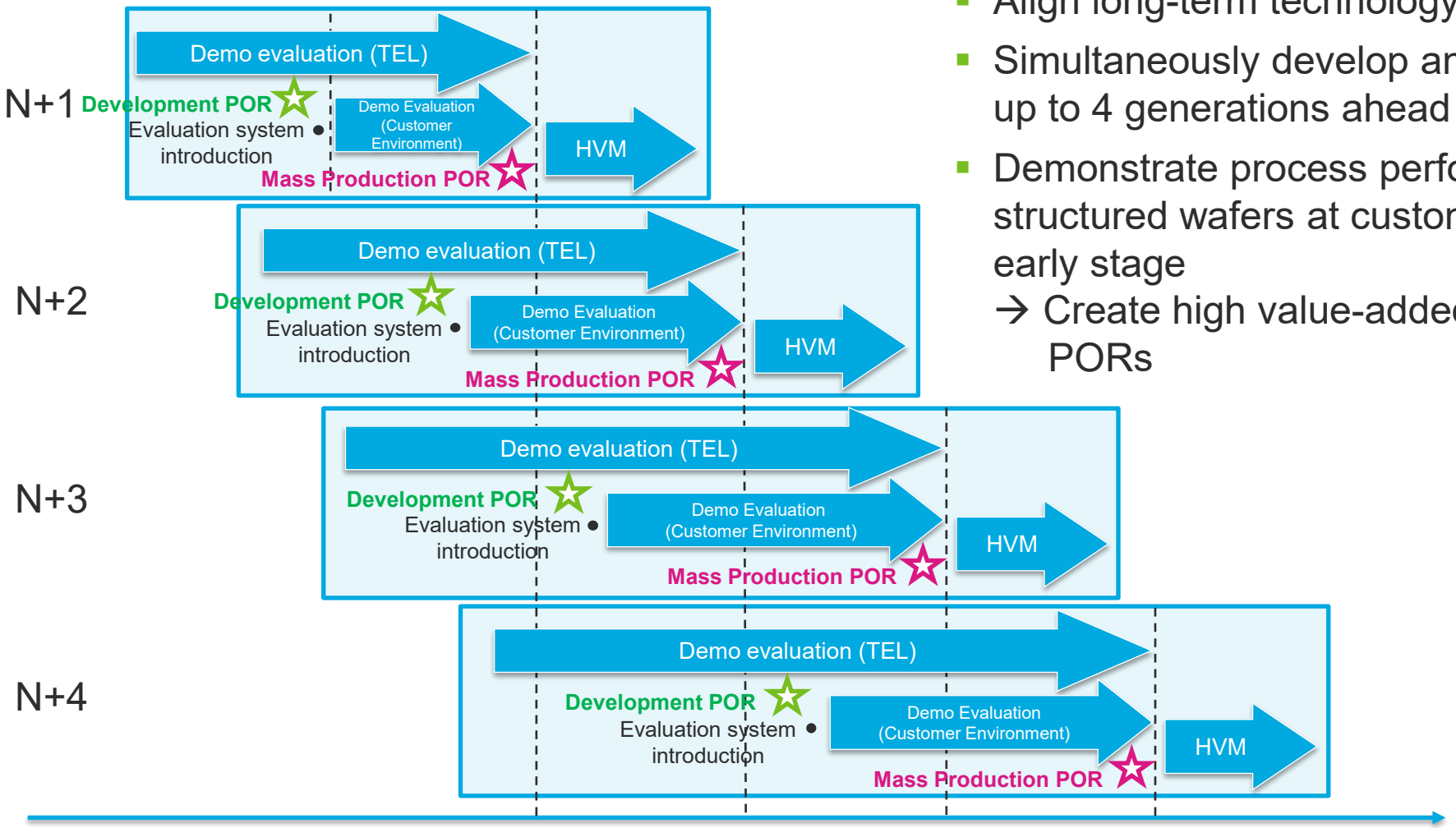


- DRAM
  - Scaling to realize
    - Reduction in manufacturing cost per bit
    - Lowering power consumption
    - Higher performance



Development Efforts

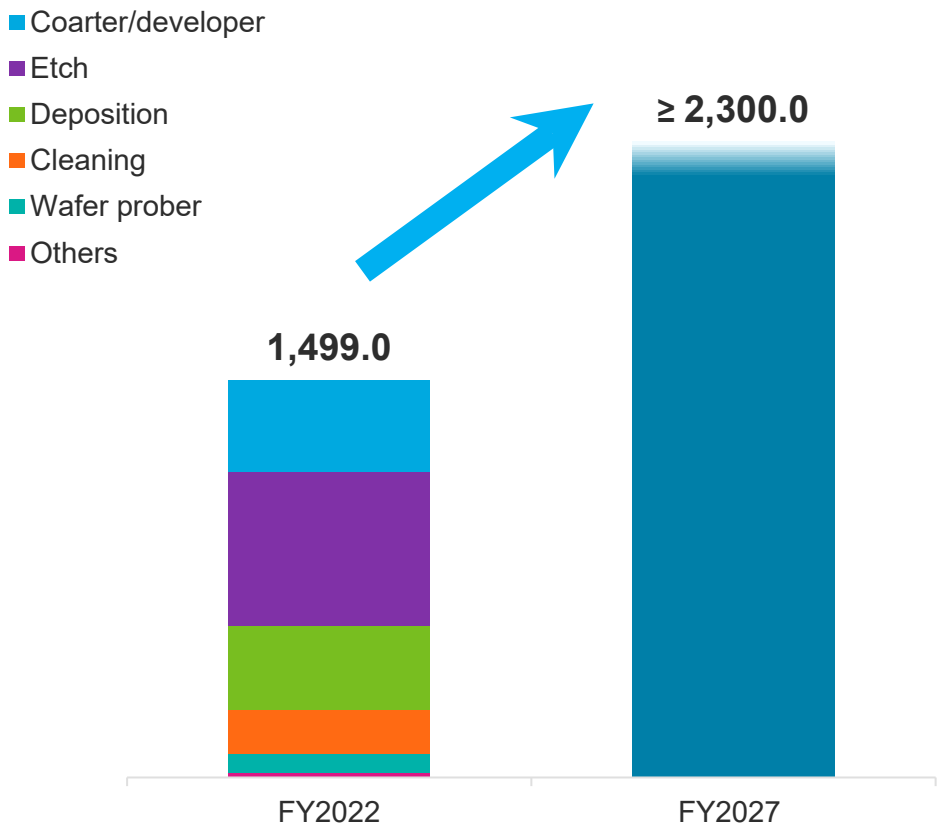
Simultaneous 4-Generation Developments



- Align long-term technology roadmap with customers
- Simultaneously develop and evaluate technologies up to 4 generations ahead
- Demonstrate process performance on customer structured wafers at customer's environments at early stage
  → Create high value-added products and acquire PORs

SPE Segment Sales Target and Business Opportunities

SPE New Equipment Sales Target ($B)
Assumptions for 5 years (FY2022 – FY2027)

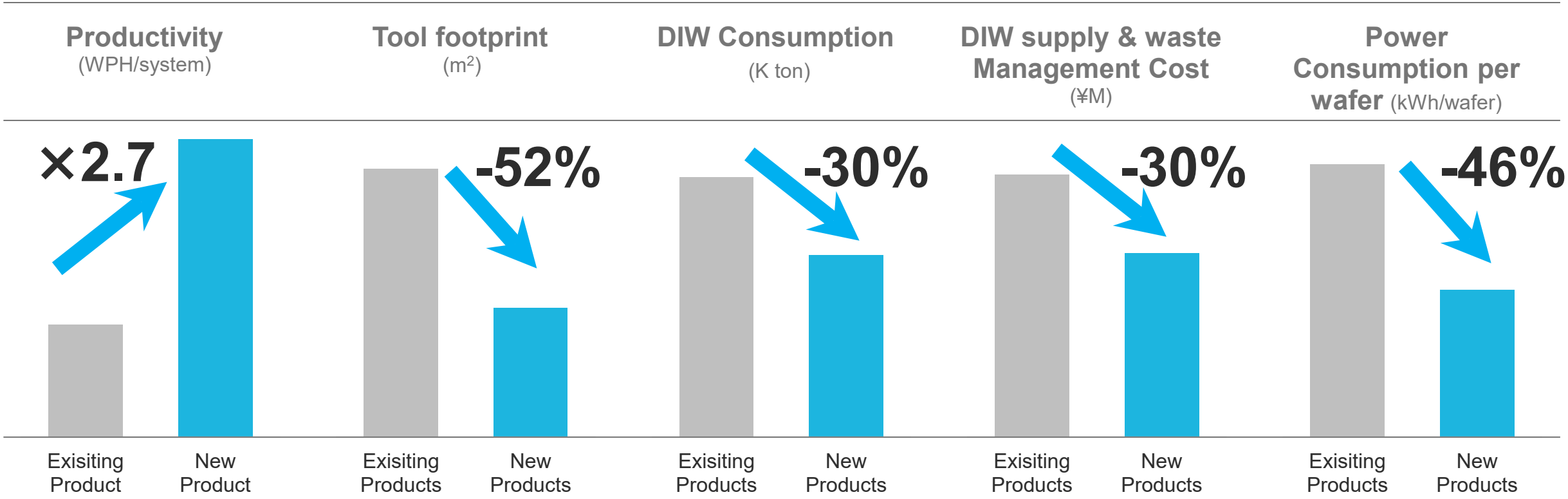


Business Opportunities

- Logic/foundry
  - Increase patterning complexity requires co-optimization between unit processes
  - Adoption of High-NA EUV lithography
  - Adoption of GAA and backside PDN
- NAND
  - 3D NAND layer counts reach more than 300 layers
  - High aspect ratio etch, high productivity sacrificial film removal and atomic-level deposition on 3D structure
- DRAM
  - Technology to suppress RC delay in wiring
  - Capacitor formation technology for further scaling

Increase Environmental Performance

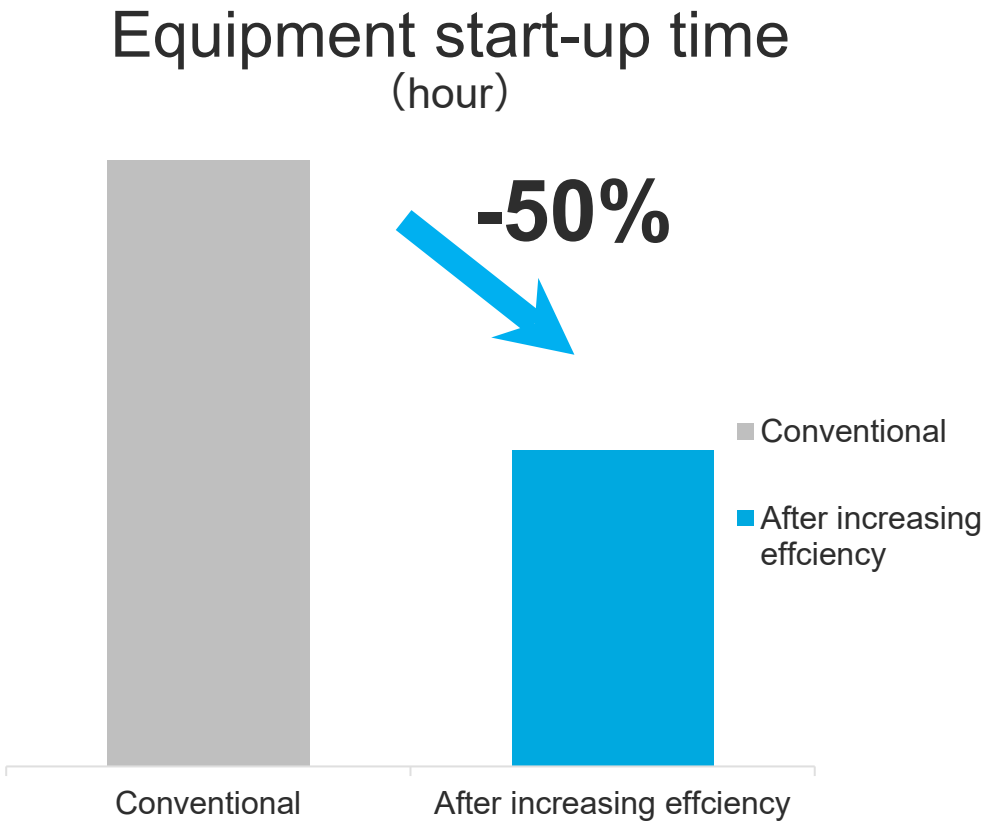
Cleaning system



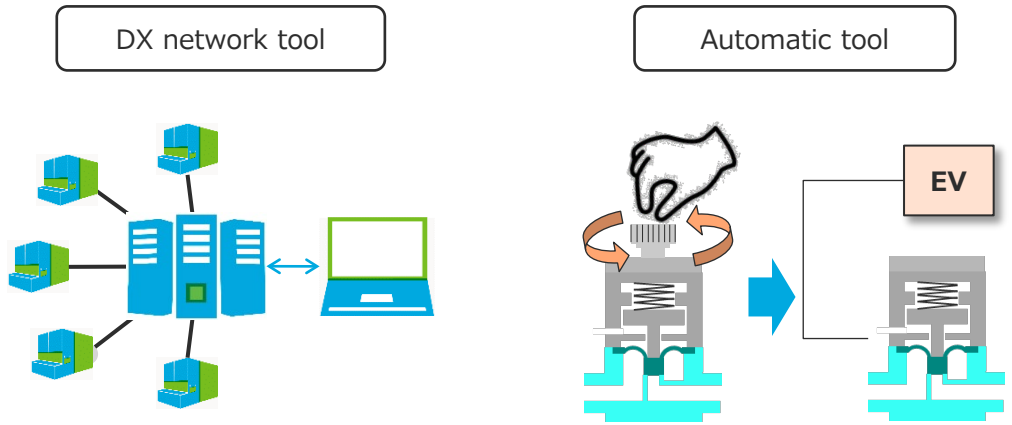
Environmental performance = equipment performance

Further enhance environmental performance

Increase Efficiency of Equipment Start-up



- Measures：
  - Optimize inspection items and automate inspection
  - Expand online support
  - DX network tool
  - Automatic tool

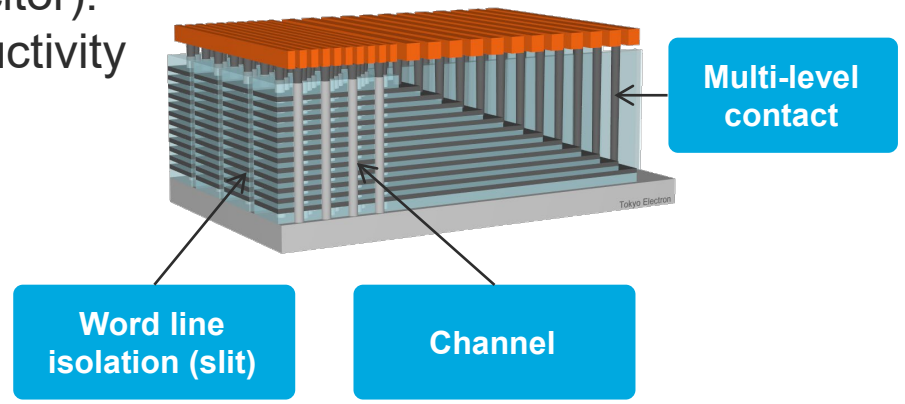


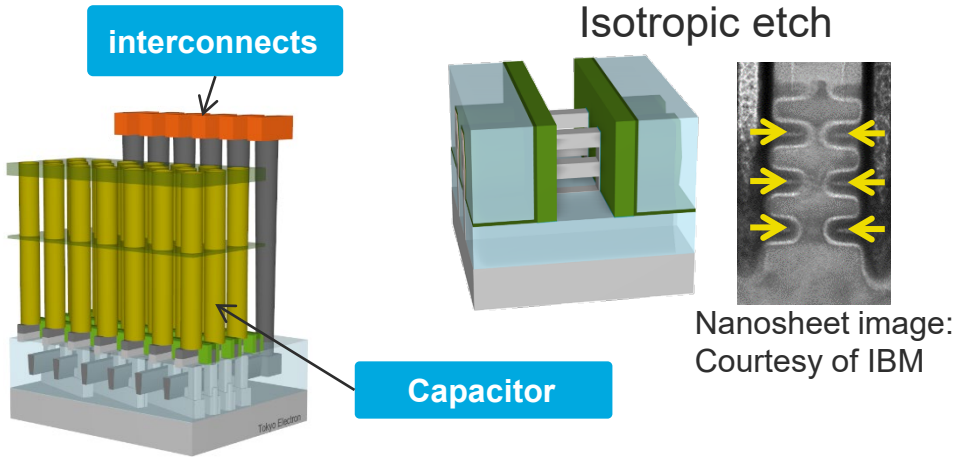
Further enhance customer satisfaction and productivity

7-2 : Etch System

Etch System Strategy

- HARC process
  - 3D NAND (multi-level contact, word line isolation), DRAM (capacitor): Continue to differentiate through process performance and productivity
  - 3D NAND (channel): Launch new systems that can differentiate by providing both precise process controllability and even higher productivity
- Patterning process
  - DRAM: Differentiate with reduced manufacturing costs for customers through process control and combining etch steps
  - Logic: Differentiate through integration of etch and deposition technologies
- Interconnect/contact process
  - Apply knowledge cultivated in logic to DRAM
- Gas chemical etch process
  - Create a new market through plasma assist technology

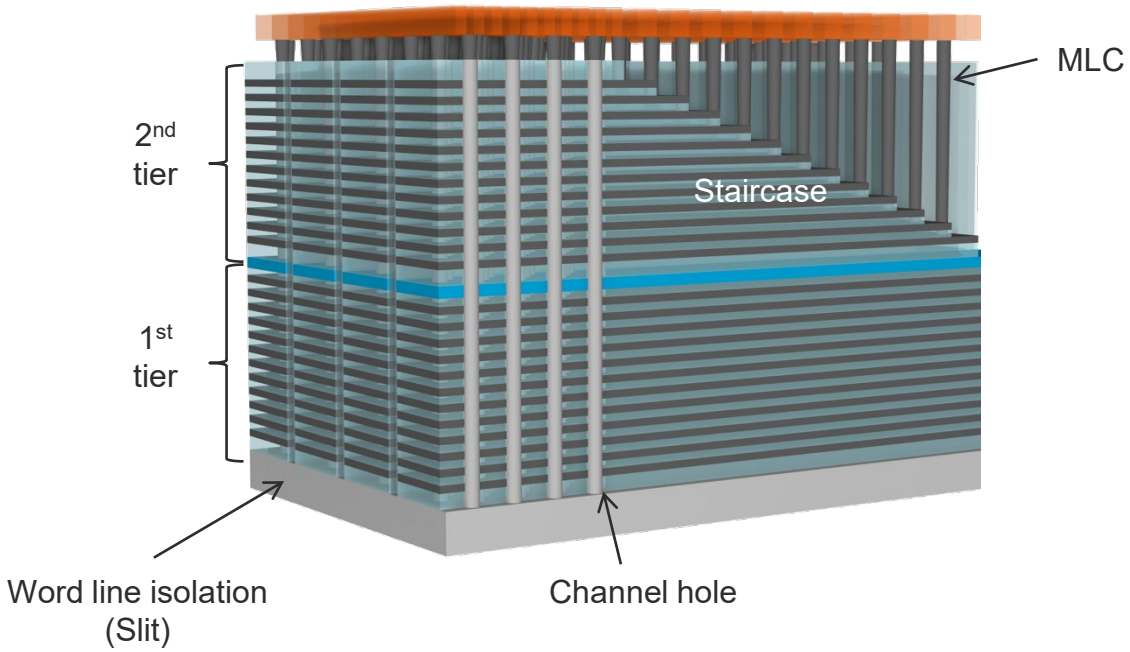




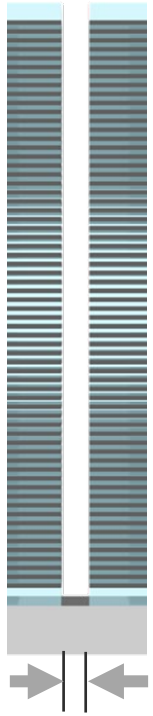
Source: N. Loubet, *et al.*, Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET

Business Opportunities in Memory

3D NAND

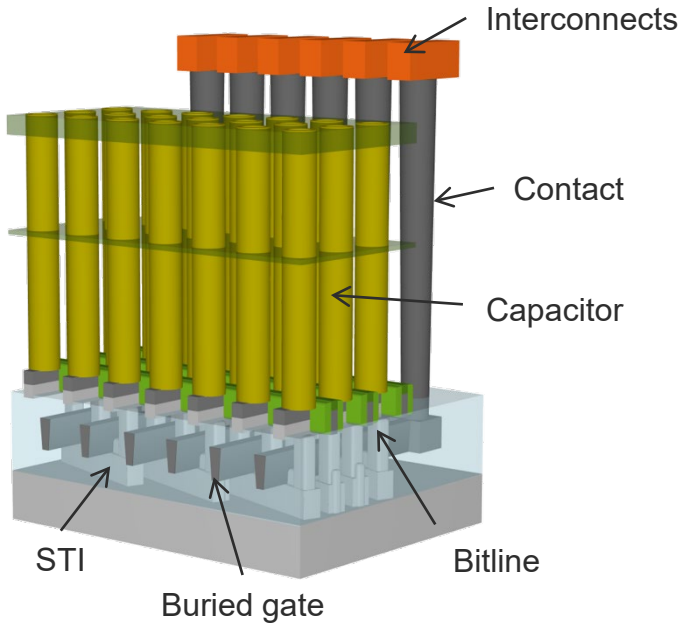


Aspect ratio 70:1



Diameter 100 nm

DRAM

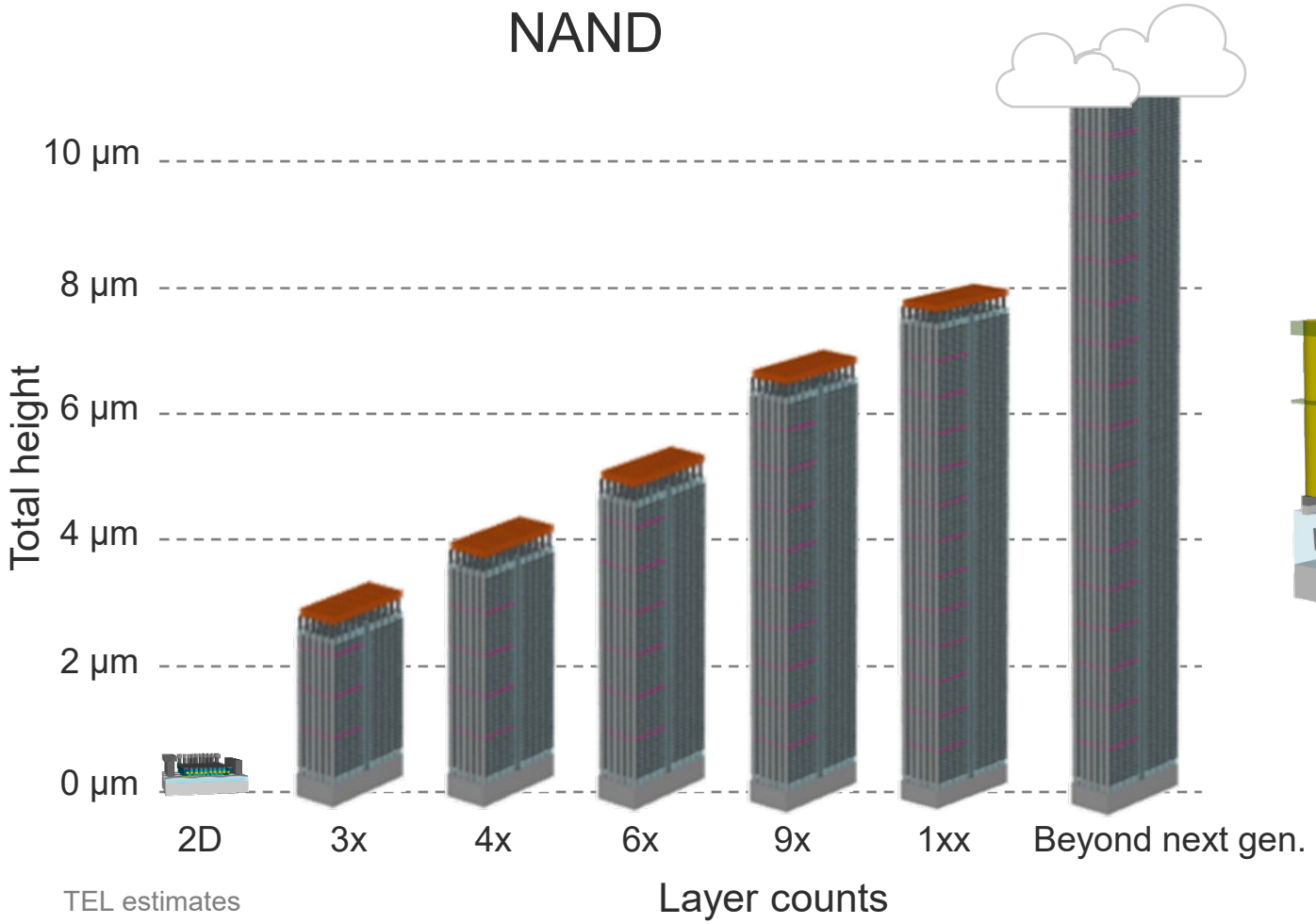


Respond to growing dry etch business opportunities in NAND/DRAM

- Etch performance that corresponds with higher aspect ratios
- Contribution to improvement of customers' productivity

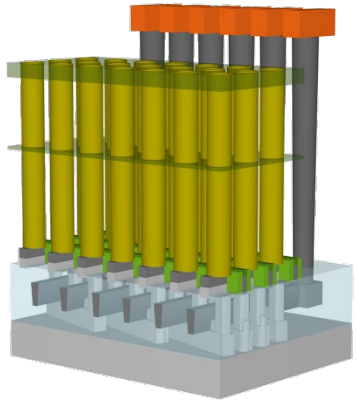
Multi-layering in Memory

NAND

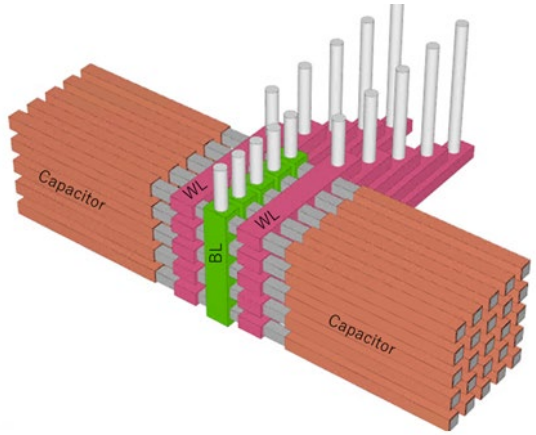


TEL estimates

DRAM



New structure



Etch market growing due to continuing 3D multi-layering

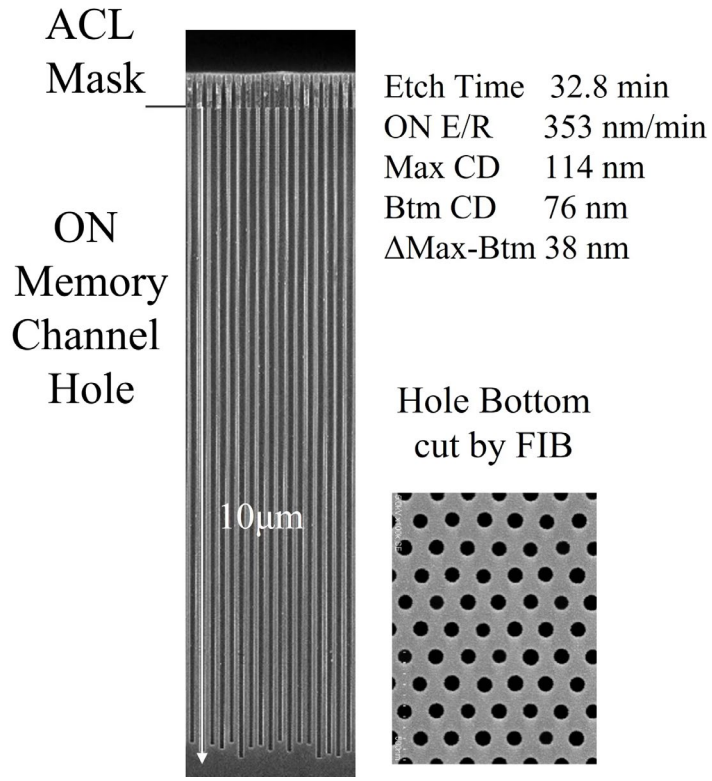
Approach for 3D NAND Channel Hole Etch Process

Channel Hole Etch Process Challenges:

- Realizing deep hole etching with even higher aspect ratio
- Environmental load of the existing process

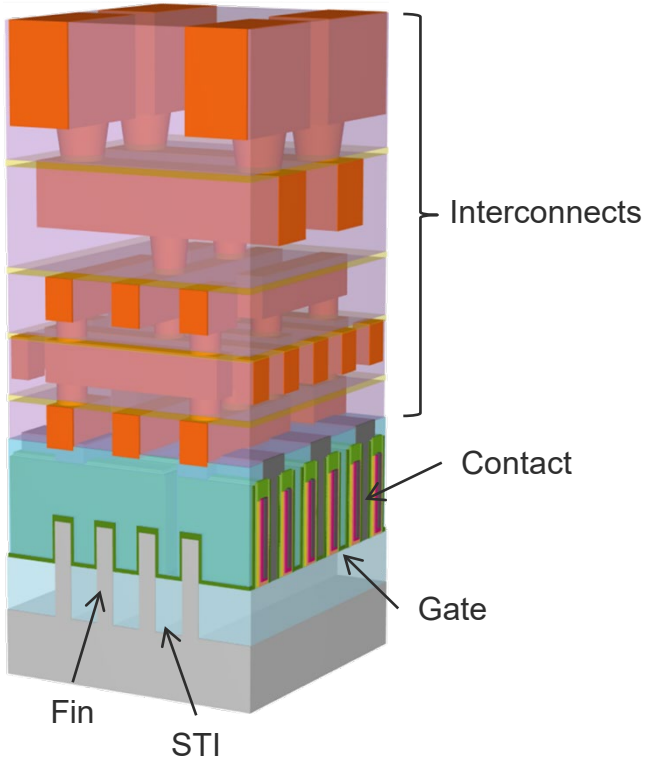
TEL's approach: Novel Cryogenic Etch Process

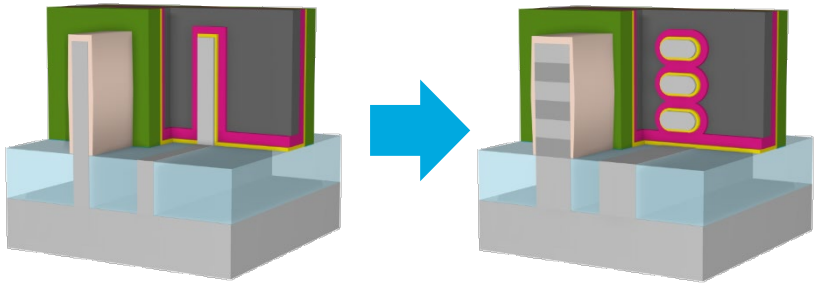
- Achieved 10-μm-deep etch
- 2.5x faster etch rate than previous technologies
- Reduction of the global warming potential by 84%



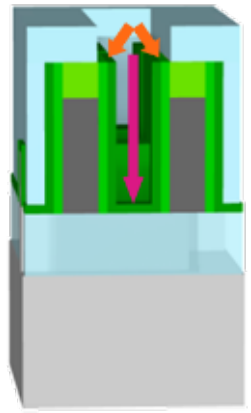
- Achieved etch depth of 10 μm in 33 minutes

Business Opportunities in Logic

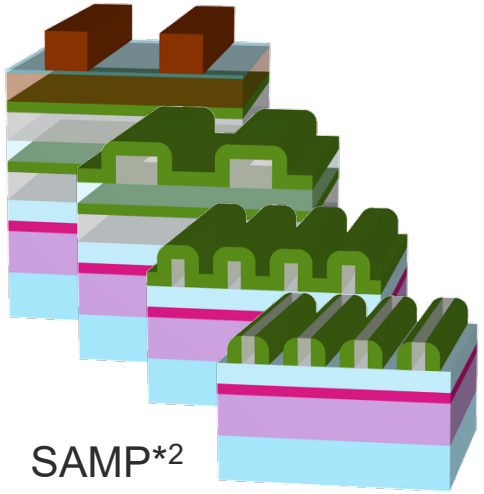




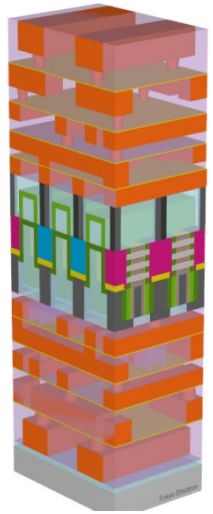
FinFET　　GAA*1 Nanosheet



Self-aligned Contact



SAMP*2



Backside PDN*3

*1 GAA: Gate all around
*2 SAMP: Self-aligned multiple patterning
*3 PDN: Power delivery network

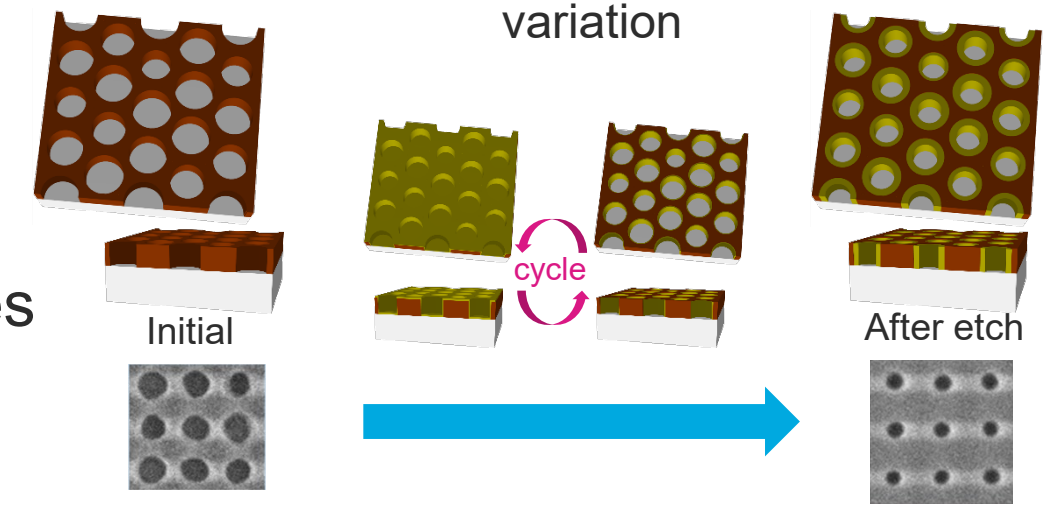
Respond to changes in device manufacturing and EUV lithography for further scaling

Etch Solution toward EUV Lithography

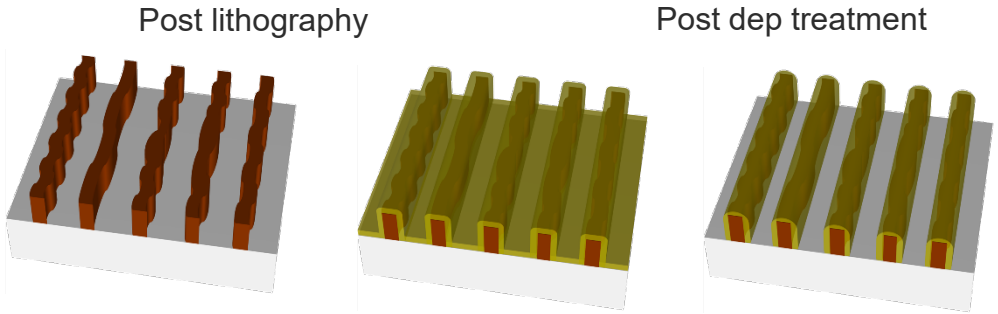
TEL's initiatives

- Improve post-lithography variation by repeating deposition and etch processes
- Improve mask selectivity by leaving film on resist
- Leverage collaborations with imec and ASML and realize patterning solutions for high NA generation

Combining deposition and etch to improve variation



Improved selectivity by deposition on resist followed by plasma treatment

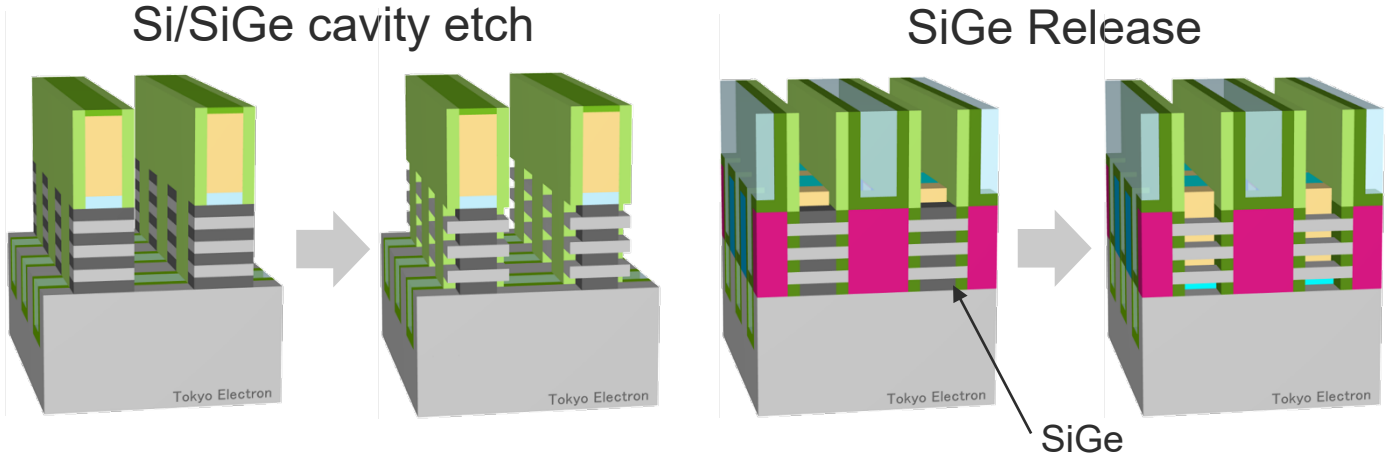


Combining deposition and etching to improve variation and etch selectivity

Initiative for GAA Nano Sheet Structures

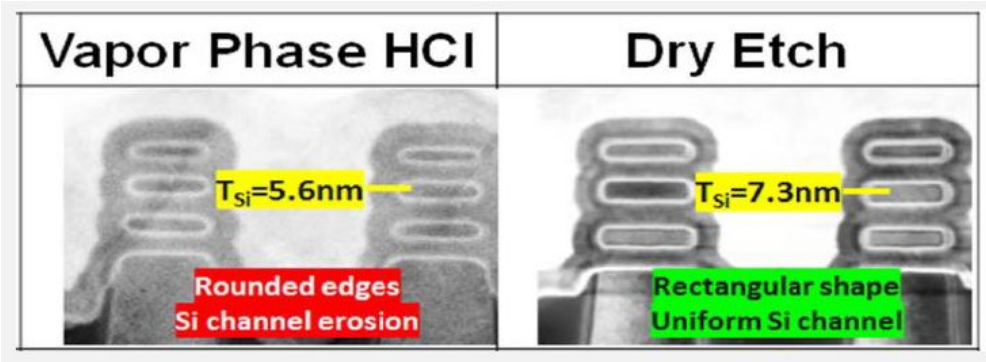
Nano Sheet process challenges:

- Uniformity in rectangle shape
- Mitigation of roughness/residue on patterned surface



TEL's initiative: Gas chemical etch

- High etch selectivity
- High uniformity
- Residue removal/decreased roughness



Source: N. Loubet, et al., IBM, TEL Technology Center, America (IEDM2019)

Leveraging the advantages of gas chemical etch to contribute to leading-edge processes

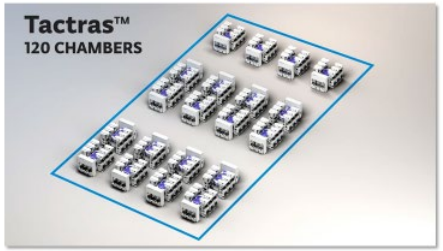
Episode™ UL

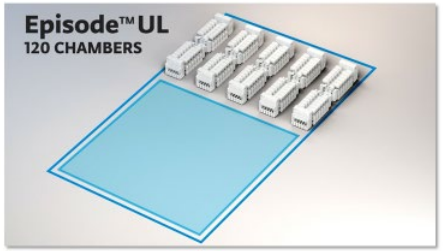
Episode™ UL Features

Flexible layout available to accommodate needs
Improved productivity through space saving and smart tools

TEL

Episode™ UL: Space

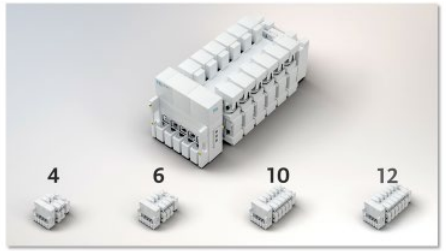




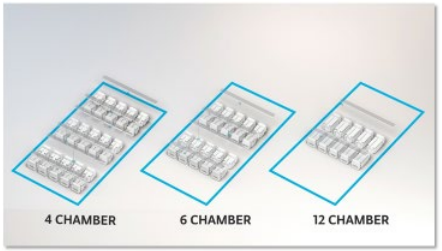
Significantly reduced footprint per chamber

TEL

Episode™ UL: Layout



Select from 4 options
4, 6, 10, and 12 chamber designs



Flexible layout available to accommodate
fab space and target processes

TEL

Episode™ UL: Smart Tools

Includes automated parts exchange functions, multiple sensors and a high-speed control system
Autonomous process control possible through big data analysis using TEL's own smart tools

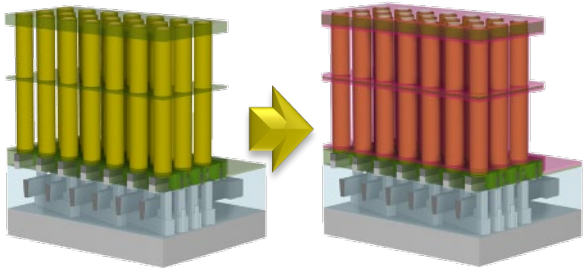
TEL

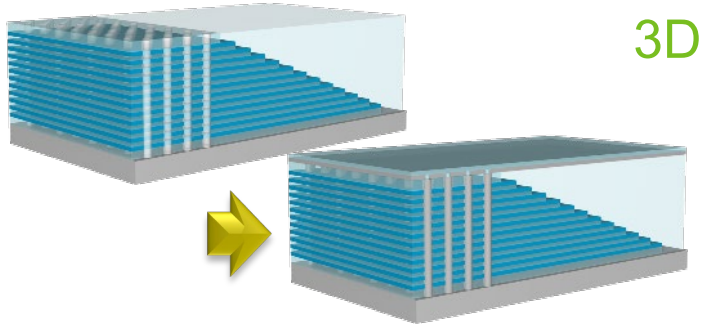
7-3：Deposition System

Deposition Business Strategy

DRAM

- Lower temperatures
- High-k dielectric film
- Capacitor electrode



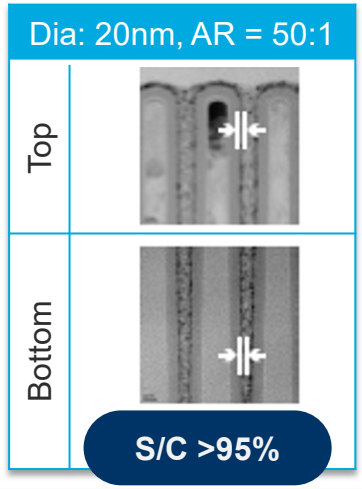


3D NAND

- Channel silicon film
- Charge trap film
- Block high-k dielectric film
- Buried oxide film
- Buried silicon film

Single-wafer System

Triase^{+}™ EX-II Pro™ TiN



Vertical Furnace

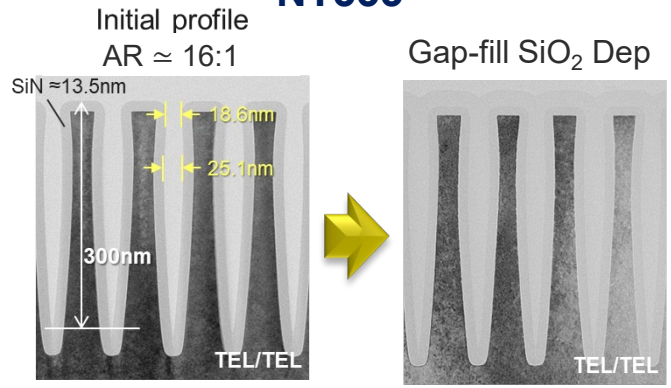
TELINDY PLUS™ Super Large Batch

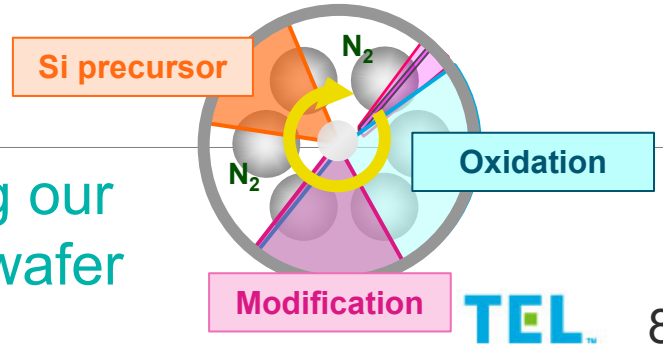
100/125

150/175

Semi-batch System

NT333™

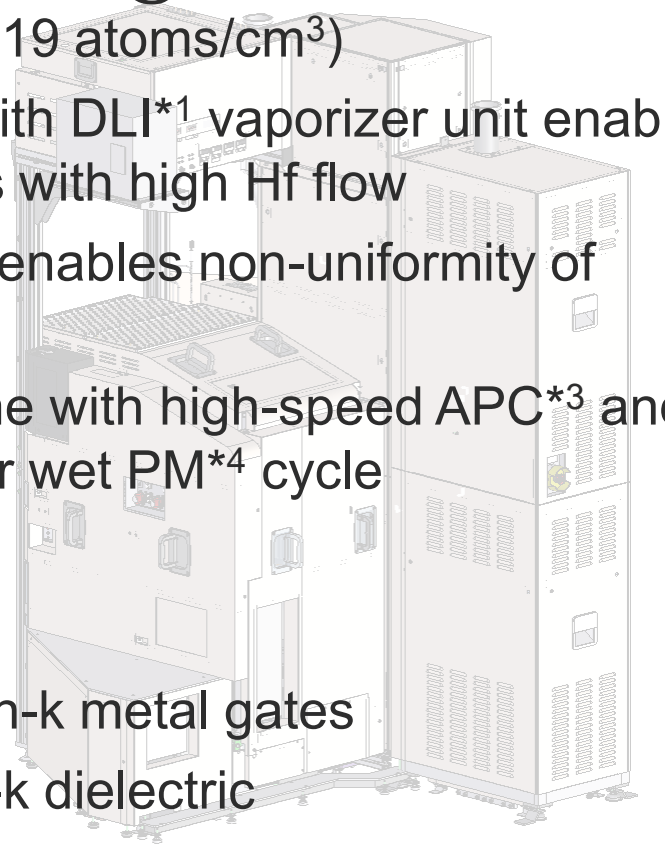




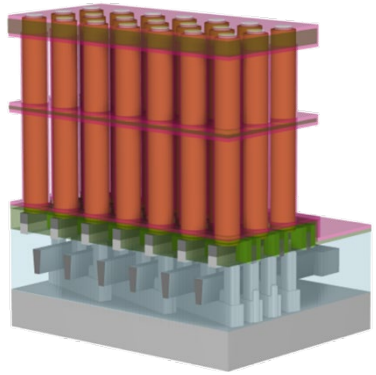
Provide high value-added technology by leveraging our advantage of having batch, semi-batch and single wafer technologies

Triase^{+}™ EX-II™ HK: High Quality High-k Dielectric

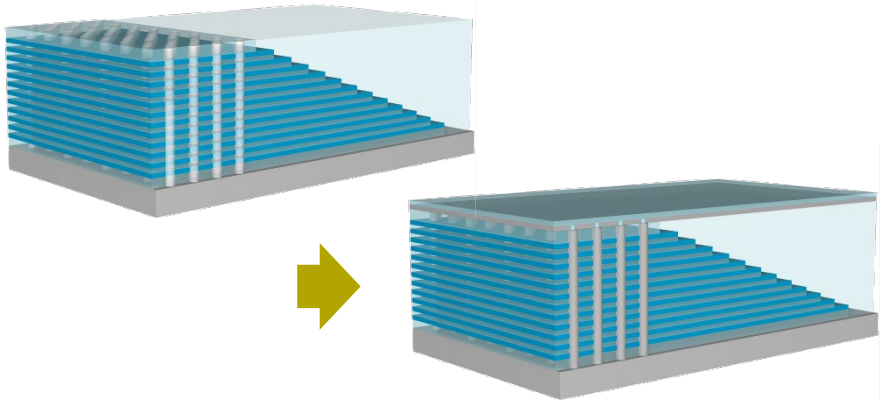
- Features
  - Designed for HfO process @ ~400℃ and ultra low carbon (~1E19 atoms/cm^3)
  - Liquid Hf precursor with DLI*1 vaporizer unit enables ideal ASFD*2 process with high Hf flow
  - Unique gas insertion enables non-uniformity of < 1% within wafer
  - Enhanced exhaust line with high-speed APC*3 and 100A piping for longer wet PM*4 cycle
- Applications
  - DRAM peripheral high-k metal gates
  - 3D NAND block high-k dielectric



DRAM High-k dielectric



3D NAND Block high-k ~ core oxide dep



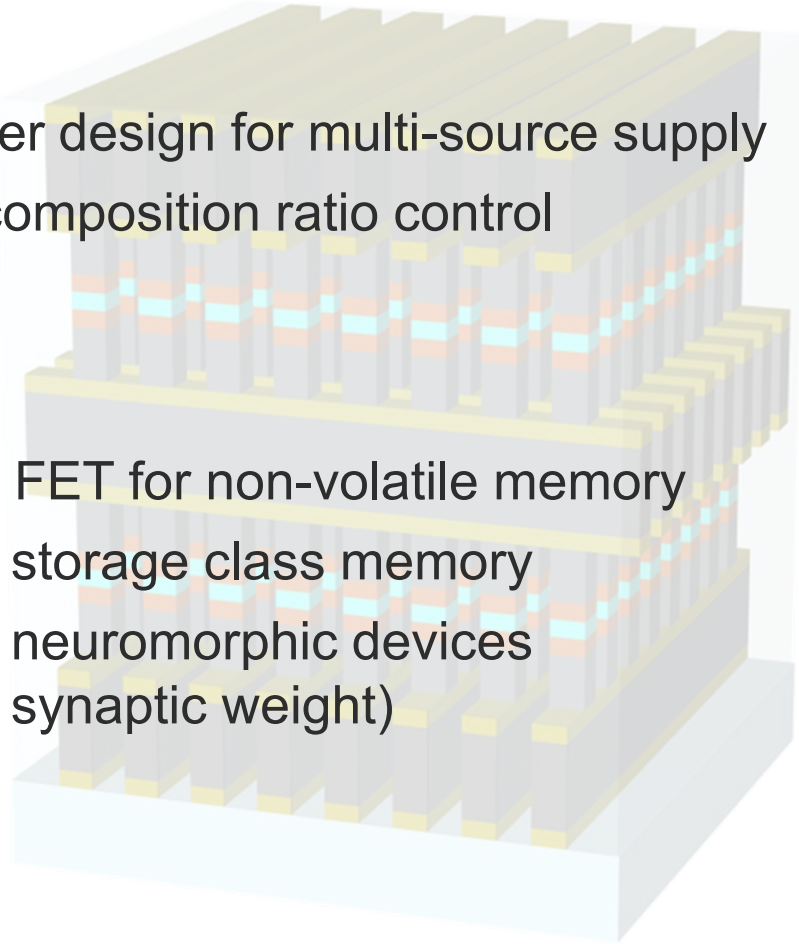
*1 DLI: Direct liquid injection
*2 ASFD: Advanced sequential flow deposition
*3 APC: Auto pressure control valve
*4 PM: Preventative maintenance

Triase^{+}™ EX-II™ MS: Multi-source Supply for Controllable Film Composition

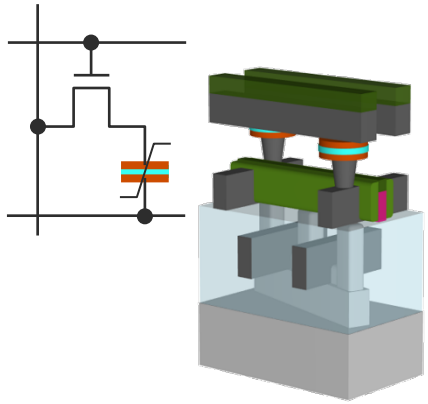
Under development

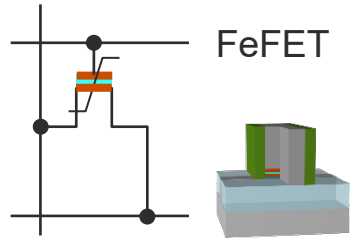
- Features
  - New Chamber design for multi-source supply
  - Capable of composition ratio control

- Applications
  - Ferroelectric FET for non-volatile memory
  - Extension to storage class memory
  - Extension to neuromorphic devices (memorizing synaptic weight)

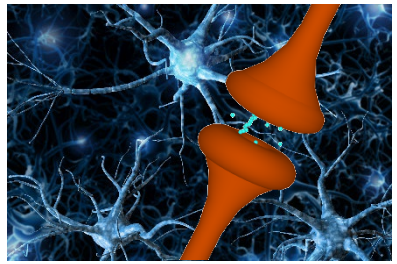


FeRAM

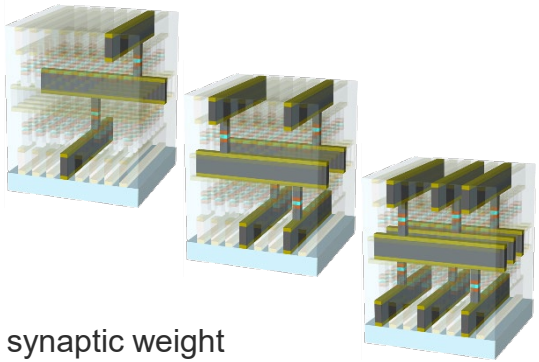




Neuromorphic



Artificial synapse

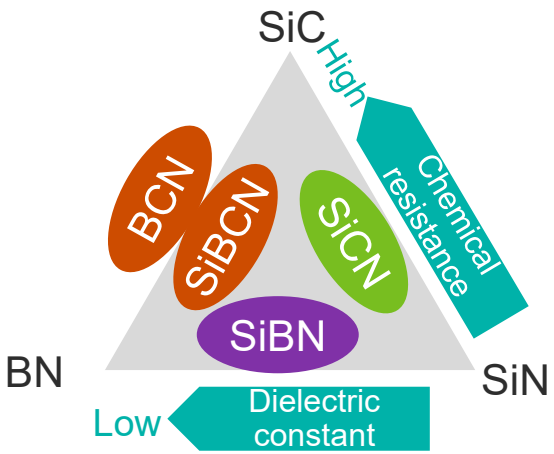


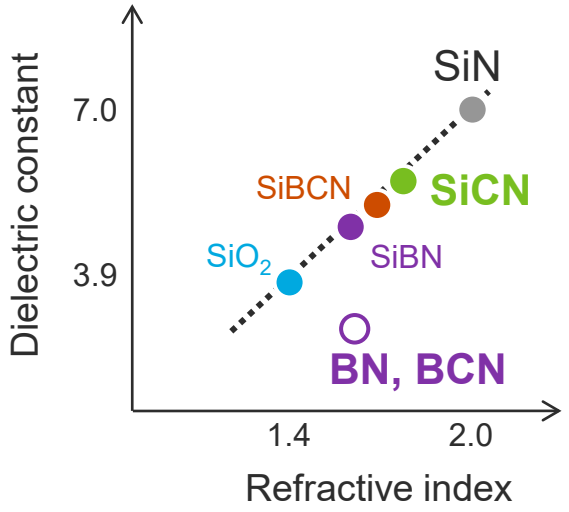
Memorizing synaptic weight

Ultra-thin Film Dielectric Process for Nano Sheet FET

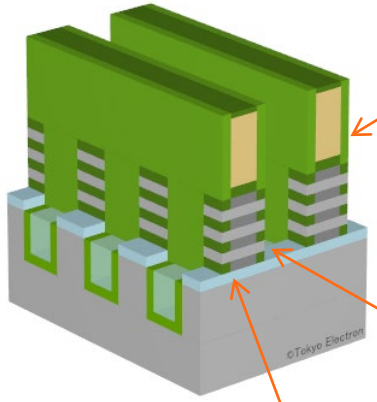
Solution for thin film formation in high aspect ratio narrow spaces

Dielectric characteristics





Ultra-thin film dielectric film deposition for nano sheet



Gate spacer

Insulation between source/drain and gate, control of doping, etc.

Inner spacer

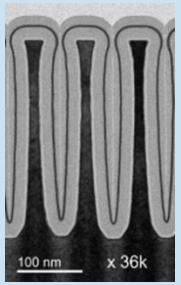
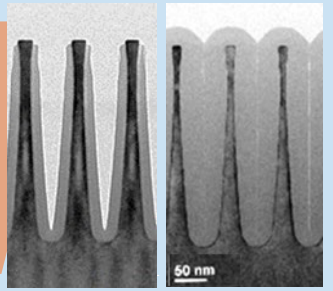
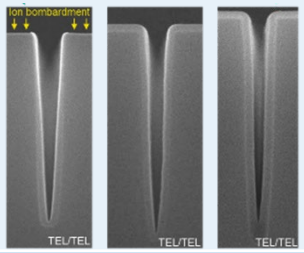
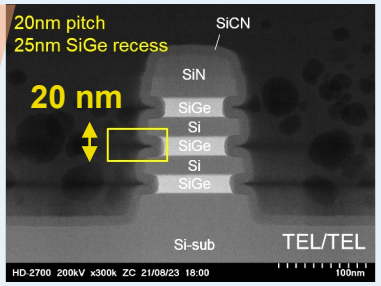
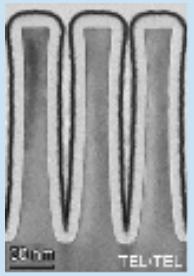
Support sheet with equal interval

Dielectric isolation

Reduce leak currents from Si channel to silicon substrate

Our batch furnaces provide the high quality and ultra-thin dielectric film required in nano sheet formation

Dielectric Film Application Map: Gapfill in Narrow Spaces, Ultra-thin Film Formation

	300 °C	400 °C	500 °C	600 °C
SiN (k ~ 7.5)	Example of dep-etch-dep processes 	Single wafer PECVD (under FS*)	**TELINDY PLUS™ IRad™** Deposition/etch fusion process	
Low-dielectric constant material (k < 4.5)	High H_2 radical Low Example of film formation inhibition technology 	Single wafer PECVD (under FS*)	**TELINDY PLUS™ IRad™** Thickness/film quality/ coverage, integration	
Ultra low-dielectric constant material (k < 3.0)		**TELINDY PLUS™ IRad™** Adoption of new materials (under FS*)		

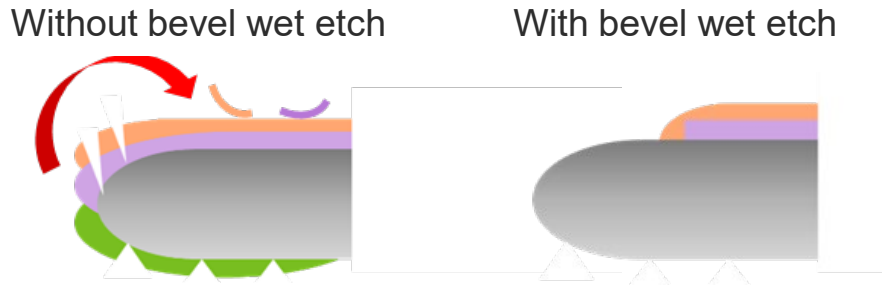
Expanding product lineup for high quality ultra-thin dielectric film

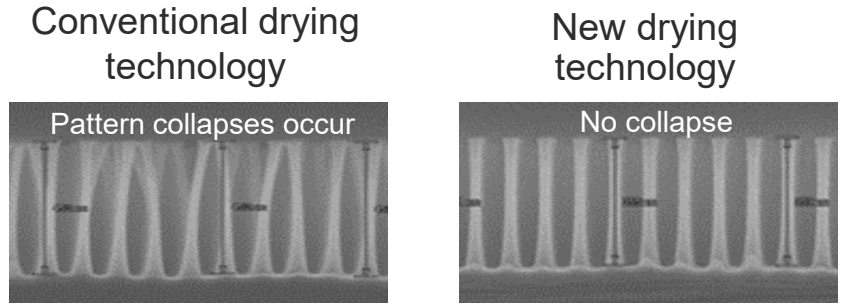
*FS: Feasibility study

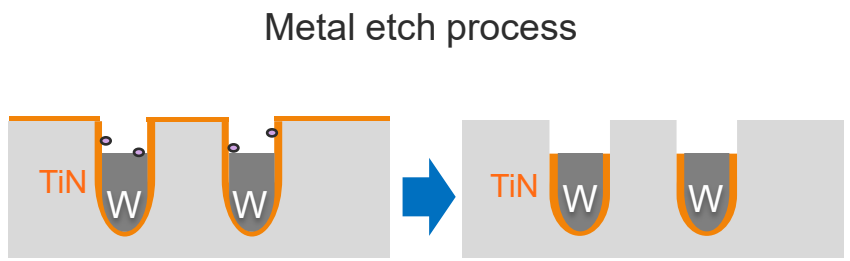
7-4：Cleaning System

Single Wafer Cleaning Strategy

- Single wafer cleaning
  - Bevel wet etch
    - Expect annual market growth rate of around 10%
    - Contribute to improving customers' yields. Maintain a high market share by differentiating through performance in precisely removing film from the outer part of the wafer
  - Prevent pattern collapse
    Expand market share by TEL original technology to reduce collapse of high aspect ratio pattern
  - Metal etch
    Launched new dedicated SPM chambers for controlling selectivity for metal in order to solve reduced yield issues caused by dry etch damage and residue





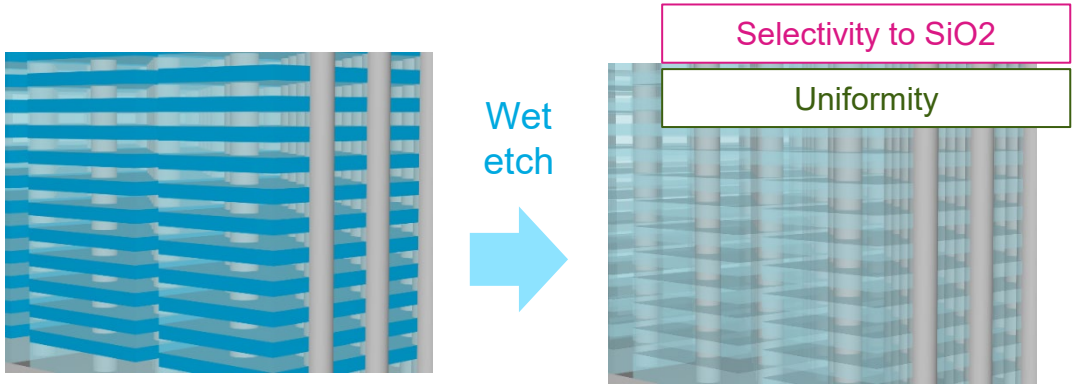


Batch and Scrubber Cleaning Strategy

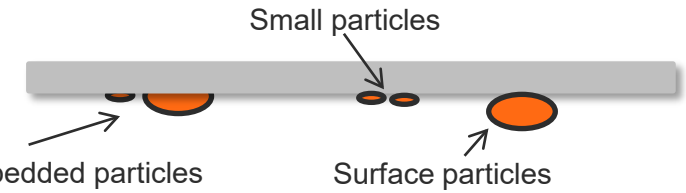
- Batch cleaning
  - SiN etch and W etch processes for 3D NAND
    Focus on processes that require long durations and advanced process technology. Differentiate by realizing high uniformity, high selectivity and high productivity in wet etch

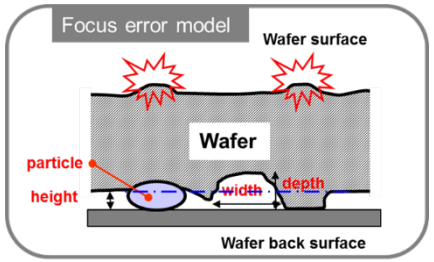
- Scrubber cleaning
  - Pre-lithography process
    Provide high-value solutions such as reducing particles brought in by wafers, contributing to the improvement of exposure tool availability which have grown increasingly important due to the introduction of EUV

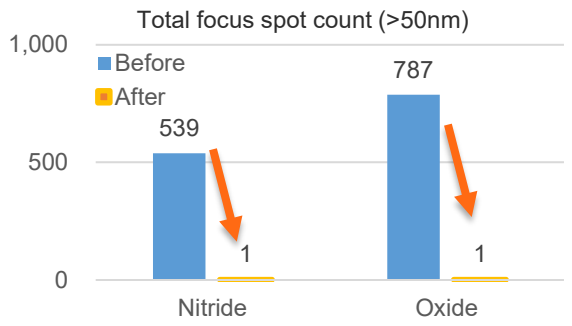
SiN etch process



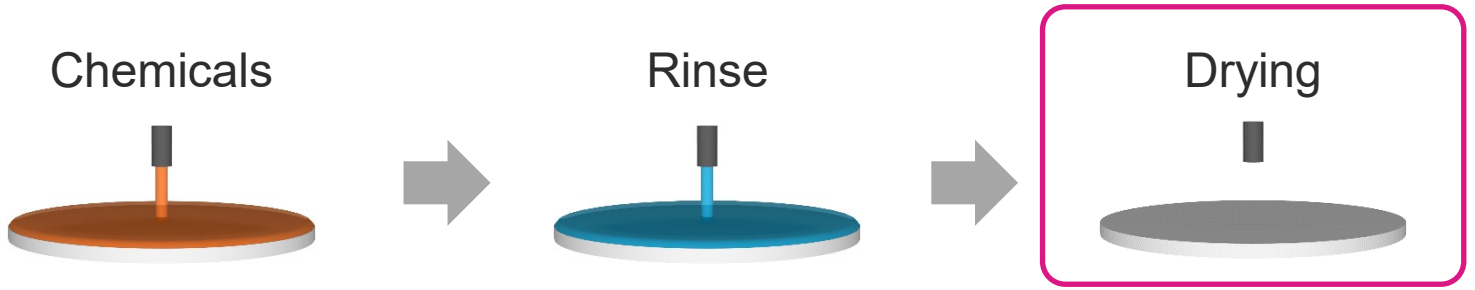
Wafer back and defocus diagram



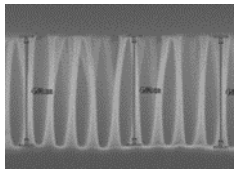




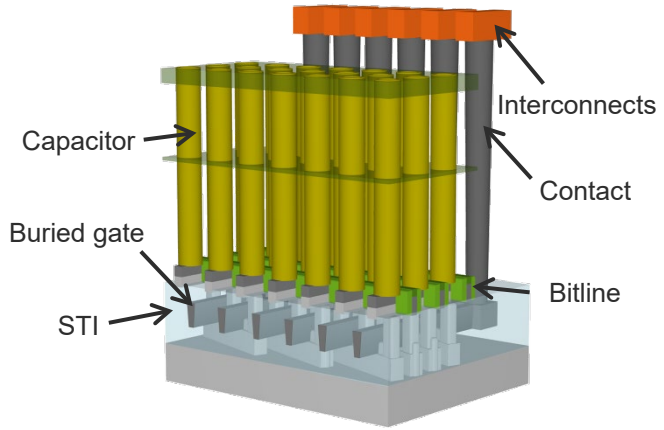
Technology Challenges in Cleaning for State-of-the-Art Devices



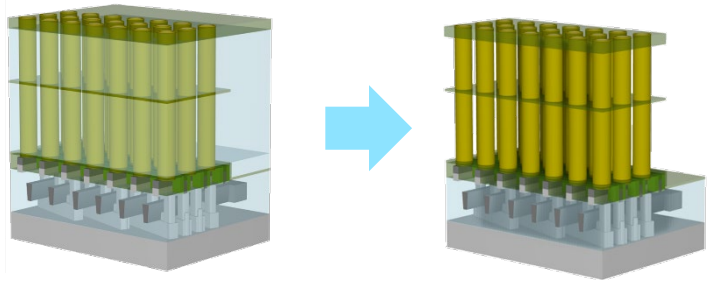
Pattern collapse



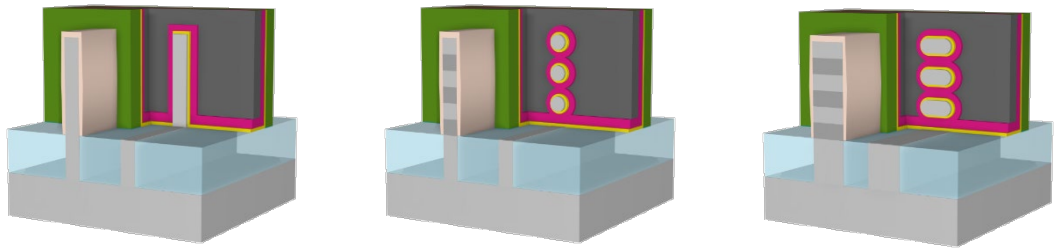
- DRAM
  - Post-STI etch cleaning
  - Mold wet etch after capacitor electrode formation



Wet etch



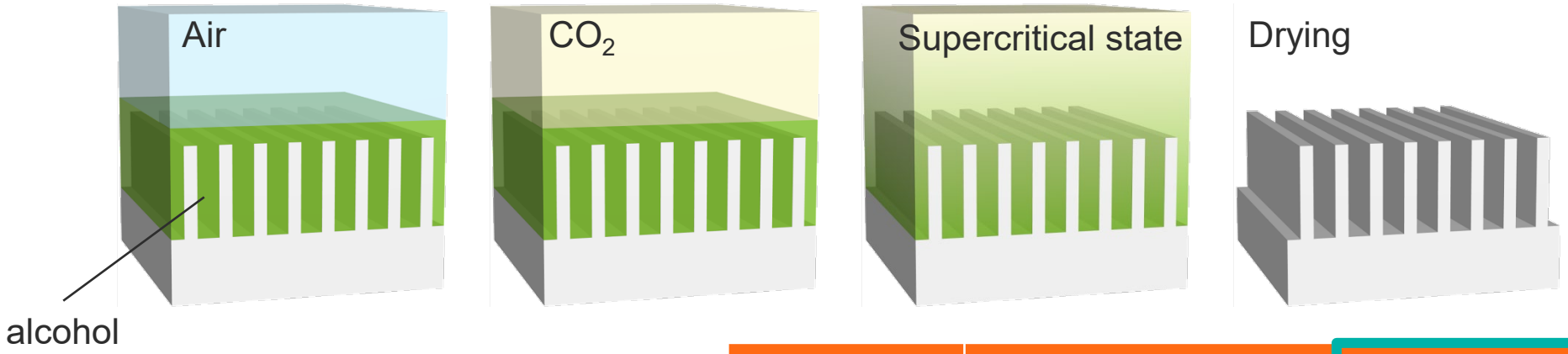
- Logic
  - Post-fin etch cleaning
  - Post-nanowire/nanosheet formation cleaning

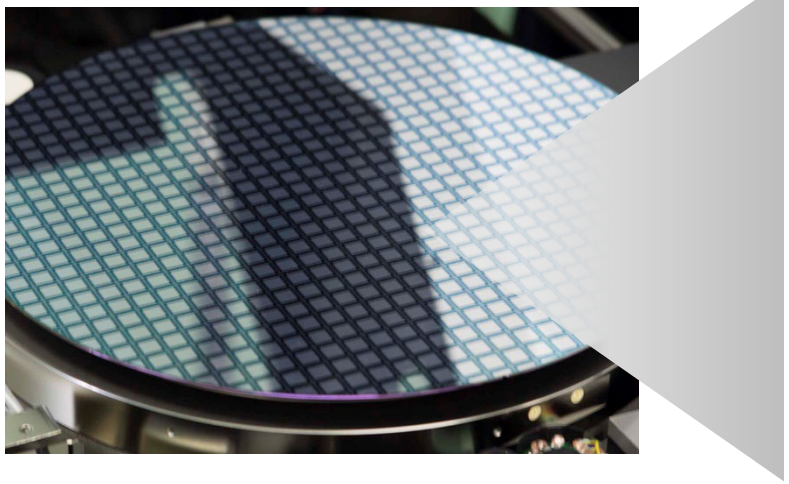


FinFET | Nanowire | Nanosheet

Drying technology more difficult due to further scaling and higher aspect ratios in device manufacturing

Supercritical Drying Technology

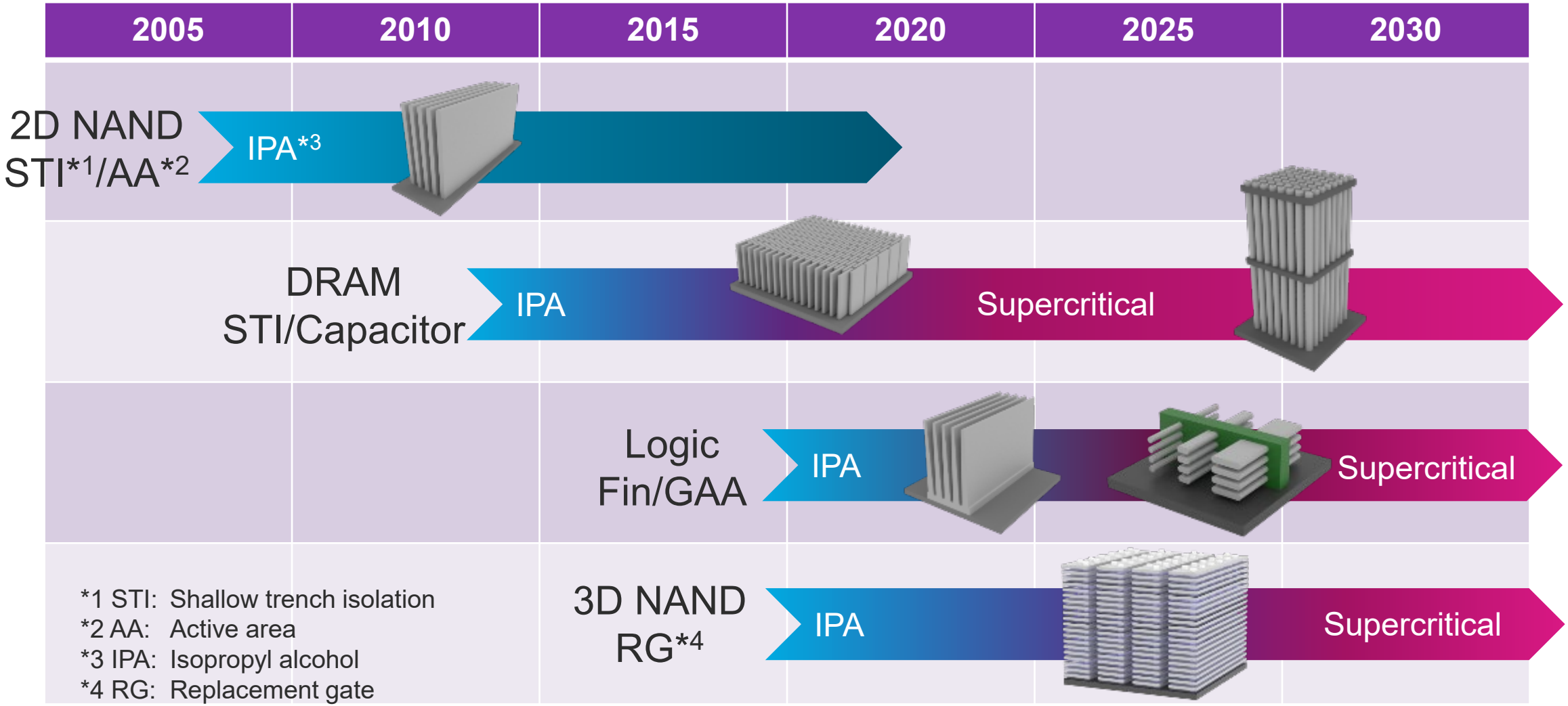




	Traditional drying	TEL's supercritical drying
Top View		
Side View		

Supercritical drying technology prevents pattern collapse

Drying Technology Roadmap

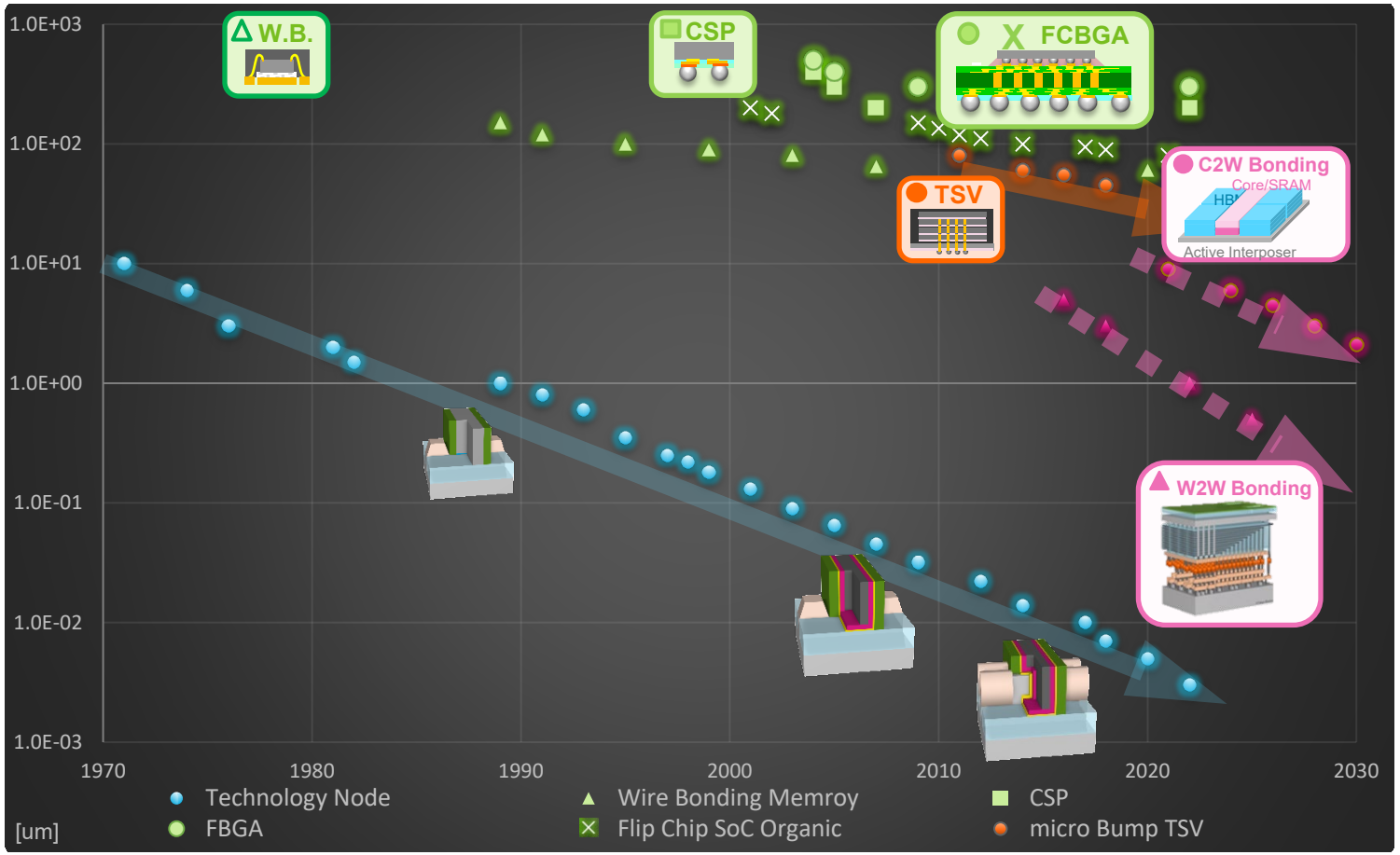


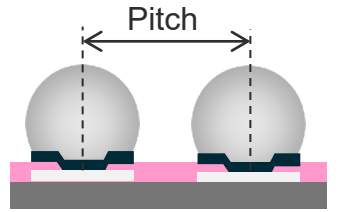
*1 STI: Shallow trench isolation
*2 AA: Active area
*3 IPA: Isopropyl alcohol
*4 RG: Replacement gate

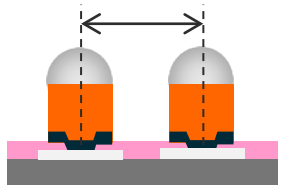
7-5 : Backend Business Strategy

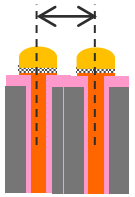
Activities for the Development of Wafer Bonding Process

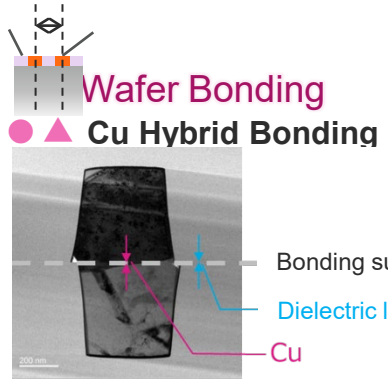
Semiconductor Technology Node and Bump Pitch





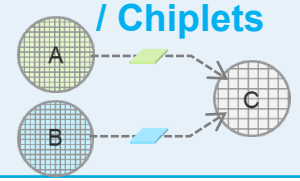
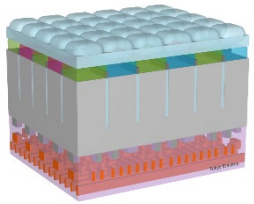
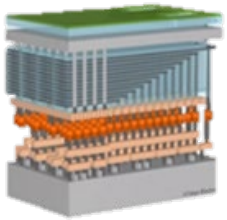
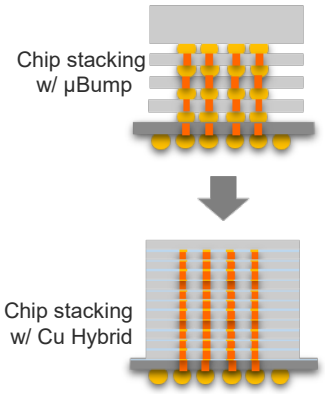
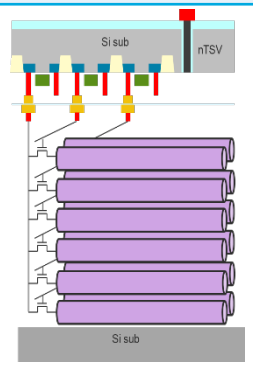
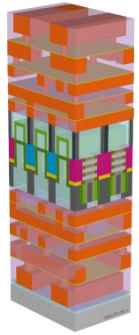
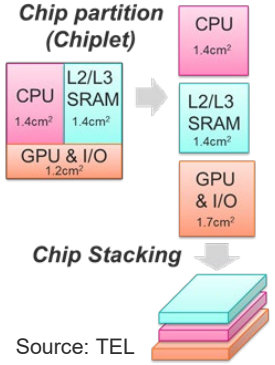






Introduction of wafer bonding technology accelerates further reduction of pitch

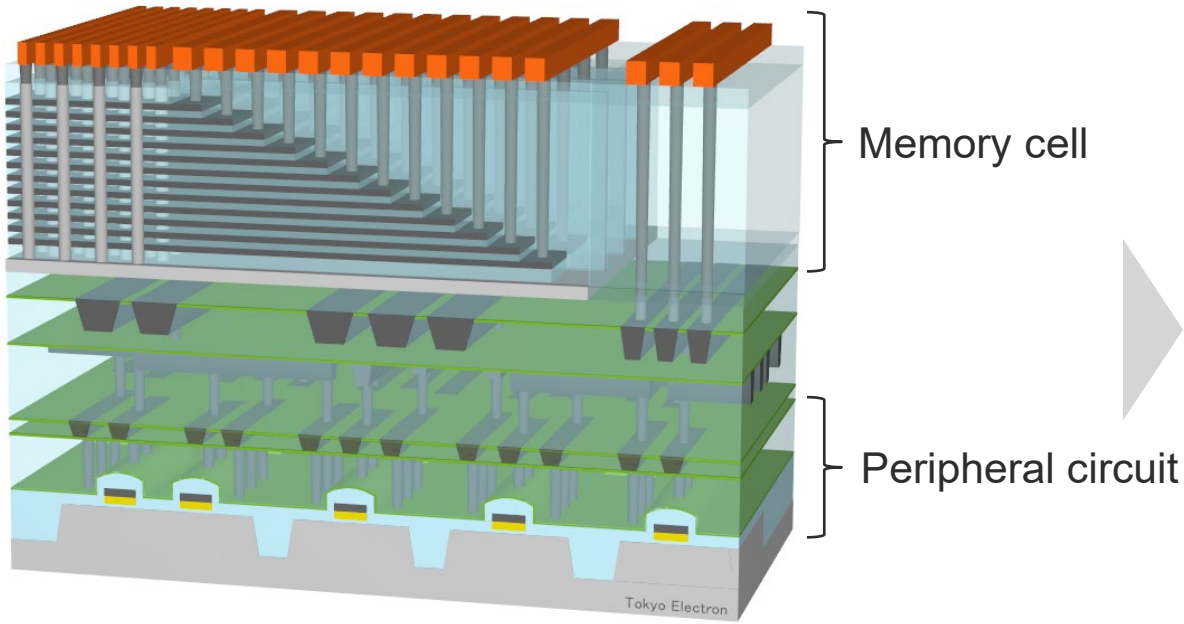
Application of Wafer Bonding

Device	CIS	NAND	DRAM		Logic		
	BSI	3D NAND	HBM	3D DRAM	Backside PDN	Sequential CFET	Disaggregation / Chiplets
Stacking Device	Sensor + (Memory) + Logic	Cell + Peripheral	DRAM (⇄) ⋮ DRAM (⇄) + Logic	Cell + Peripheral	Logic + Bare Si	Logic + Logic	
Bonding	W-W Cu Hybrid	W-W Cu Hybrid	D-W Cu Hybrid	W-W Cu Hybrid	W-W Ox Fusion	W-W Ox Fusion	D-W / D-D Cu Hybrid
3D I/O Pitch	3 μm →1 μm	1 μm →0.5 μm	40 μm →25 μm	1 μm →0.5 μm	Sub μm (nTSV)	Sub μm (nTSV)	10 μm →1 μm
Structure				 Source: TEL 3D DRAM structure			 Source: TEL
Status	HVM	R&D~HVM	R&D	R&D	R&D	R&D	R&D

Expanding adoption of wafer bonding technology for next-generation devices

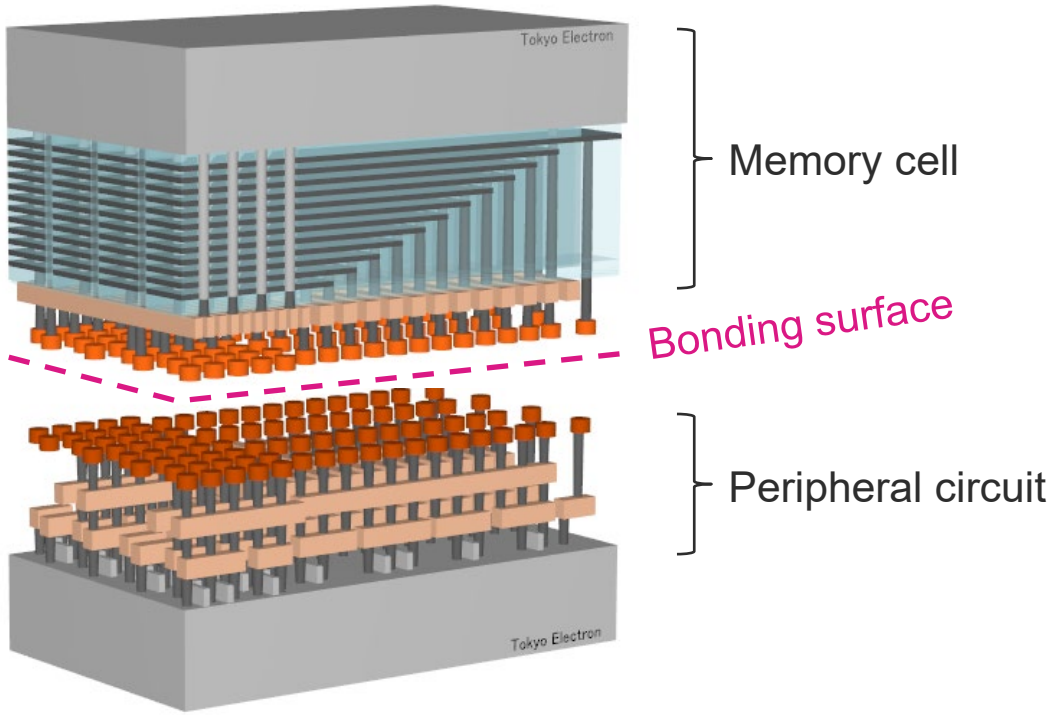
Wafer Bonding Application for 3D NAND

Current structure



- ✓ Peripheral circuit performance deteriorates due to exposure to high temperature during memory cell manufacturing
- ✓ Long interconnects wiring

New structure

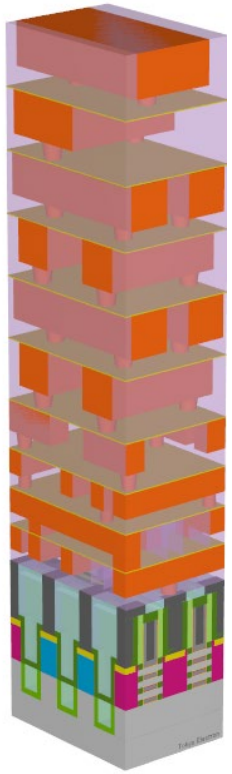


- ✓ Peripheral circuit is manufactured on the separate wafer and bond to the memory cell wafer
  - higher peripheral circuit performance
  - shorter TAT* process
- ✓ Shorter interconnects wiring

* TAT: Turnaround time

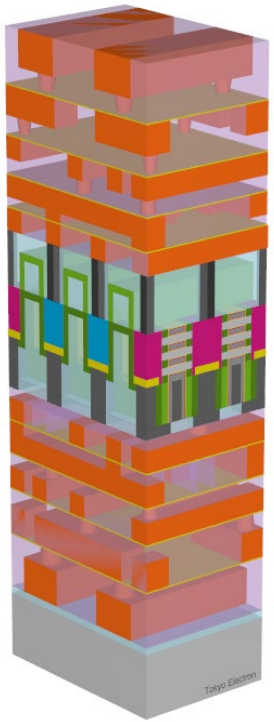
Wafer Bonding Application for Logic Backside PDN

Current structure



Signal & Power

Backside PDN：Power Delivery Network



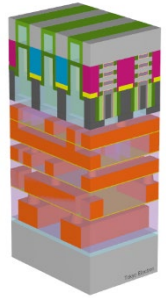
Power

Signal

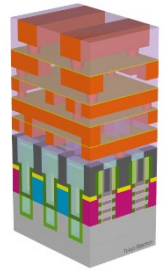
Pursue further scaling without the power wiring bottleneck

Power BEOL (Backside)

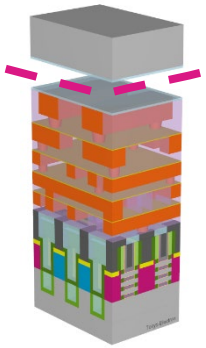
Backside thinning



Signal BEOL (Front side)

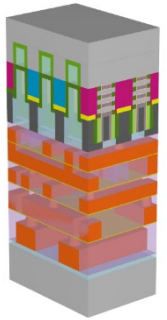


Bulk Si Wafer bonding

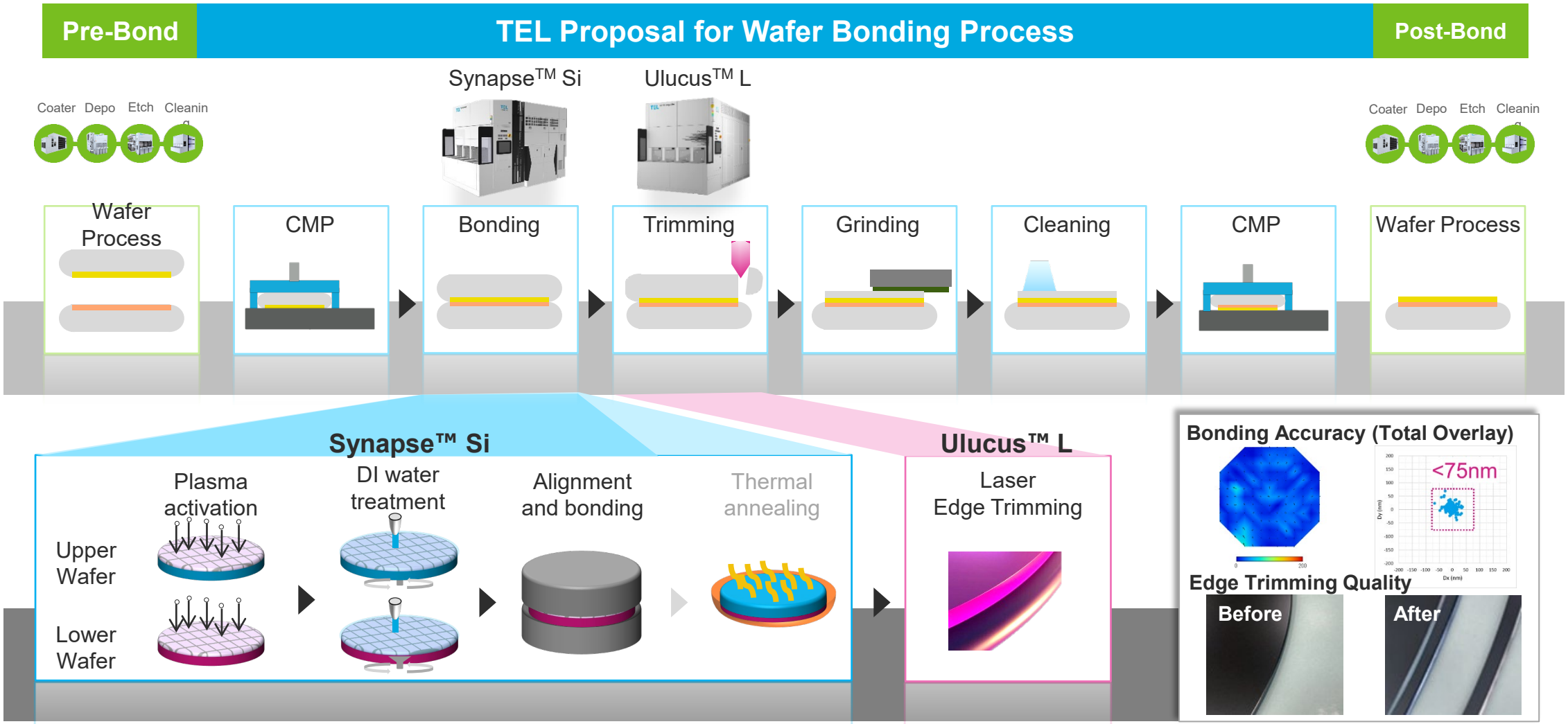


Bonding surface

Reverse



Our Proposal for Wafer Bonding Process



Wafer Bonding System

- Synapse™ Si
  - Integrate high high-productivity platform cultivated in the front-end process with plasma, cleaning and high-accuracy bonding modules
  - high productivity (uptime ≧ 90%)
    - alignment accuracy 3σ ≦ 50nm

High productivity and stable operation are realized at mass production fabs
Contribute to our customers to realize the future of "3D integration"

Laser Trimming System

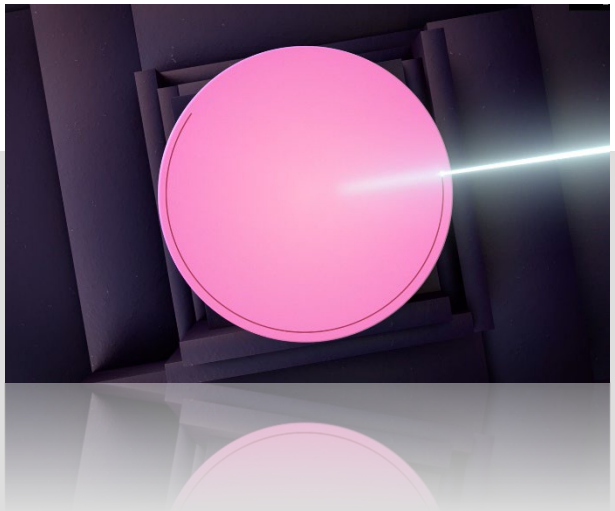
- Ulucus™ L (New release)
  - Edge trimming on bonded wafer
  - Latest platform utilizing super clean technology from the front-end process, with the integration of laser control technology

Laser technology realizes high accuracy and quality trimming processes, and environment-friendly capability through the reduction of DIW usage

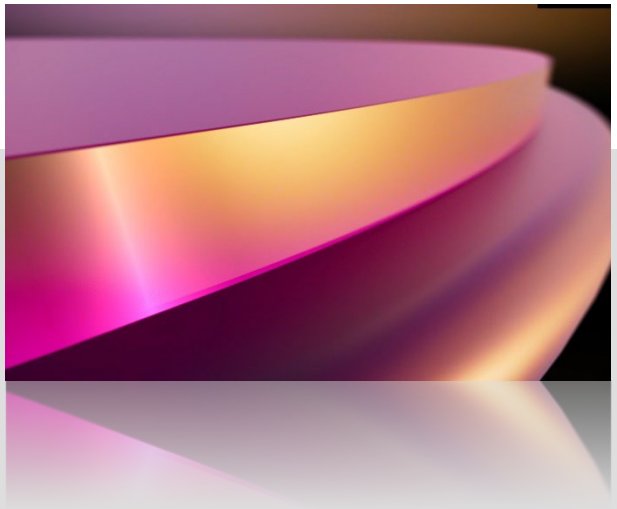
Laser Trimming System

Revolutionize wafer bonding process with laser technology

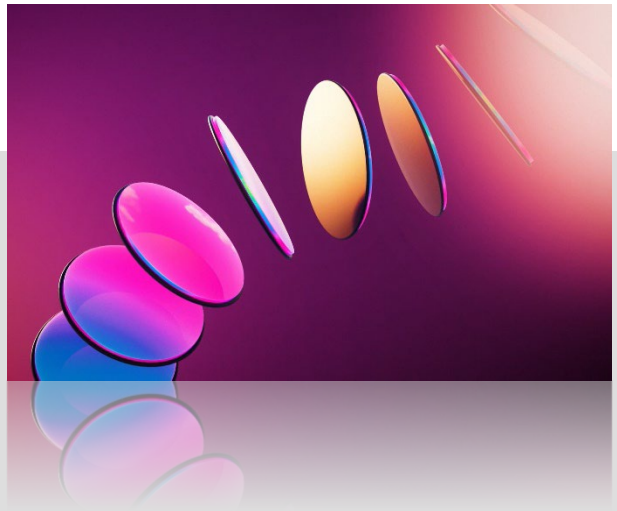
Enhance yield and significantly reduce the use of DIW in the edge trimming process



Higher Accuracy
Enabling narrower trimming width



Smooth Sidewall
Less damage, Better yield



Higher Throughput
High productivity, Reliability

Save Water
Reducing DIW to 70% or more

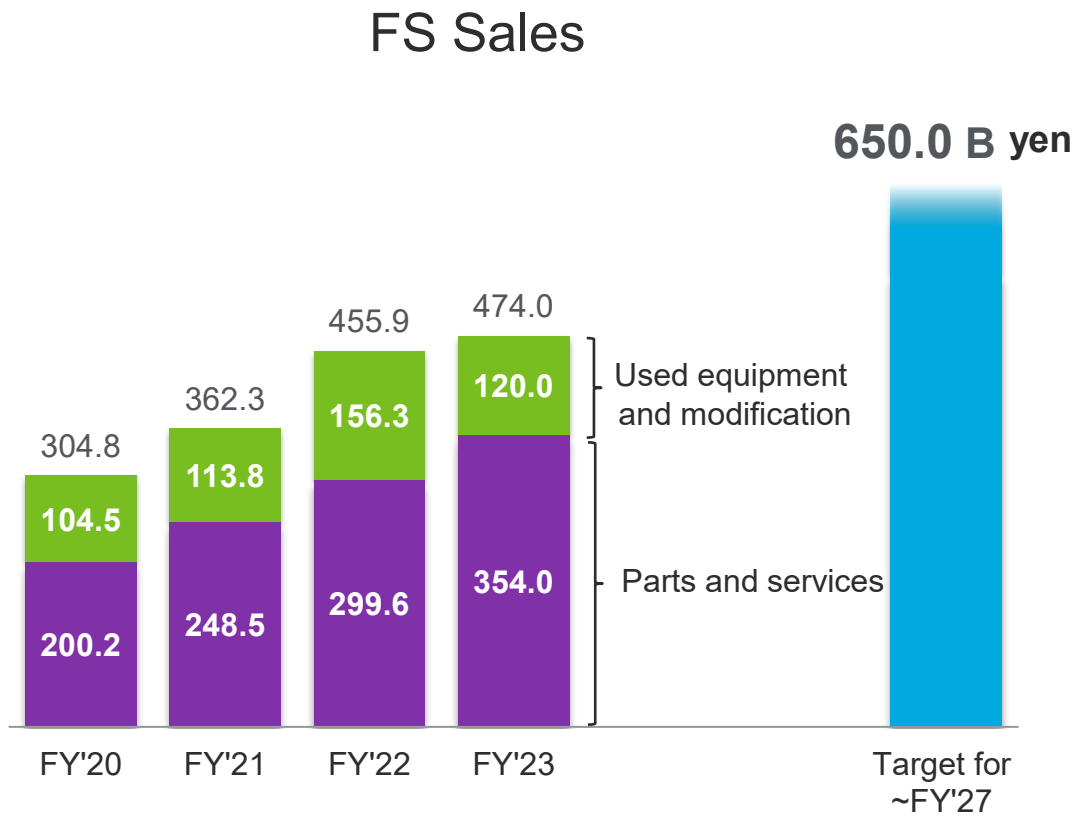
7-6：Field Solutions Business Initiatives

Basic Strategy for Field Solutions (FS)

- Expand sales for equipment for mature (legacy) nodes
- Deploying solution business based on installed base
- Development and promotion of advanced Field Solutions
  - Providing leading-edge and sustainable support that utilizes the latest technology, such as DX
  - Development of remote maintenance support and training tools
- Enhancing the front-lines engineers and capabilities
  - Continuous skill improvement for field engineers

Support customers to maximize their business operations through services with high added value

Field Solutions (FS) Sales Results and Business Contents

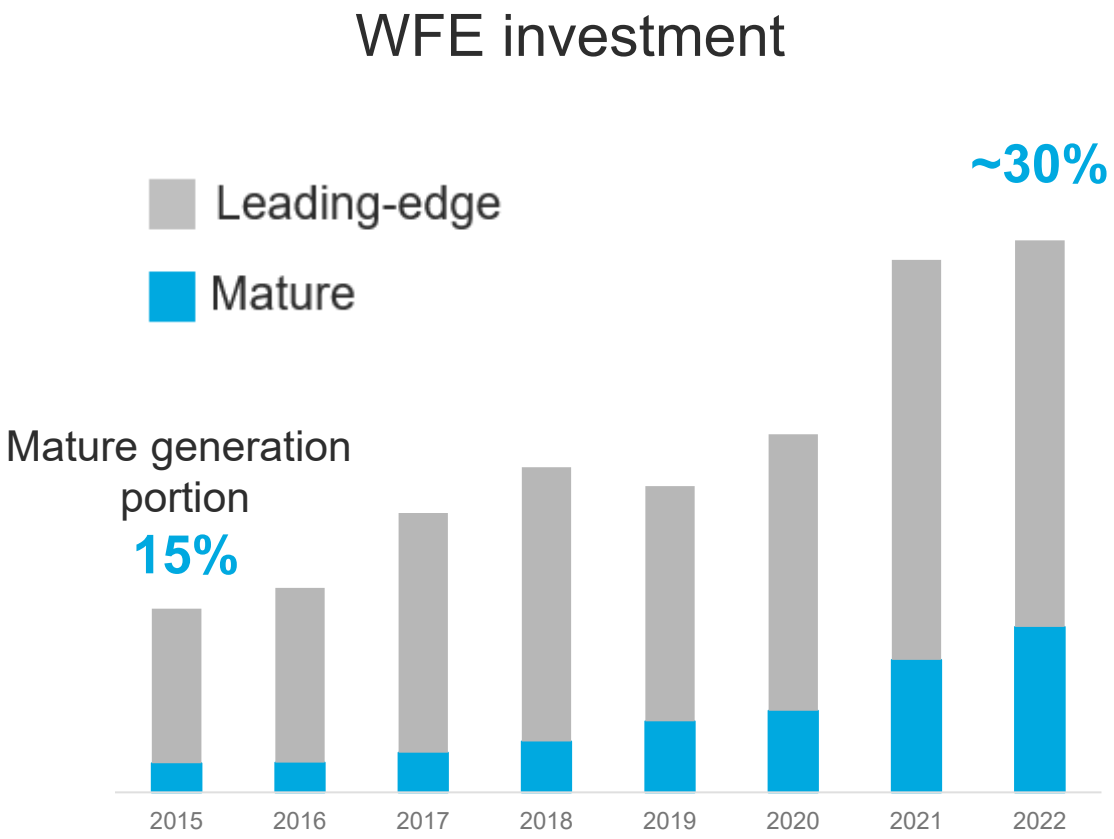


- Parts and repair
  - Predictive maintenance for parts deterioration
  - Appropriate parts inventory management and prompt delivery
- Services
  - Providing “comprehensive contract type” services that encompass everything from equipment delivery to after-care maintenance
  - Proposing solutions that address customer demands and maximizing equipment utilization rates
- Modification
  - Productivity improvement
  - Yield improvement

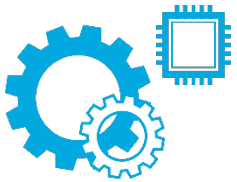
SAM*1 is expanding with 91,000*2 installed base currently and increasing by approx. 5,000 to 6,000 units each year

*1 SAM: Served available market
*2 As of December 31, 2023

Rapidly Growing Investment in Mature Generation



- Equipment
  - Reengineered equipment for 200mm wafer
  - New equipment for power devices
- Parts, repair and services
  - Parts replacement
  - Overhaul, cleaning, renewal
  - Repair, maintenance, relocation
- Modification
  - Performance enhancement
  - Process change, productivity enhancement
  - Modifications to software, hardware



With the expansion of investment in mature generations, a wide range of business opportunities are growing

Equipment for Mature Generations

- Reengineered equipment for 200mm wafer
  - Thermal deposition systems, coater/developer, etch systems, etc.
  - Sales expansions not only for replacement demand of existing customers, but also for emerging customers

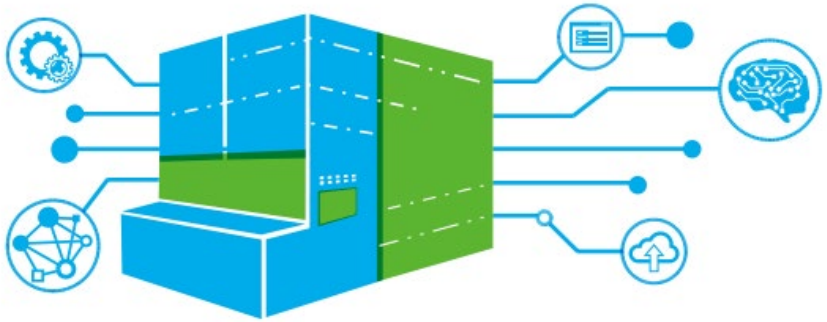
- Equipment for power devices
  - Equipment for SiC wafer, 300mm etch system
  - Respond to rapid growth in demand for power devices, such as for automotive

SiC epitaxial film deposition system

By integrating our technological assets with new technologies, improve productivity and reduce impact on the environment

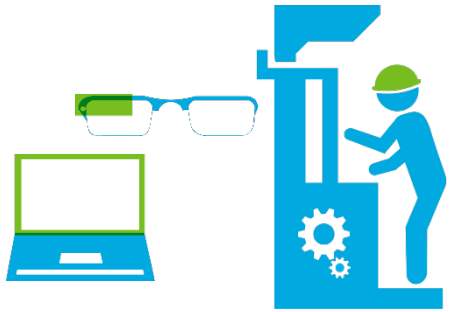
Advanced Field Solutions

TELeMetrics™



- Monitoring data on individual equipment
- Knowledge management and accumulation of problem case studies

Remote Support



- Minimization of downtime through predictive maintenance of equipment
- Remote support that enables prompt response even under travel restrictions

Strengthen Global System

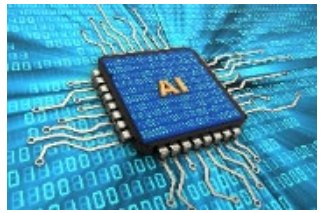
- Provision of support that takes advantage of time differences
- Parts management and delivery through advanced logistics
- Engineer training program

Proposing solutions with high added value centered around “TELeMetrics™” that utilize DX

7-7：Digital Transformation (DX) Initiatives

TEL DX Vision

- The tide of DX ripples throughout the industrial world as a whole, and the semiconductor industry is no exception. It is positioned as a part of the solution toward further demands for die miniaturization and layering



AI Chip


Autonomous


Cloud Service


AR/VR

TEL DX Vision

A global company where all employees drive enterprise value creation sustainably through activities such as value addition and efficiency improvements by leveraging digital technology

DX activities are ultimately a method and an opportunity to realize sustainable creation of corporate value. We have defined the image we must achieve (our “To-Be Image”) in order to realize transformation

TEL DX Grand Design

TEL Vision

A company filled with dreams and vitality that contributes to technological innovation in semiconductors

TEL Medium-term Management Plan

Achieving the Financial Model in TEL's Medium-term Management Plan

Net Sales ≥ 3 trillion yen | Operating Margin ≥ 35%

The 4 Materialities

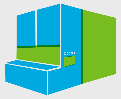
- Product Competitiveness
- Customer Responsiveness
- Higher Productivity
- Management Foundation

TEL DX Vision

A global company where all employees drive enterprise value creation sustainably through activities such as value addition and efficiency improvements by leveraging digital technology

DX Application

Innovative enhancement of materiality through DX activities that connect PLM steps



Development

Manufacturing

Field

DX Business Platform

Enhancing the Management Foundation through digitization and digital technology

DX Infrastructure

Skill Development

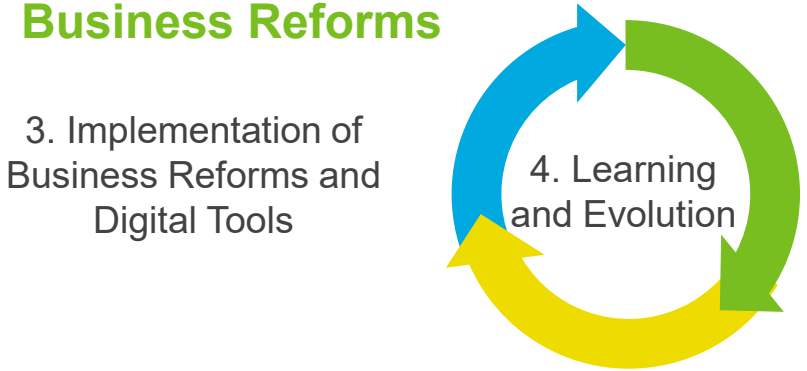
Consciousness and Culture

Data Governance and Platform

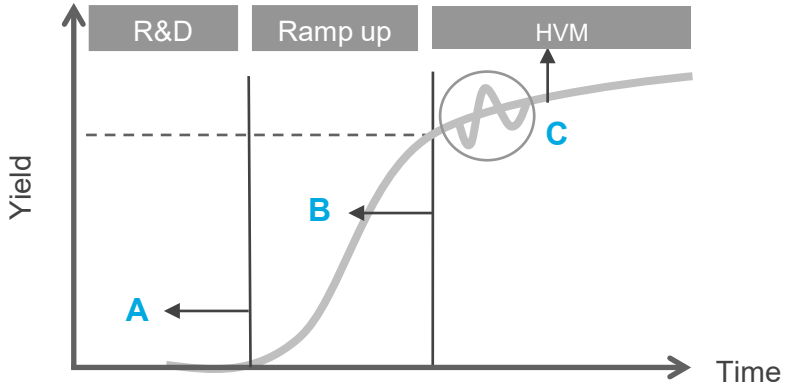
Steps of DX Activities

Product Innovation

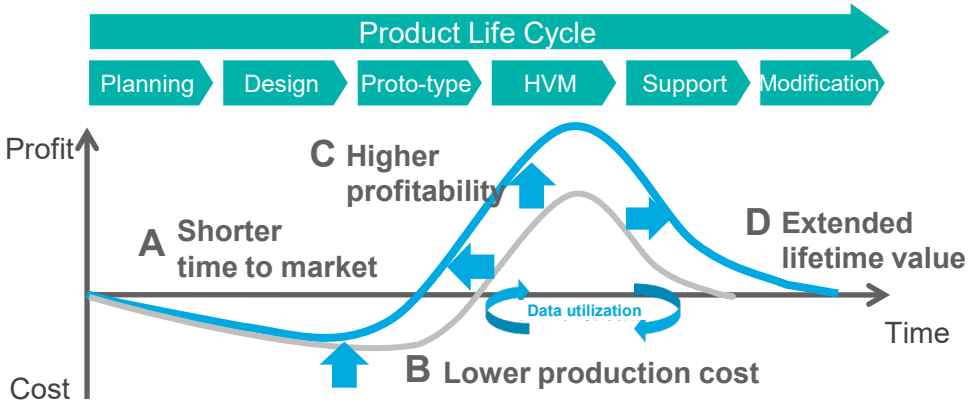
Business Reforms



DX in Contributing to Customers' Value Creation



DX in Raising Capital Efficiency



Solving issues of a higher dimension through digital transformation

Relationships between Projects in DX-related Developments

DX Foundation

- Company-wide DX training
- Data lake maintenance
- Maintenance of environments for DX development

Capital Efficiency/ Management Foundation Application

- Development of apps for equipment
- Development of apps for the field
- Development of apps for GBP

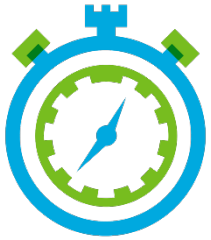
Equipment Foundation

- Development of equipment frames
- Development of equipment foundation technologies

Added Value Application

- Development of equipment AEPC
- Development of service tools
- Development related to measuring instruments

Quality

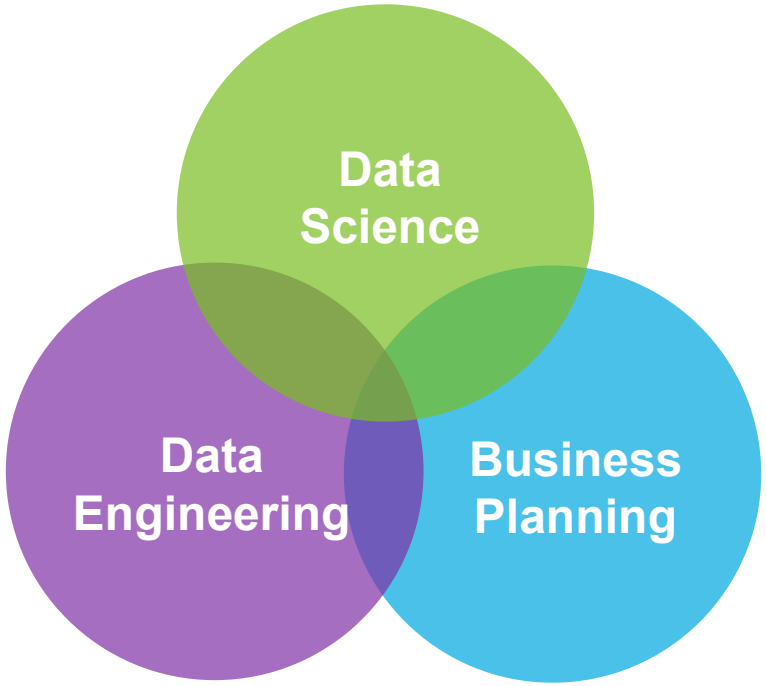


Time

Talents

Through a DX foundation and DX that improves capital efficiency,
we will improve the quality and speed of our work,
and transition toward a use of time that creates even greater value

DX Engineer Training Plan



All Employees

The ability to understand and utilize knowledge of information science, such as cutting-edge information processing, artificial intelligence and statistics

The ability to realize a form of data science that meaningfully contributes to TEL's creation of corporate value, and to practice and operate data science in a manner that fits our purposes

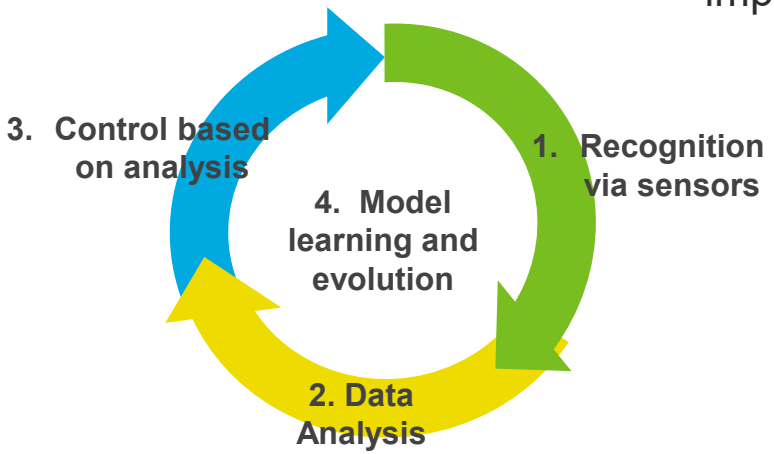
The ability to organize issues and their backgrounds, derive solutions, and connect them to our business

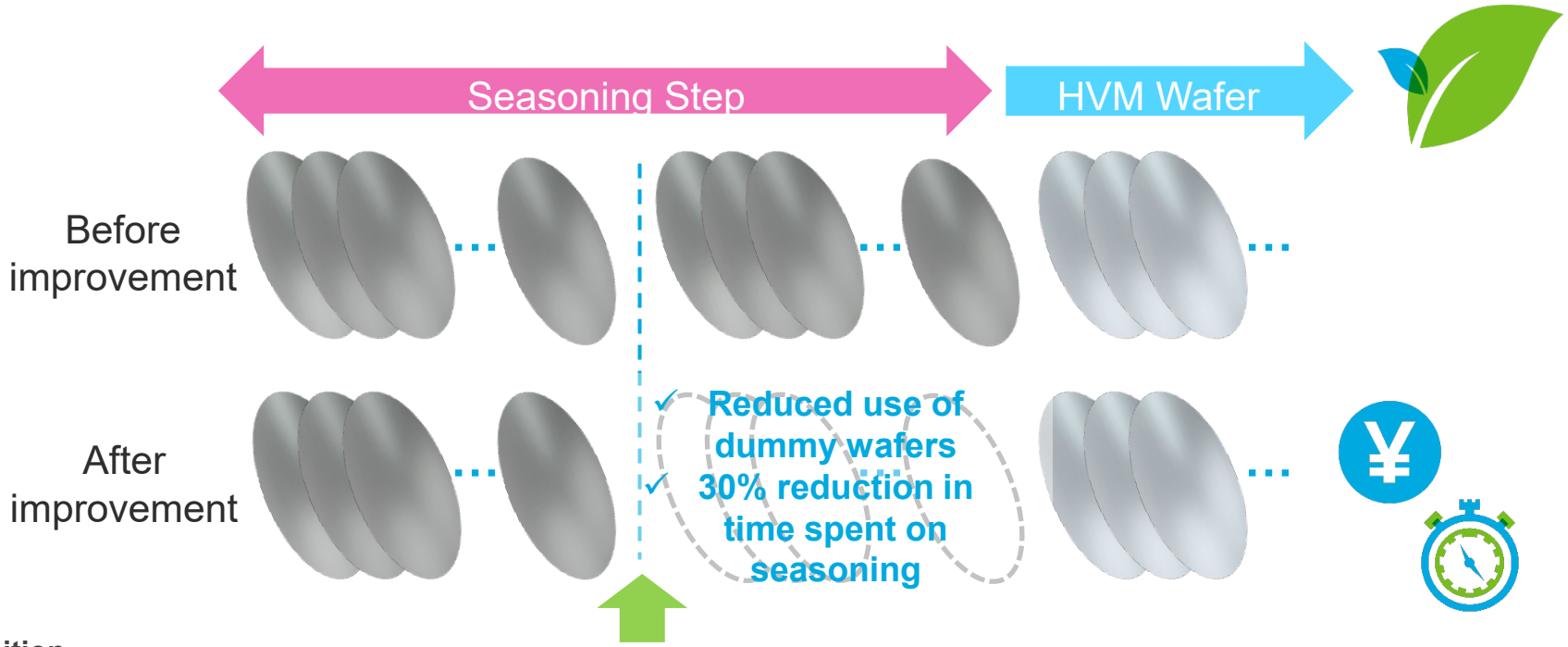
Utilizing data and digital technology in our day-to-day business operations in order to optimize our business operations and create added value

Engaging in planned training to foster personnel who can capitalize data science in TEL's business

Example Activity 1 – Increasing Productivity of Equipment:

Improving Utilization of Etch Equipment





Seasoning at the right time with endpoint detection

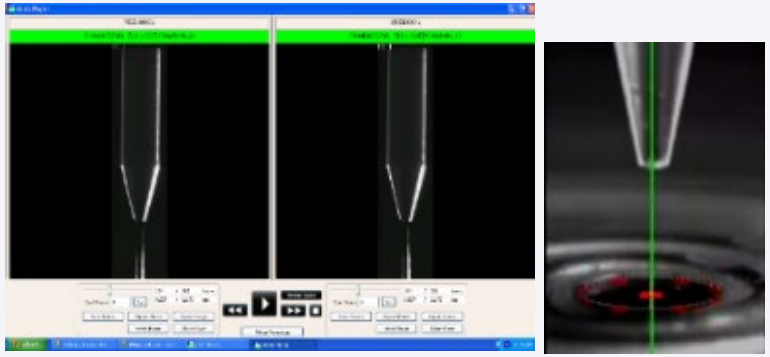
*ISSM 2020, from "Seasoning Optimization by using Optical Emission Spectroscopy," published by the Company

Feedback from the sensor provided an appropriate understanding of chamber conditions and improved utilization of equipment

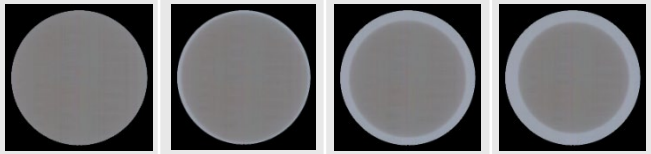
Example Activity 2 – Increasing Operation Cost of Equipment:

Reducing Chemicals of Coater/Developer

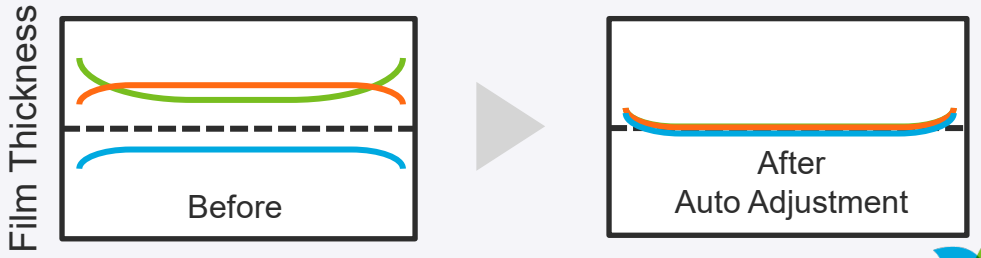
Monitoring of chemical discharge status
using image processing technology

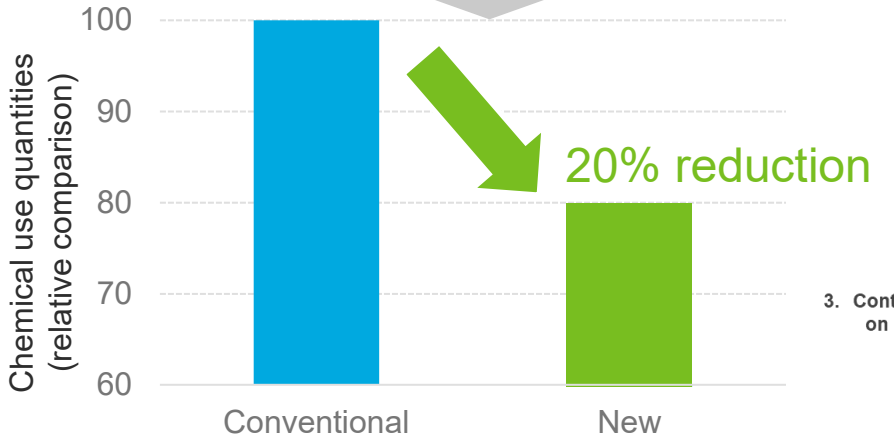


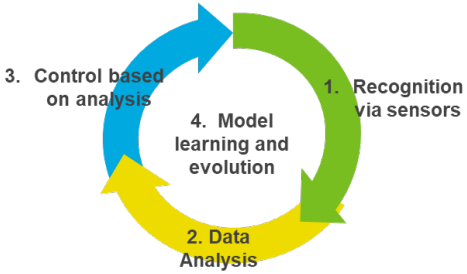
Monitoring of chemical coverage of interior of surfaces
using image processing technology

Dispense Volume	X ml	Y ml	Z ml	A ml
Judgement	Passed	Passed	Failed	Failed
Wafer image by WIS				

Automatic film thickness adjustment function

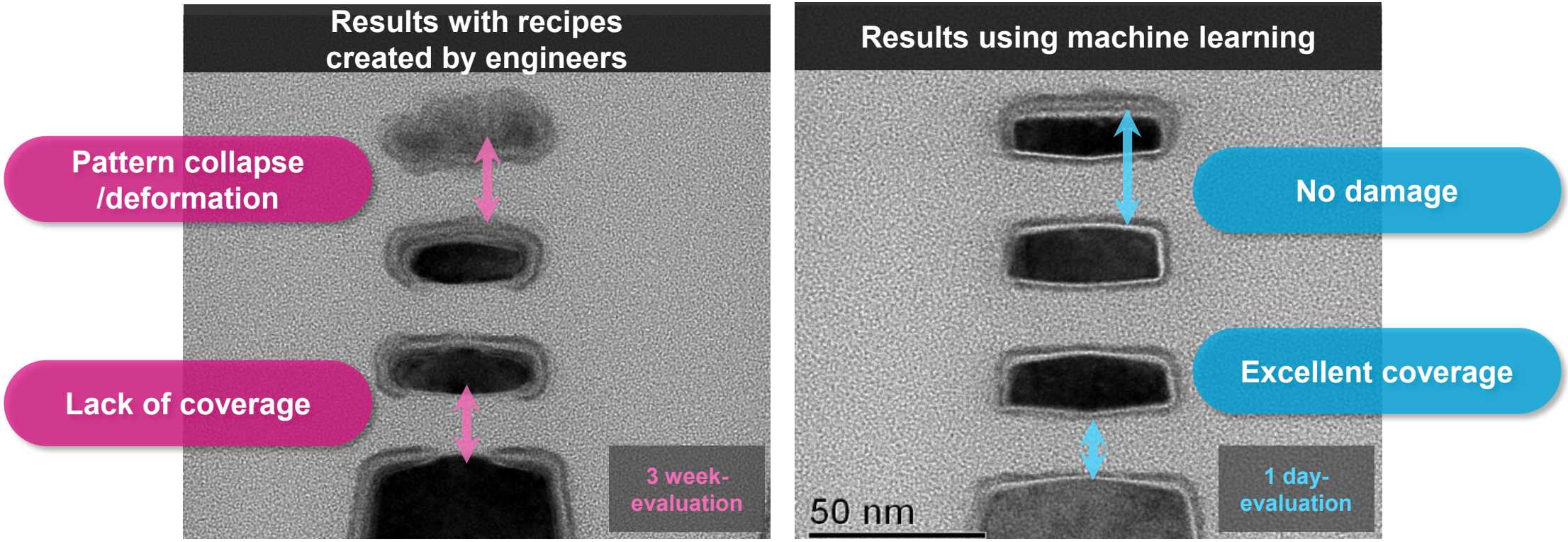






Contributed to customer operation costs
and the environment by using machine learning

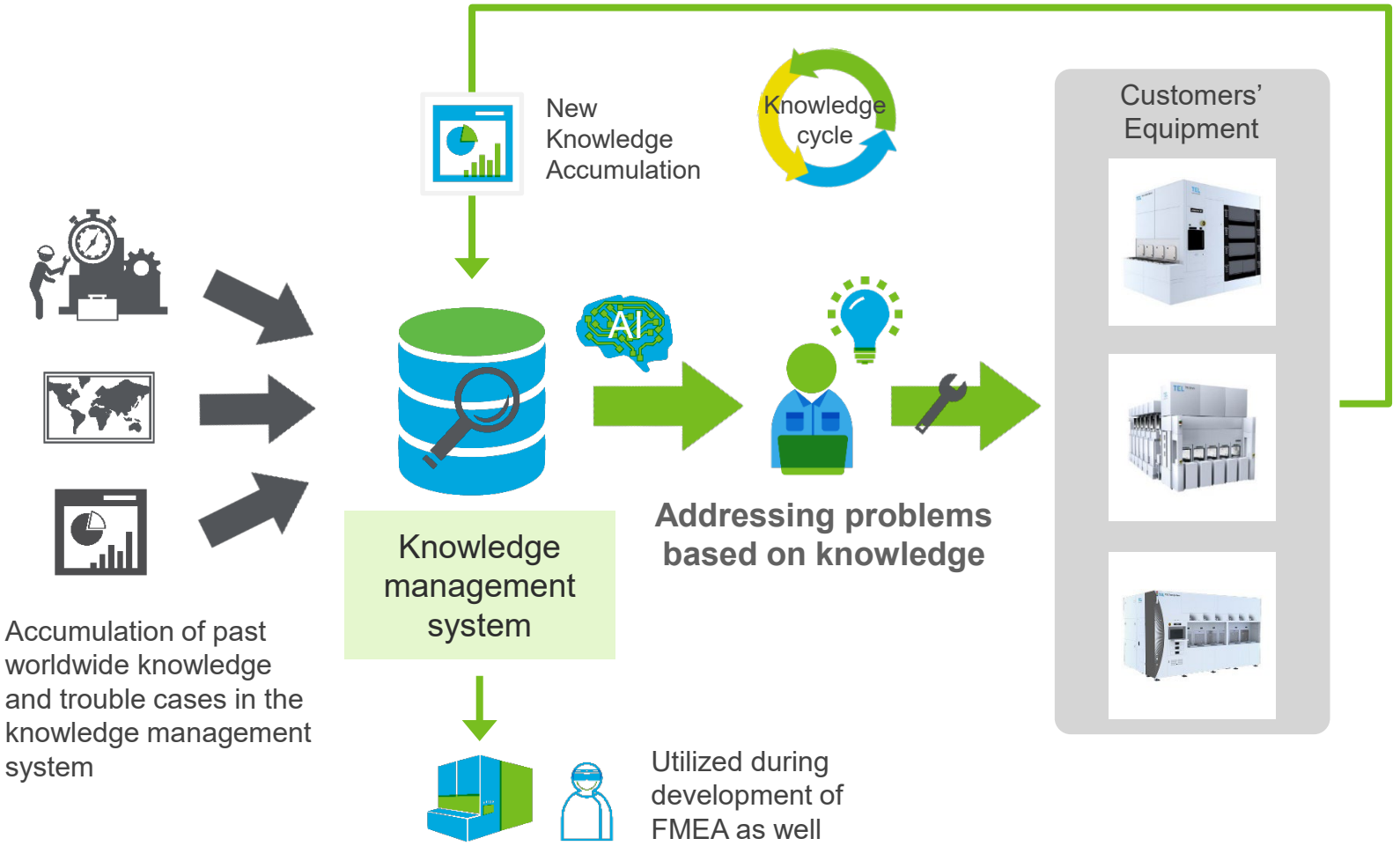
Example Activity 3 – Increasing Productivity of R&D:
Process Informatics



Source: Tokyo Electron Technology Solutions Limited / Tokyo Electron Limited

Achieved good step coverage with no pattern deformation in the ALD process by machine learning

Example Activity 4 – Improving Overall Equipment Effectiveness



Time Taken to Resolve Problems
(from incidence of problems to cause investigation)

Conventional	Several days
Knowledge utilization	Same day (improved OEE)

OEE: Overall Equipment Effectiveness
FMEA: Failure Mode and Effects Analysis

Using the Knowledge Management System to reduce the time taken to resolve problems and improve equipment operation rates

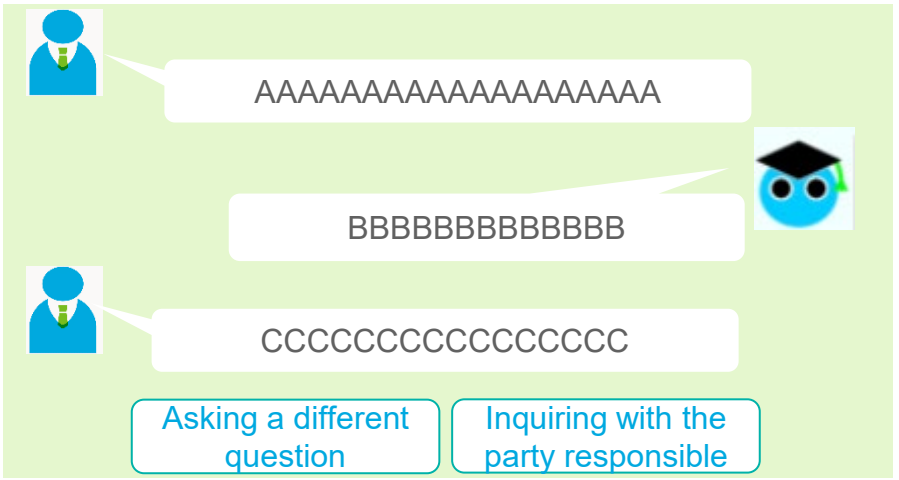
Example Activity 5 – Increasing Productivity of Operations:

Optimizing Business Operations by Implementing Chat-bots in Back-Office Work

Legal Department, Finance Department, Personnel Department, General Affairs Department

Responding department

- Reduce the number of inquiries, man-hours spent on inquiries
- Share know-how to resolve issue of tasks becoming too personalized, train younger employees



- Make it possible to answer using choices or free input
- If chat-bot cannot provide an automated answer, make it possible to use the system to engage in inquiries
- Realize a smarter system by analyzing user histories and adding FAQs

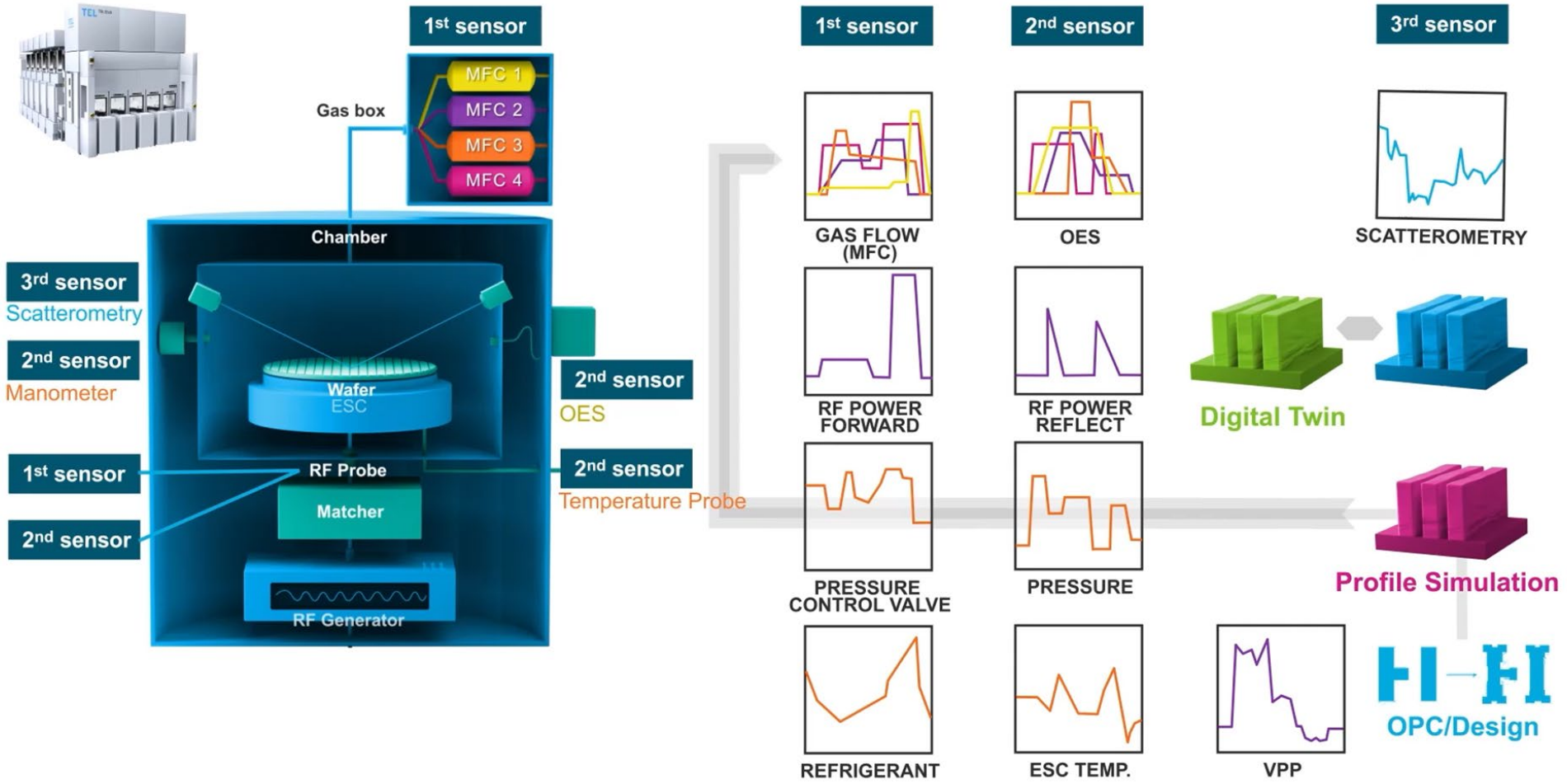
Employee

- Make it possible to ask questions any time without hesitation
- Clarify the departments responding to inquiries
- Reduce variability in answers based on the person in charge

Reduced the number of man-hours spent by employees answering questions with introducing chat-bots in multiple departments

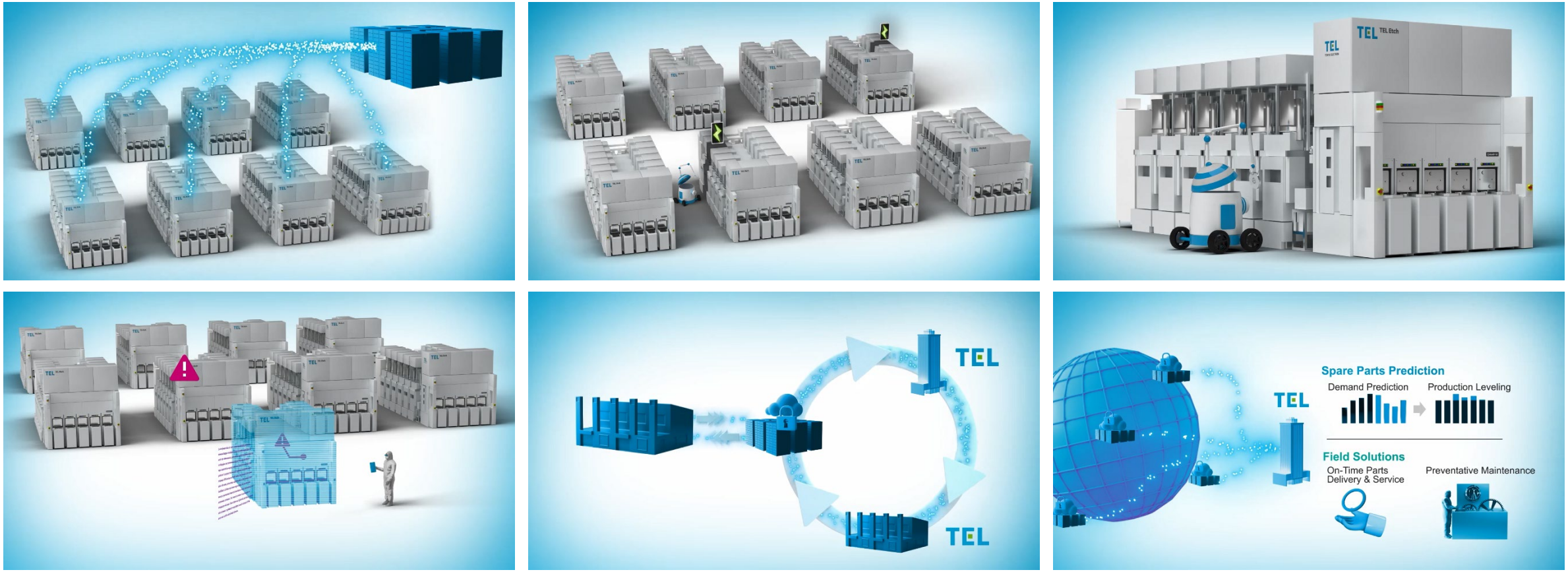
Digital Technologies to Increase Customer Value 1:

Example in Etch Equipment



Aiming to maximize customer value using all digital technologies

Digital Technologies to Increase Customer Value 2:
Example in Etch Equipment

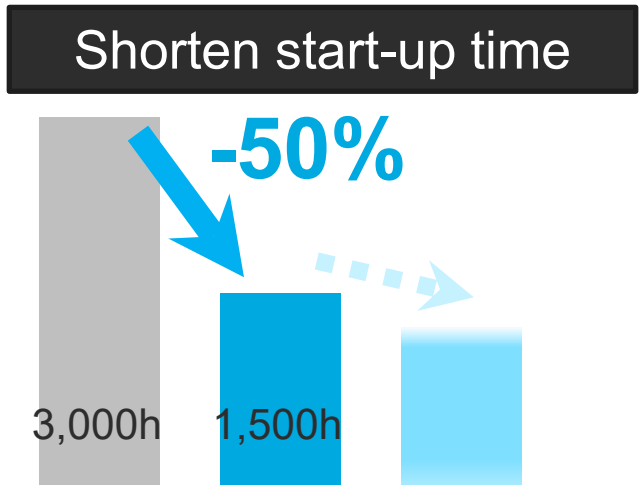


Aiming to maximize customer value using all digital technologies

7-8：Procurement and Manufacturing Strategy

Continuous Production Innovation in Pursuit of Safety, High Quality and High Reliability

- Build a production system able to quickly respond to market changes
- Shorten time from new product development to mass production
- Shorten production lead times: Achieve 100% module shipment
- Utilize DX and automation in manufacturing, and expand automated warehouse
- **Significantly reduce equipment start-up time (One-touch start-up)**
  - Reduce start-up time up to 75% (primary target), One-touch (final target)

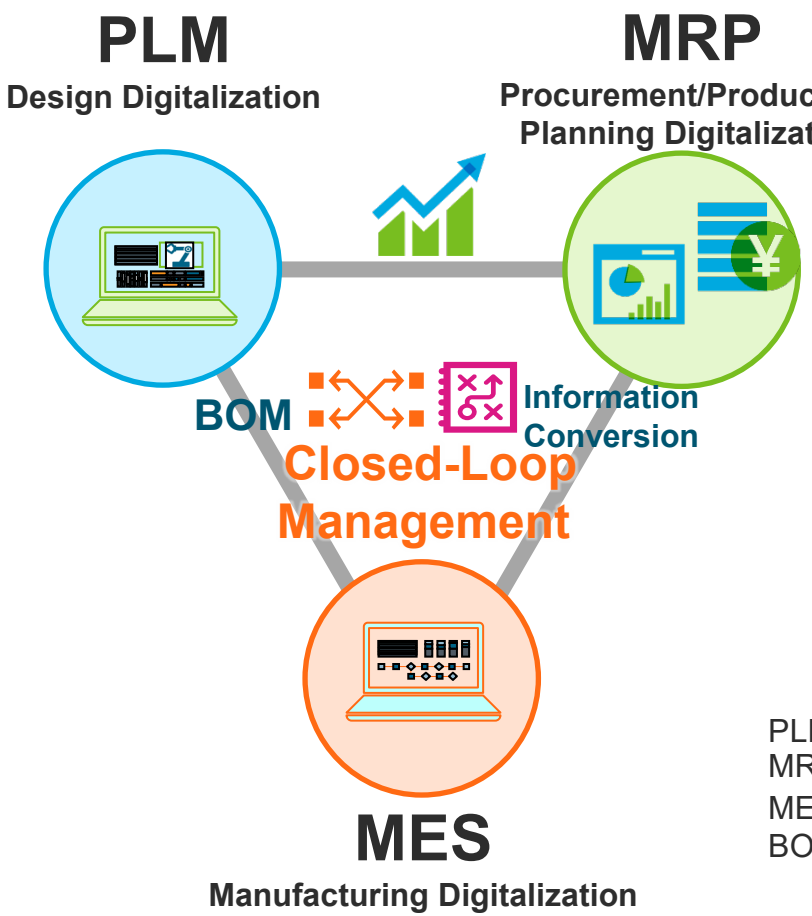


Conventional ➔ after production innovation

Expected outcome from shorten start-up time

- Enhance productivity and start-up quality
- Reduce accident risks
- Optimize resources and the work-life balance

Efforts to Utilize TEL PLM-DX and Improve Productivity and Efficiency



TEL PLM-DX

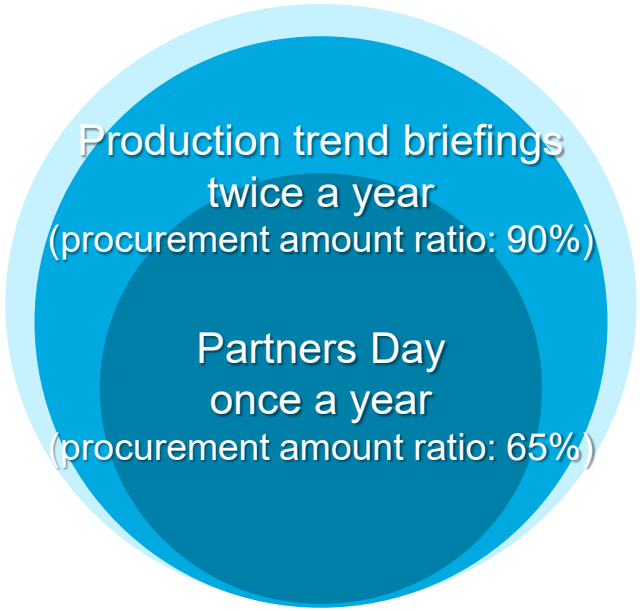
PLM: Product Lifecycle Management
MRP: Material Resource Planning
MES: Manufacturing Execution System
BOM: Bill of Material

- Improve core system
  - Production leveling < 12 months
  - MRP processing capability for procurement increased 10-fold
- Introduce PLM-DX and BOM concept
  - Enhance production capability up to 2 times within 3 years
  - Minimize manufacturing lead time
  - 3-fold increase in design efficiency
  - Reduce new product development period by half

"Shift Left" production plan toward the business scale of 1 trillion-yen procurement

Build a Sustainable Supply Chain

- Fair and transparent relationships and reliable trust relationship with our business partners
  - – Implement CSR/BCP assessments based on industry codes of conduct
  - – Share knowledge in such areas as safety, quality, the environment and compliance



E-COMPASS

Applaud environmental impact reduction activities, adding environmentally related items to assessment studies

- ✓ Reduce CO_2 emissions and the amount of energy usage
- ✓ Introduce renewable energy
- ✓ Promote resource conservation
- ✓ Promote waste reduction and recycling
- ✓ Promote activities for reducing the environmental impact of logistics

Procurement BCP and Proactive Procurement Activities

Mid- and long-term forecast
Promote “Shift Left” procurement strategy
Build BCP system resilient to procurement difficulty

Safety stock
Inventory liquidity

Oversee whole supply chain from upstream to downstream
Visualize and grasp risks

Visualize supply chain

Supply chain responsive to any kind of risks (Raw materials, parts, processing and assembly)
Strong and reliable supply chain

Risk management on business partners
Strengthen partnership

Measures for procurement BCP

Early procurement of parts

- Early procurement for long term
- Ensure inventory exchange flexibility among factories
- Inventory reductions in total

Secure semiconductor devices

- Secure semiconductor devices for our equipment
- Visualize and streamline distribution channel
- Collaborate with semiconductor makers

= TEL can be a customer of our customers

Parts and Suppliers

- Identify and analyze risk parts
- Multi sourcing of producing countries
- Standardization, centralization and decentralization of parts
- Measures to secure capacity for us

Appendix：Data section

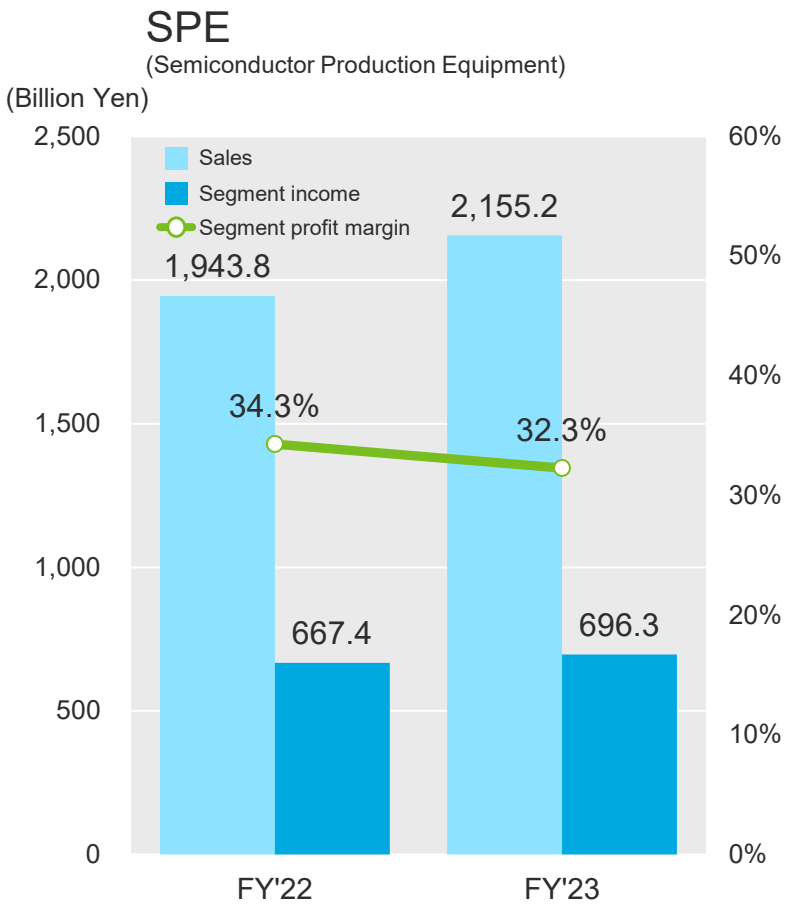
Financial Summary

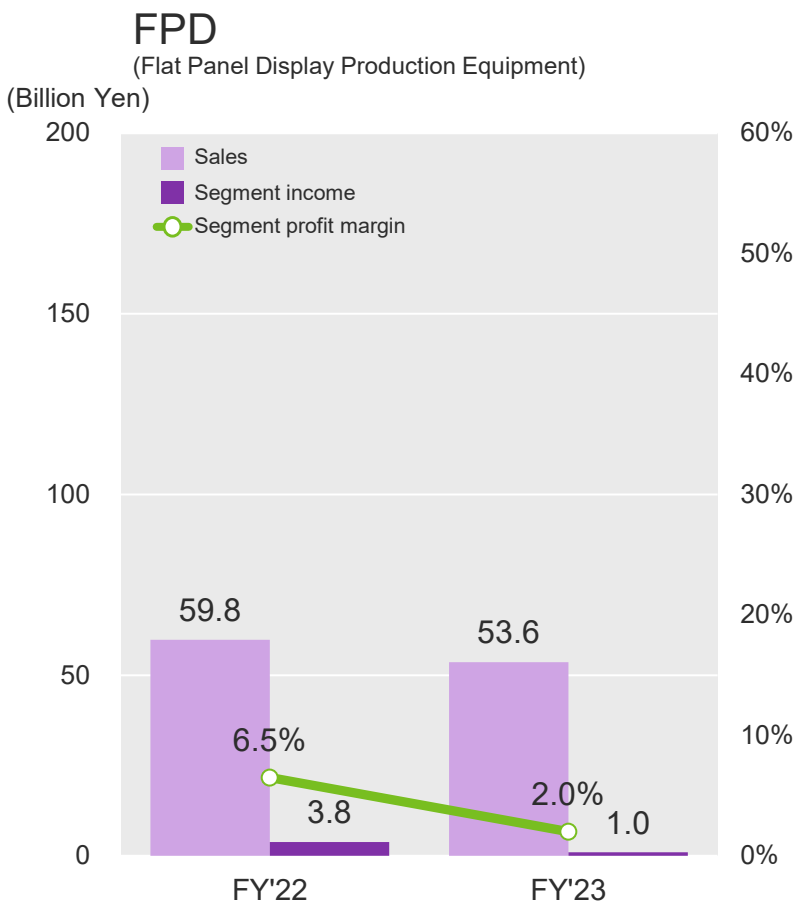
(Billion Yen)

	FY2022	FY2023	YoY Change
Net sales	2,003.8	2,209.0	+10.2%
SPE	1,943.8	2,155.2	+10.9%
FPD	59.8	53.6	-10.3%
Gross profit	911.8	984.4	+8.0%
Gross profit margin	45.5%	44.6%	-0.9pts
SG&A expenses	312.5	366.6	+17.3%
Operating income	599.2	617.7	+3.1%
Operating margin	29.9%	28.0%	-1.9pts
Income before income taxes	596.6	624.8	+4.7%
Net income attributable to owners of parent	437.0	471.5	+7.9%
EPS (Yen)	935.95	1,007.82	+7.7%
R&D expenses	158.2	191.1	+20.8%
Capital expenditures	57.2	74.4	+29.9%
Depreciation and amortization	36.7	42.9	+16.9%

1. In principle, export sales of Tokyo Electron's mainstay semiconductor and FPD production equipment are denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of exchange rate fluctuations on profits is negligible.
2. Profit ratios are calculated using full amounts, before rounding.
3. EPS is calculated based on the number of outstanding shares excluding treasury stock after the stock split.

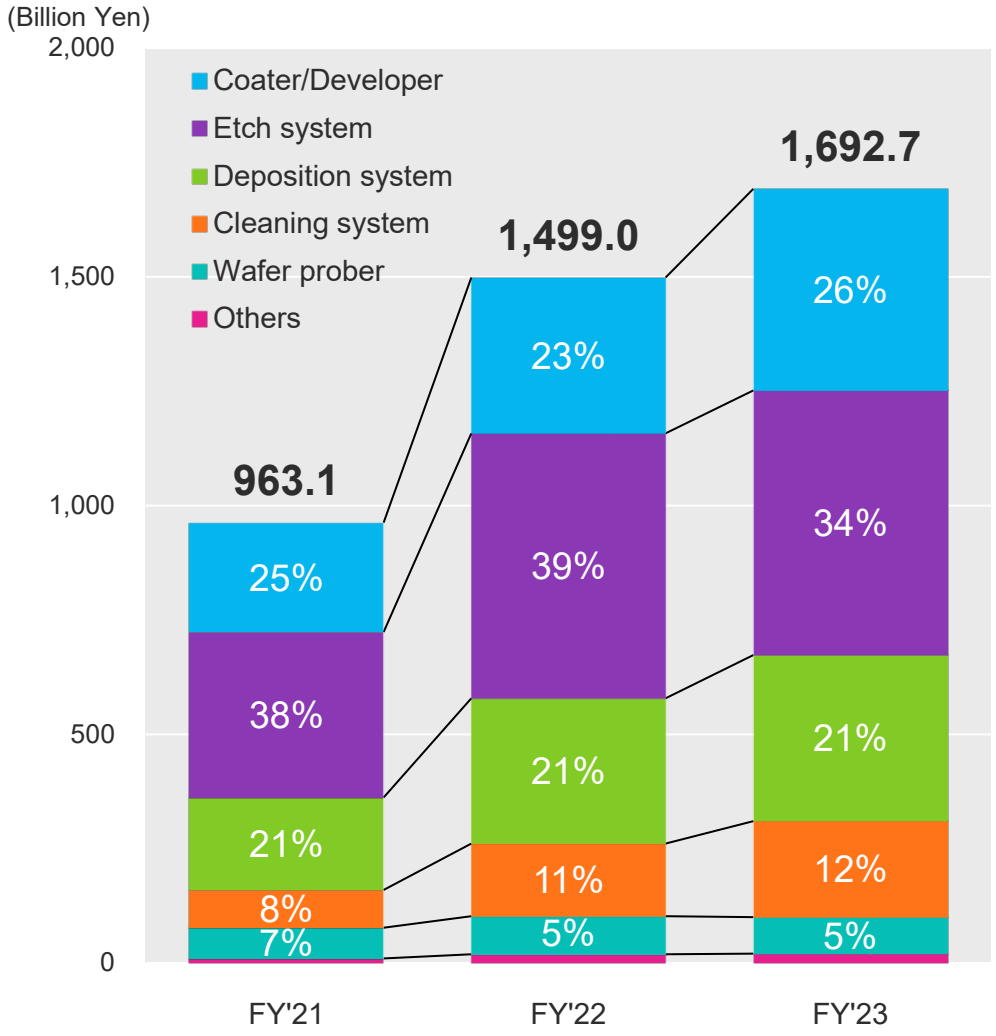
Segment Information





1. Segment income is based on income before income taxes.
2. R&D expenses such as fundamental research and element research, etc. and other general and administrative expenses are not included in the above reportable segments.
3. Composition of net sales figures is based on the sales to customers.

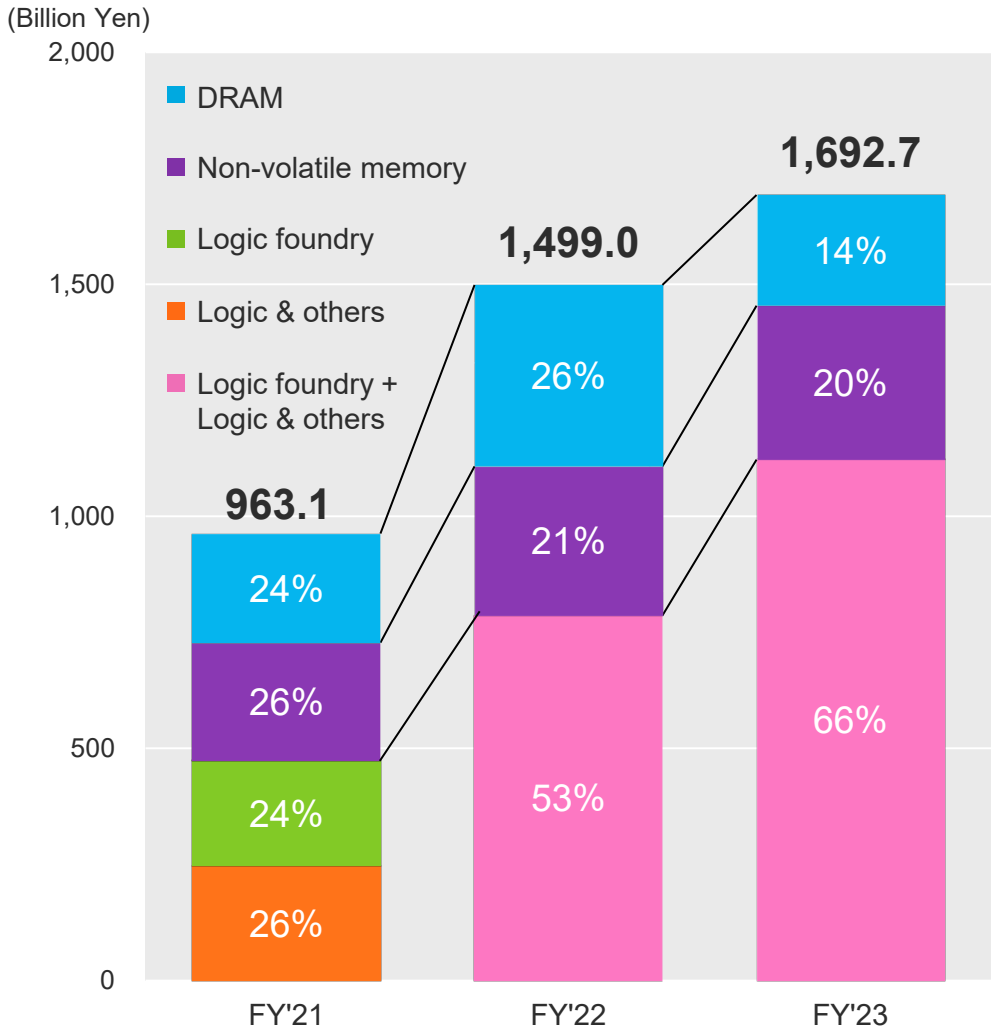
SPE Division: New Equipment Sales by Product



- FY2023 new equipment sales increased by 12.9% YoY to ¥1,692.7B
- Although there was a change in the composition ratio of equipment due to changes in the customers' investment mix, overall new equipment sales increased YoY

Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

SPE Division: New Equipment Sales by Application

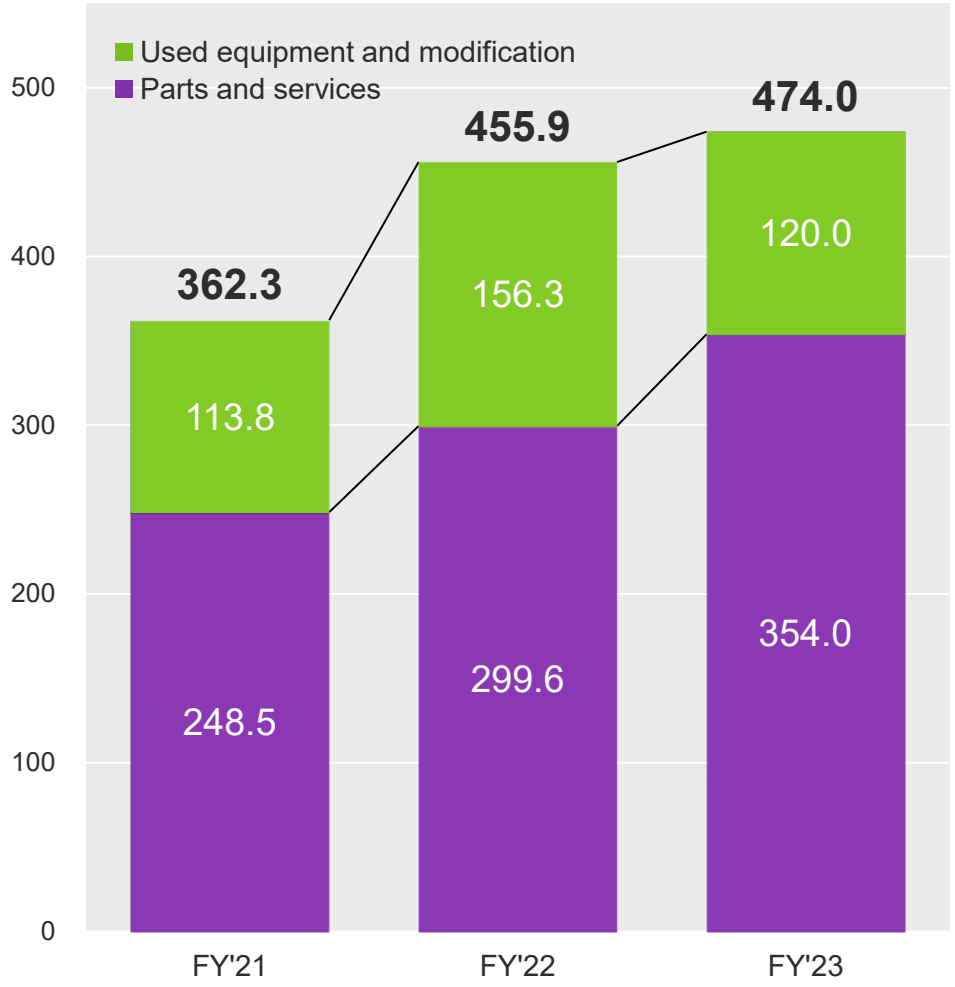


- In logic/foundry, sales increased significantly on the back of solid investment
- Due to inventory adjustments by customers, sales composition for memory decreased

Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

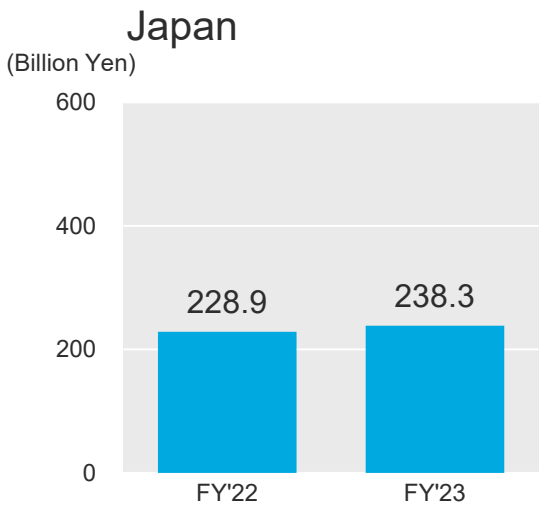
Field Solutions Sales

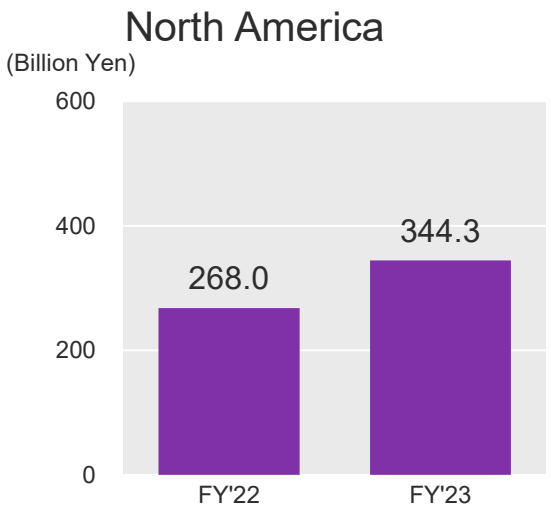
(Billion Yen)

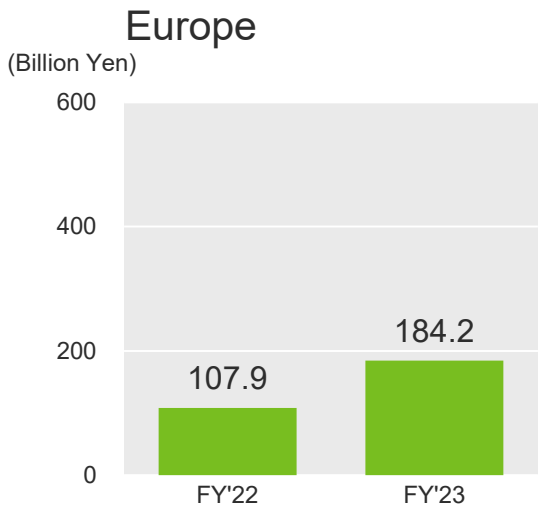


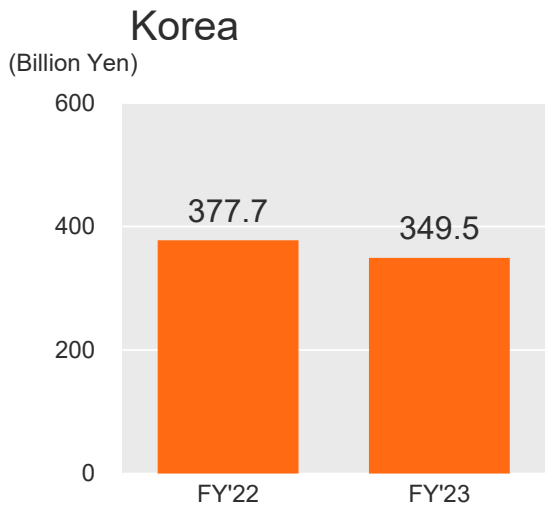
- FY2023 Field Solutions sales increased by 4.0% YoY to ¥474.0B
- Parts and services sales continued to be solid

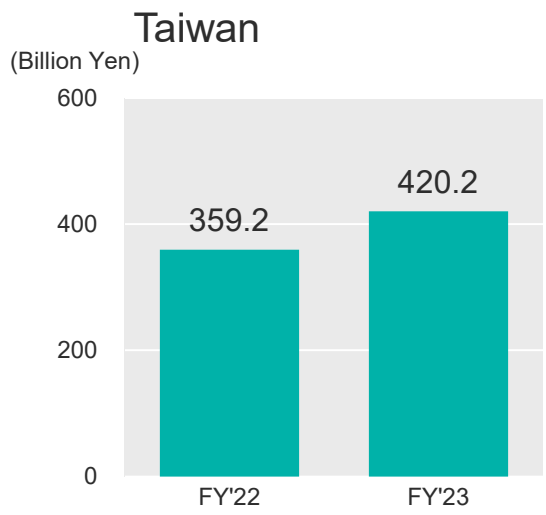
SPE Division: Sales by Region

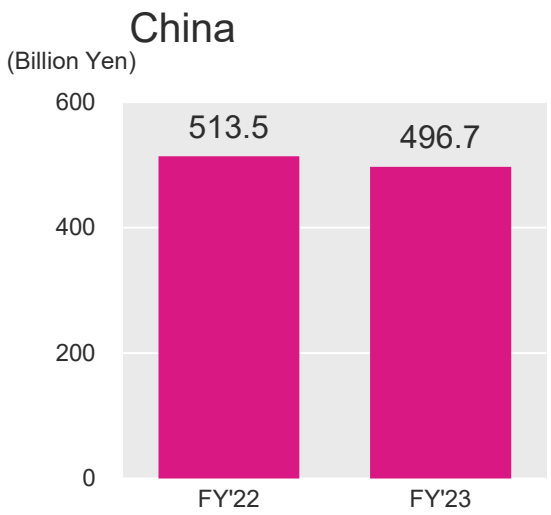


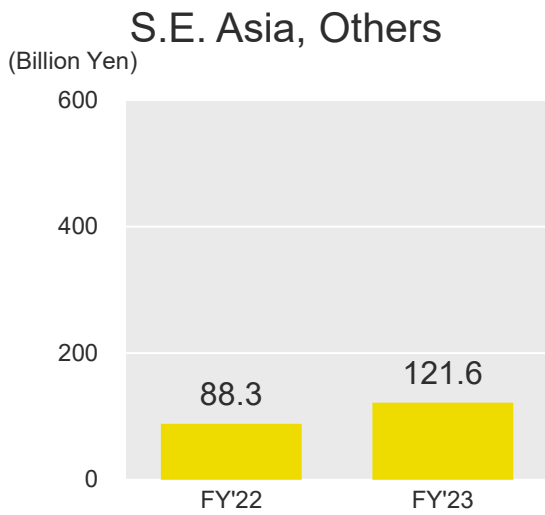


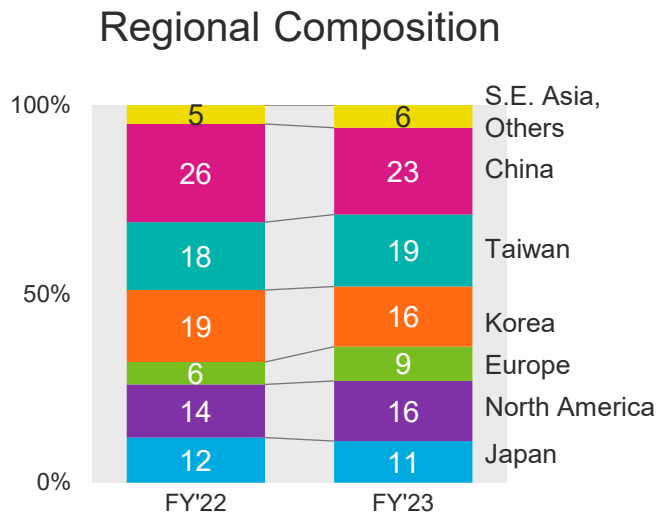












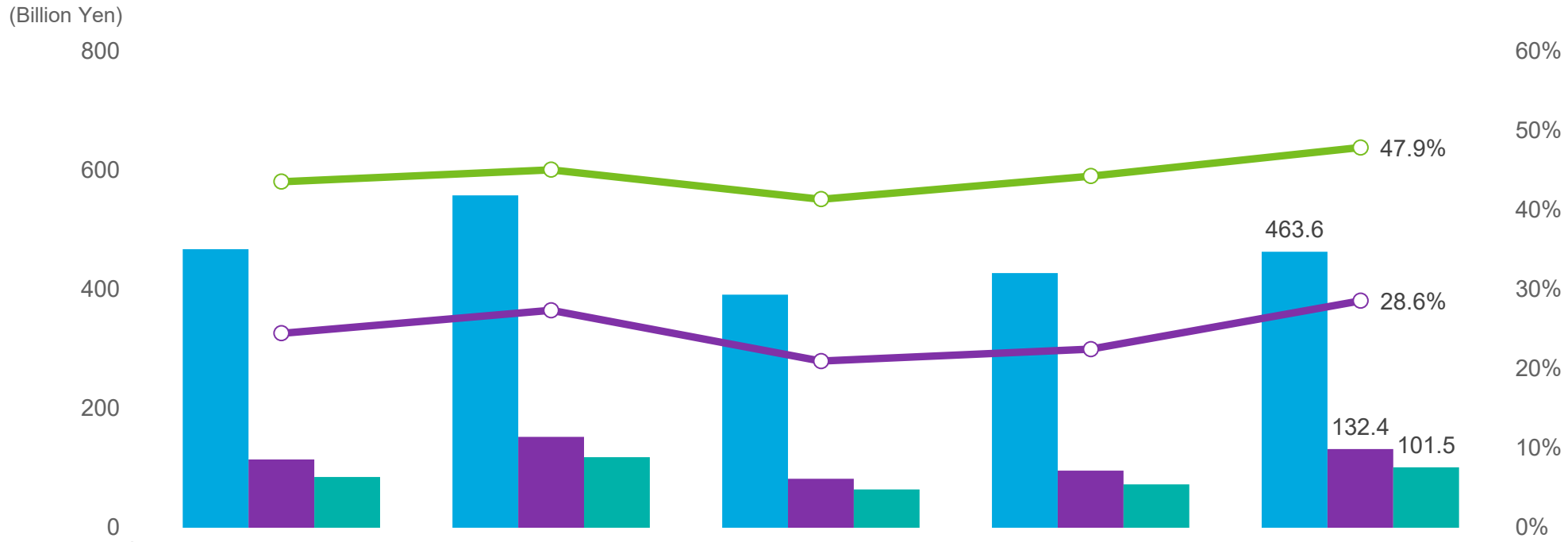
Financial Summary (Quarterly)

(Billion Yen)

	FY2023			FY2024		QoQ	YoY
	Q3	Q4	Q1	Q2	Q3	vs. Q2 FY2024	vs. Q3 FY2023
Net sales	467.8	558.2	391.7	427.8	**463.6**	+8.4%	-0.9%
Gross profit	203.9	251.6	162.3	189.7	**222.1**	+17.1%	+8.9%
Gross profit margin	43.6%	45.1%	41.4%	44.3%	**47.9%**	+3.6pts	+4.3pts
SG&A expenses	89.1	98.9	79.8	93.5	**89.6**	-4.2%	+0.6%
Operating income	114.7	152.7	82.4	96.1	**132.4**	+37.8%	+15.4%
Operating margin	24.5%	27.4%	21.0%	22.5%	**28.6%**	+6.1pts	+4.1pts
Income before income taxes	116.3	155.6	83.0	98.1	**134.4**	+37.0%	+15.6%
Net income attributable to owners of parent	85.5	118.6	64.3	73.1	**101.5**	+38.7%	+18.6%
R&D expenses	46.1	53.7	43.6	51.0	**49.7**	-2.4%	+8.0%
Capital expenditures	12.5	26.3	39.3	17.6	**31.8**	+80.5%	+153.2%
Depreciation and amortization	11.2	12.0	10.6	12.5	**13.8**	+9.7%	+22.6%

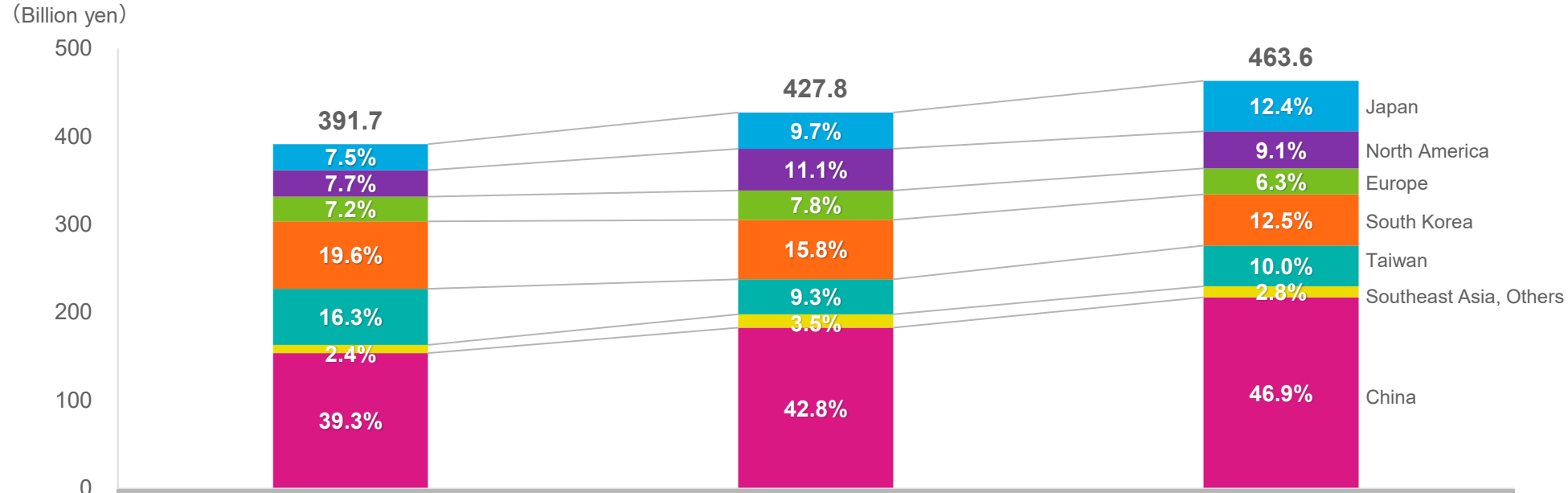
1. In principle, export sales of Tokyo Electron's products is denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of exchange rate fluctuations on profits is negligible, unless extreme fluctuations occur.
2. Profit ratios are calculated using full amounts, before rounding.

Financial Performance (Quarterly)



	FY2023		FY2024		
	Q3	Q4	Q1	Q2	Q3
Net sales	467.8	558.2	391.7	427.8	**463.6**
Operating income	114.7	152.7	82.4	96.1	**132.4**
Net income attributable to owners of parent	85.5	118.6	64.3	73.1	**101.5**
Gross profit margin	43.6%	45.1%	41.4%	44.3%	**47.9%**
Operating margin	24.5%	27.4%	21.0%	22.5%	**28.6%**

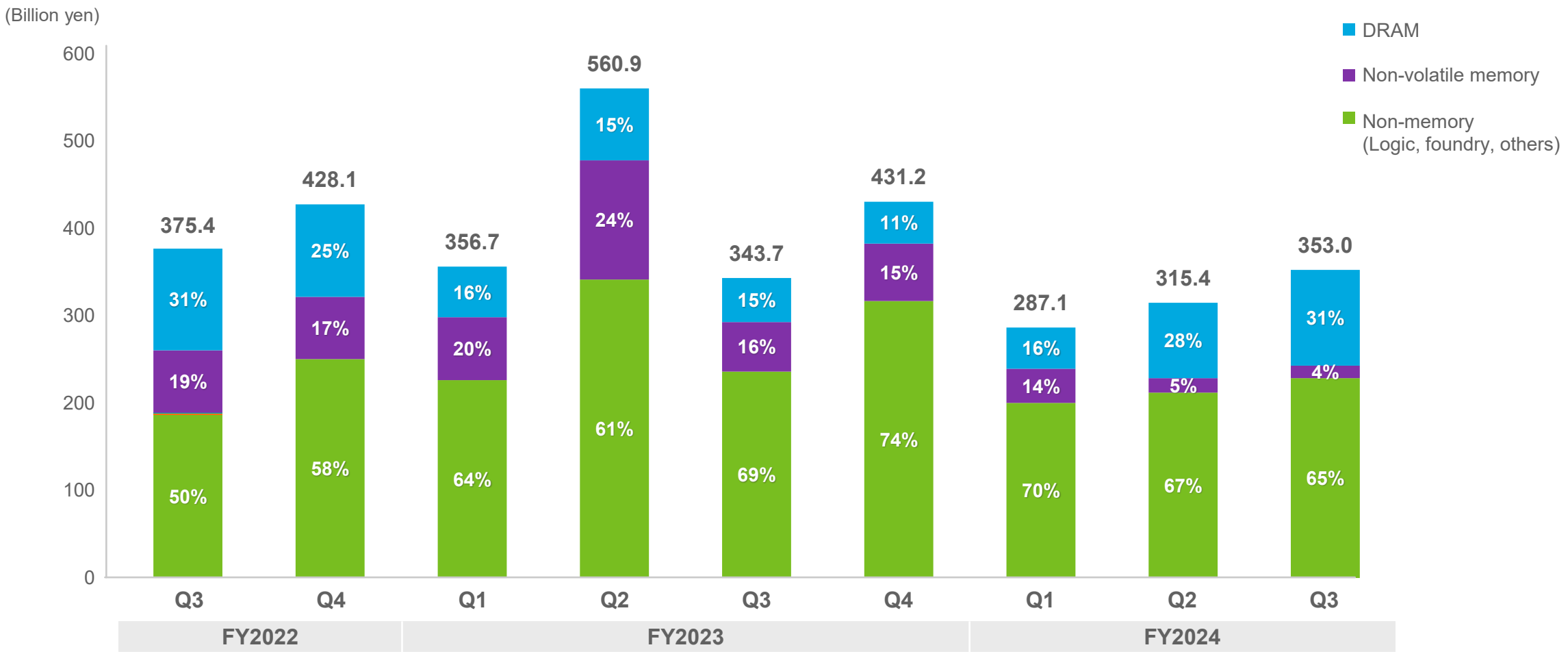
Composition of Net Sales by Region (FY2024 Q1-Q3)



	FY2024 Q1	FY2024 Q2	FY2024 Q3
Japan	29.5	41.2	**57.4**
North America	30.1	47.4	**42.1**
Europe	28.1	33.5	**29.4**
South Korea	76.7	67.4	**58.2**
Taiwan	63.9	39.9	**46.3**
Southeast Asia, Others	9.2	15.1	**12.7**
China	153.9	182.9	**217.2**

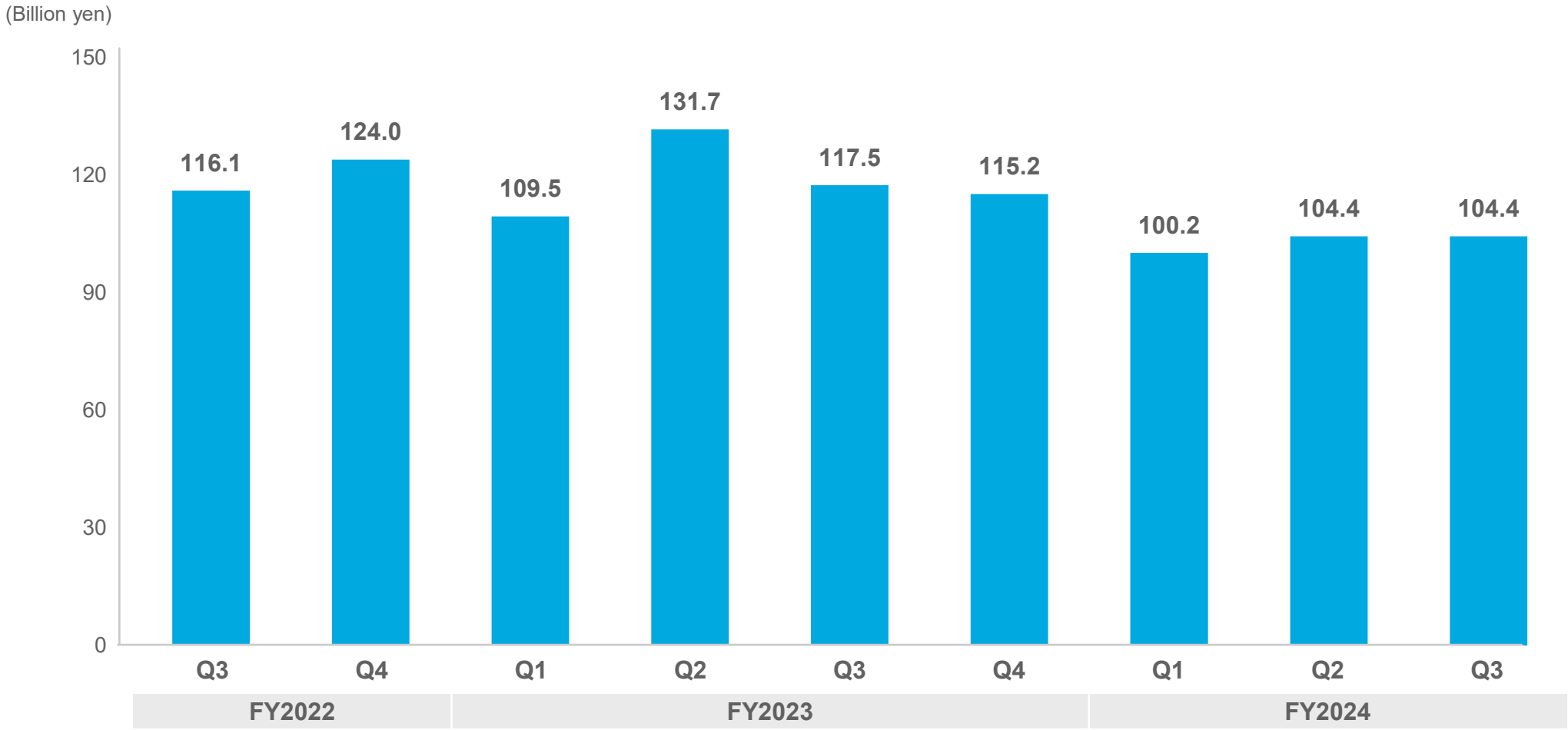
*Display production equipment sales are included

SPE New Equipment Sales by Application (Quarterly)



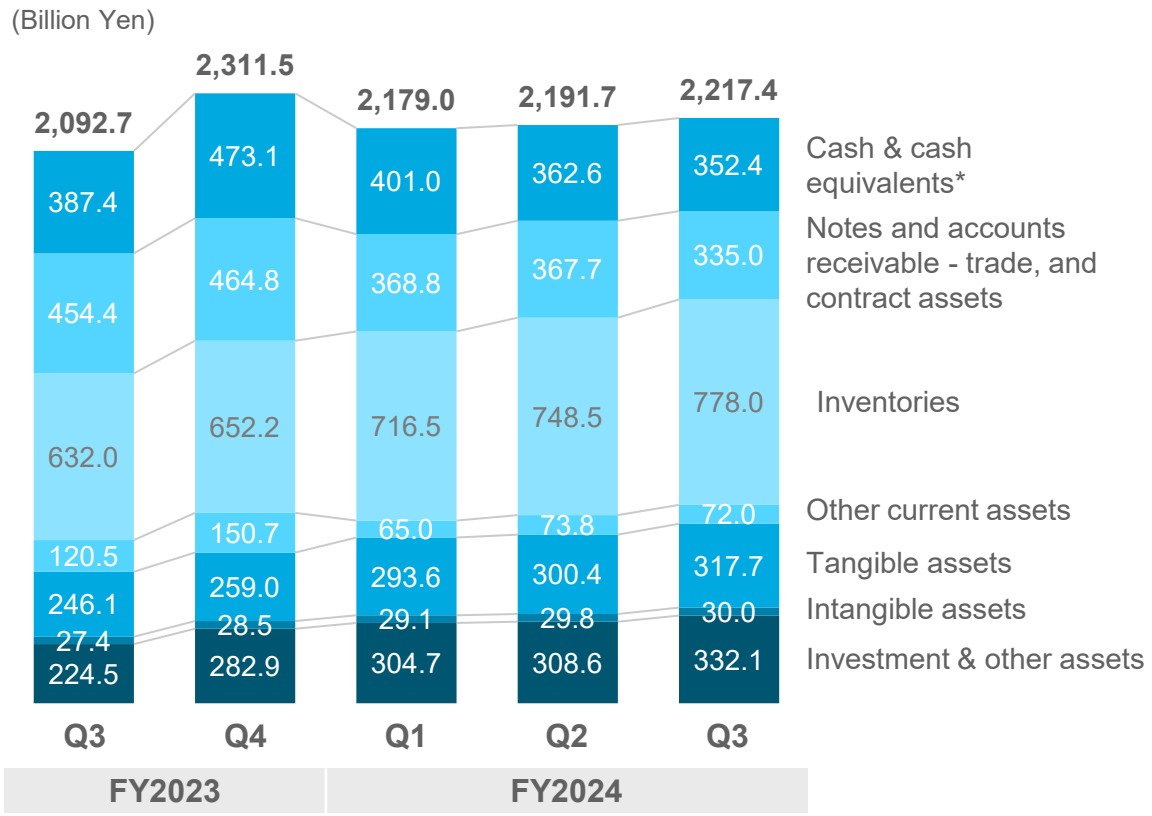
*1 SPE: Semiconductor production equipment
*2 Percentages on the graph show the composition ratio of new equipment sales. Field Solutions sales are not included.

Field Solutions Sales (Quarterly)

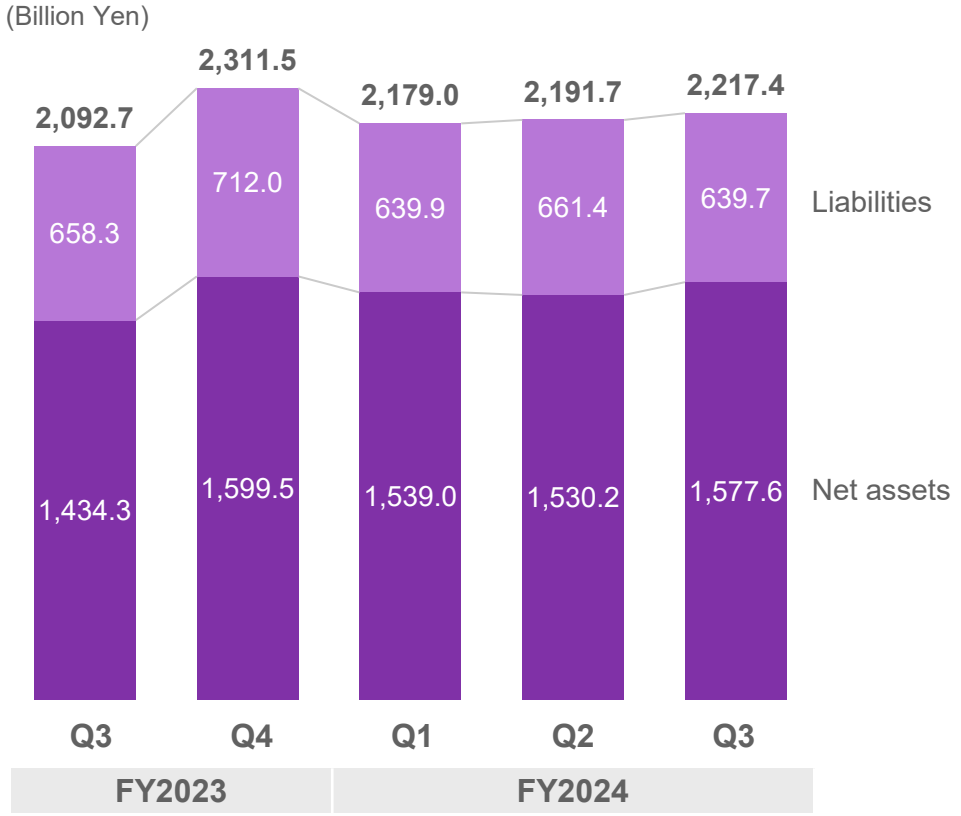


Balance Sheet (Quarterly)

Assets

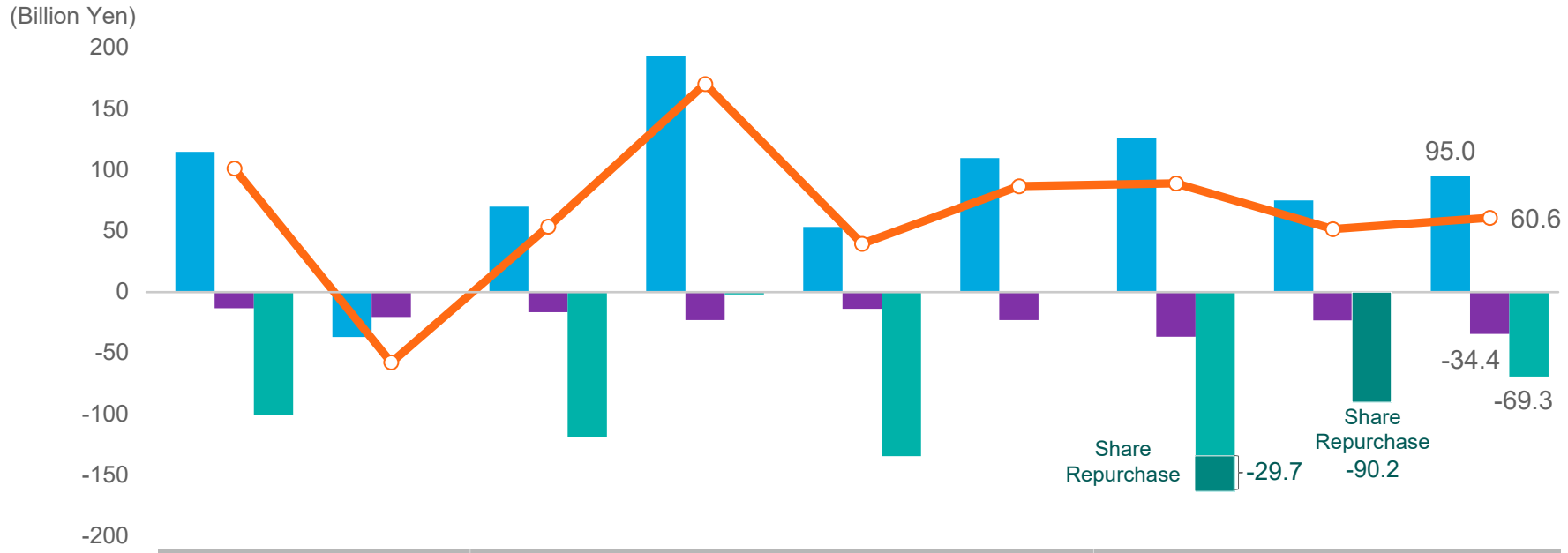


Liabilities & Net Assets



*Cash and cash equivalents: Cash and deposits + Short-term investments, etc. (Securities in B/S).

Cash Flow (Quarterly)



	FY2022		FY2023				FY2024		
	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
Cash flow from operating activities	114.6	-37.1	69.9	193.4	53.2	109.6	125.7	74.8	**95.0**
Cash flow from investing activities*1	-13.5	-20.7	-16.6	-23.1	-13.8	-23.1	-36.8	-23.4	**-34.4**
Cash flow from financing activities	-100.7	-0.2	-119.1	-2.1	-134.6	-0.5	-164.1	-90.8	**-69.3**
Free cash flow*2	101.0	-57.9	53.3	170.2	39.3	86.5	88.8	51.4	**60.6**
Cash on hand*3	423.9	371.2	314.6	484.6	387.4	473.1	401.0	362.6	**352.4**

*1 Cash flow from investing activities excludes changes in time deposits and short-term investments.

*2 Free cash flow = cash flow from operating activities + cash flow from investing activities (excluding changes in time deposits and short-term investments).

*3 Cash on hand includes cash and cash equivalents + time deposits and short-term investments with original maturities of more than three months.

Consolidated 10-year Financial Summary

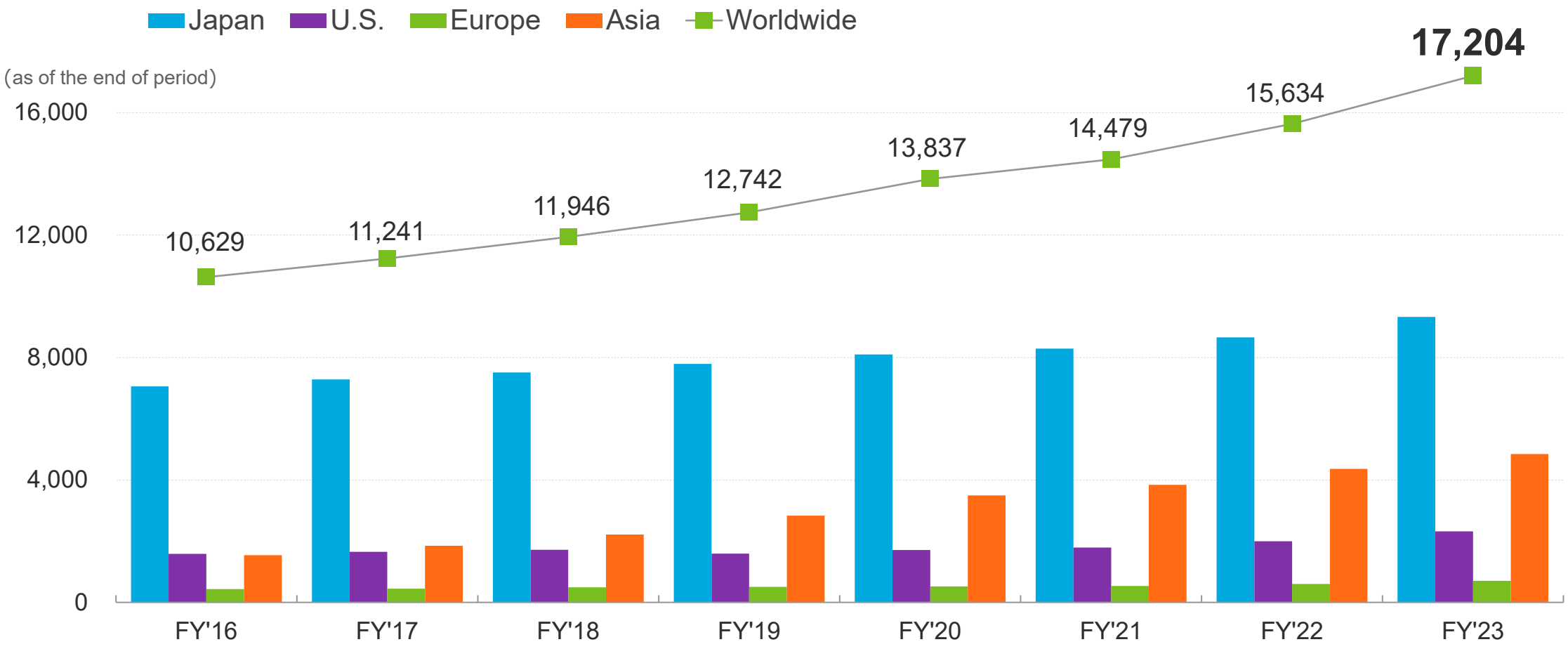
Millions of yen

	FY2014	FY2015	FY2016	FY2017	FY2018	FY2019	FY2020	FY2021	FY2022	FY2023
Net sales	612,170	613,124	663,948	799,719	1,130,728	1,278,240	1,127,286	1,399,102	2,003,805	2,209,025
Semiconductor production equipment	478,841	576,242	613,032	749,893	1,055,234	1,166,781	1,060,997	1,315,200	1,943,843	2,155,206
FPD production equipment	28,317	32,709	44,687	49,387	75,068	111,261	66,092	83,772	59,830	53,674
PV production equipment	3,805	3,617	-	-	-	-	-	-	-	-
Electronic components/ Computer networks	100,726	-	-	-	-	-	-	-	-	-
Other	479	555	6,228	438	425	197	197	129	131	144
Gross profit	201,892	242,773	267,209	322,291	475,032	526,183	451,941	564,945	911,822	984,408
Gross profit margin	33.0%	39.6%	40.2%	40.3%	42.0%	41.2%	40.1%	40.4%	45.5%	44.6%
SG&A expenses	169,687	154,660	150,420	166,594	193,860	215,612	214,649	244,259	312,551	366,684
Operating income	32,204	88,113	116,788	155,697	281,172	310,571	237,292	320,685	599,271	617,723
Operating margin	5.3%	14.4%	17.6%	19.5%	24.9%	24.3%	21.0%	22.9%	29.9%	28.0%
Ordinary income	35,487	92,949	119,399	157,549	280,737	321,662	244,979	322,103	601,724	625,185
Income before income taxes	-11,756	86,827	106,466	149,116	275,242	321,508	244,626	317,038	596,698	624,856
Net income attributable to owners of parent	-19,408	71,888	77,891	115,208	204,371	248,228	185,206	242,941	437,076	471,584
Depreciation and amortization	24,888	20,878	19,257	17,872	20,619	24,323	29,107	33,843	36,727	42,927
Capital expenditures	12,799	13,183	13,341	20,697	45,603	49,754	54,666	53,868	57,288	74,432
R&D expenses	78,663	71,349	76,286	83,800	97,103	113,980	120,268	136,648	158,256	191,196

	FY2014	FY2015	FY2016	FY2017	FY2018	FY2019	FY2020	FY2021	FY2022	FY2023
Interest-bearing debt	13,531	-	-	-	-	-	–	–	–	–
Equity	578,091	639,483	562,369	643,094	767,146	880,748	819,301	1,012,977	1,335,152	1,587,595
Total assets	828,591	876,153	793,367	957,447	1,202,796	1,257,627	1,278,495	1,425,364	1,894,457	2,311,594
Debt-to-equity ratio	2.3%	-	-	-	-	-	–	–	–	–
Equity ratio	69.8%	73.0%	70.9%	67.2%	63.8%	70.0%	64.1%	71.1%	70.5%	68.7%
ROE	-3.3%	11.8%	13.0%	19.1%	29.0%	30.1%	21.8%	26.5%	37.2%	32.3%
Cash flow from operating activities	44,449	71,806	69,398	136,948	186,582	189,572	253,117	145,888	283,387	10,965
Cash flow from investing activities	-19,599	155,737	-150,013	-28,893	-11,838	-84,033	15,951	-18,274	-55,632	-23,128
Cash flow from financing activities	-186	-18,213	-138,600	-39,380	-82,549	-129,761	-250,374	-114,525	-167,256	-5
Net income per share (Yen)	-36.10	133.69	153.70	234.09	415.16	504.53	390.19	520.73	935.95	1,007.82
Cash dividends per share (Yen)	17	48	79	117	208	253	196	260	468	570
Number of employees	12,304	10,844	10,629	11,241	11,946	12,742	13,837	14,479	15,634	15,883

1: From FY2019, the Company adopts “Partial Amendments to Accounting Standard for Tax Effect Accounting” (ASBJ Statement No. 28, revision on February 16, 2018). “Total assets” and "equity ratio" for FY2018 have been restated in the table in accordance with the revised accounting standard.
2: From the beginning of FY2022, the Company applies “Accounting Standard for Revenue Recognition” (ASBJ Statement No. 29).
3:The Company implemented a 3-for-1 common stock split on April 1, 2023. Net income per share and dividend per share (yen) are the figures after the stock split.

Worldwide Employees



- Disclaimer regarding forward-looking statement
  Forward-looking statements with respect to TEL's business plan, prospects and other such information are based on information available at the time of publication. Actual performance and results may differ significantly from the business plan described here due to changes in various external and internal factors, including the economic situation, semiconductor/FPD market conditions, intensification of sales competition, safety and product quality management, intellectual property-related risks, and impacts from COVID-19.

- Processing of numbers
  For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.

- Exchange risk
  In principle, export sales of Tokyo Electron's mainstay semiconductor and FPD production equipment are denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of exchange rate fluctuations on profits is negligible.

- Disclaimer regarding Gartner data (Page 6, 11)

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FPD: Flat panel display


TEL
60
years