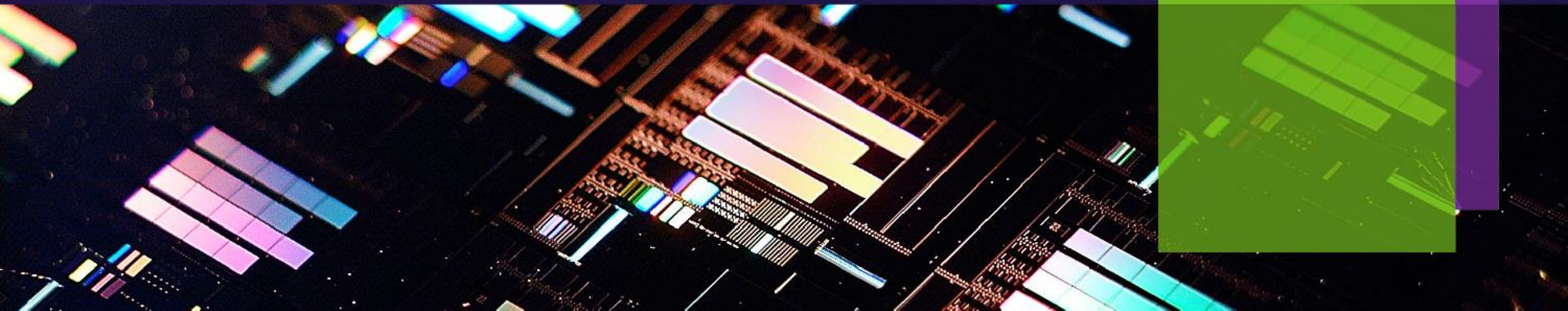
TOKYO ELECTRON

Tokyo Electron IR Day

October 12, 2021



Forward Looking Statements

- Disclaimer regarding forward-looking statements
  Forward-looking statements with respect to TEL's business plan, prospects and other such information are based on information available at the time of publication. Actual performance and results may differ significantly from the business plan described here due to changes in various external and internal factors, including the economic situation, semiconductor/FPD market conditions, intensification of sales competition, safety and product quality management, intellectual property-related risks, and impacts from COVID-19.
- Processing of numbers
  For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.
- Exchange risk
  In principle, export sales of Tokyo Electron's mainstay semiconductor and FPD production equipment are denominated in yen. While some settlements are denominated in dollars, exchange risk is hedged as forward exchange contracts are made individually at the time of booking. Accordingly, the effect of exchange rates on profits is negligible.

FPD: Flat panel display

Agenda

1. Opening 14:30-14:35
2. Presentation 14:35-16:45
   - Aiming to Be a Truly Excellent Company
   - Supply Chain Initiatives for the Environment
   - Technology Trends and TEL's Business Opportunities

     <Break, 10 minutes>
   - Challenges and Solutions for Advanced EUV Resist Process Technology
   - Latest Technological Challenges and TEL's Activities in Etch
   - TEL's Approach to Next Generation Film Deposition Technology
3. Q&A 16:45-17:30

TOKYO ELECTRON

Aiming to Be a Truly Excellent Global Company

October 12, 2021

Toshiki Kawai
Representative Director, President & CEO

Current World Situation

COVID-19 pandemic
Frequent natural disasters due to climate change
Geopolitical and human rights issues

Severe impact on people's lives

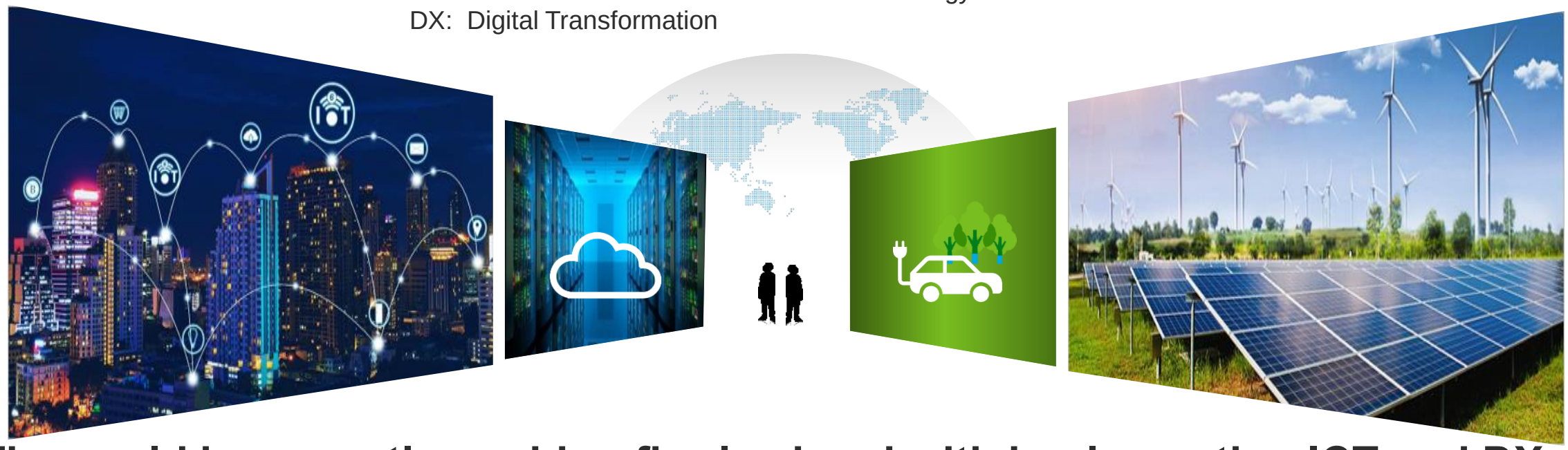
The Shape of a New Era

Semiconductors, essential for information and communication technologies, are conspicuously important

Trends Toward the Future

Digital (ICT/DX) × **Green (decarbonization)**

ICT: Information and Communication Technology
DX: Digital Transformation



The world is currently pushing firmly ahead with implementing ICT and DX, as well as taking action to realize a carbon-free society in order to build a strong and resilient society in which economic activities do not stop under any circumstances

Market Structure of Digitalization

Smartening across industries


Autonomous driving


Smart cities


Smart factories


Smart agriculture


Smart healthcare

ICT industry

Digital infrastructure

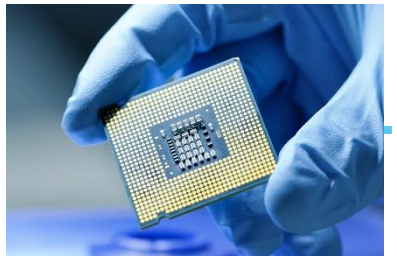
Semiconductors

Semiconductor production equipment

Video/music streaming, mobile apps, cloud services, mobile communication services, etc.

Data centers, 5G network, mobile devices, etc.

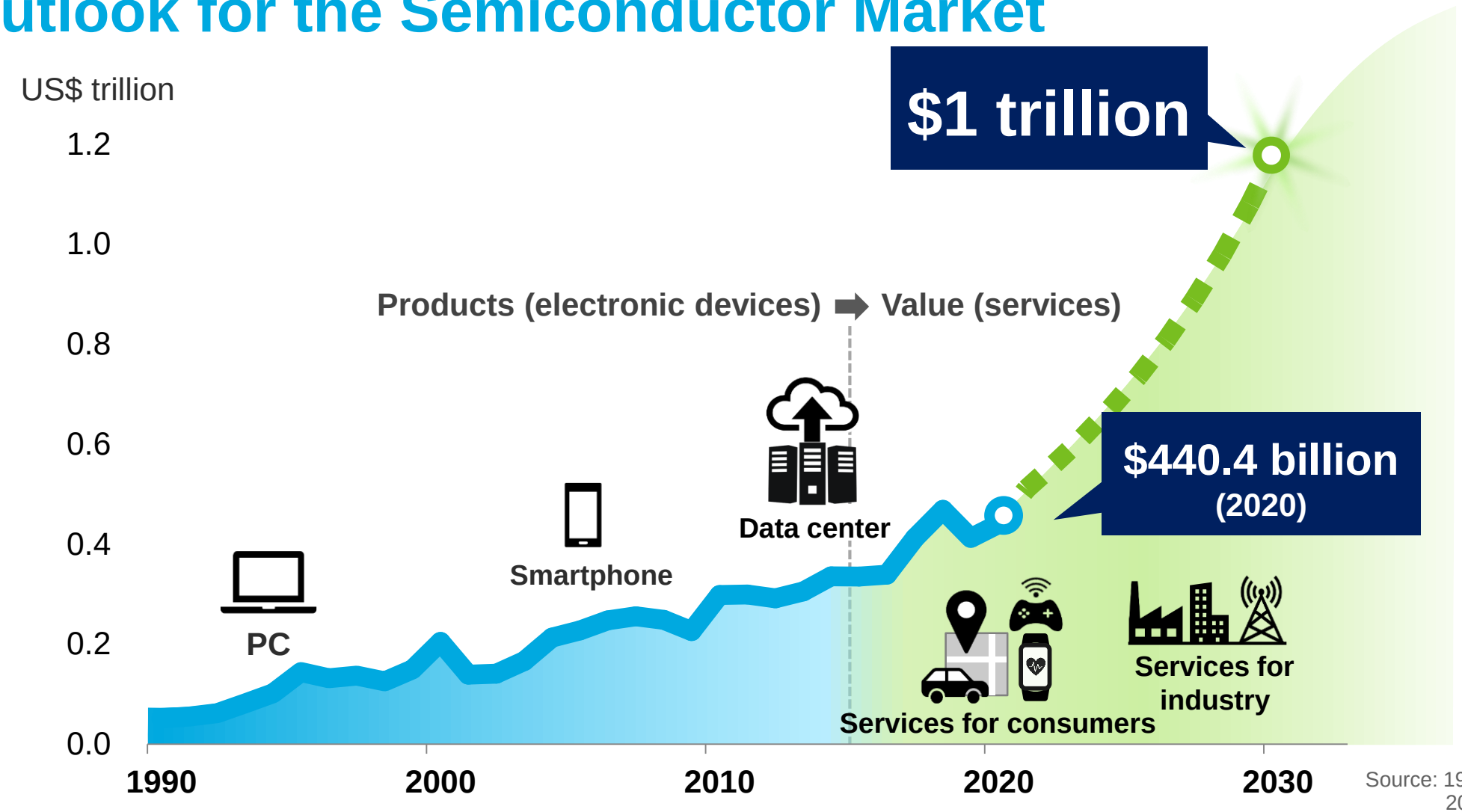
Semiconductors



“Key in industry and society”

Semiconductors are a critical infrastructure at the core of our social system

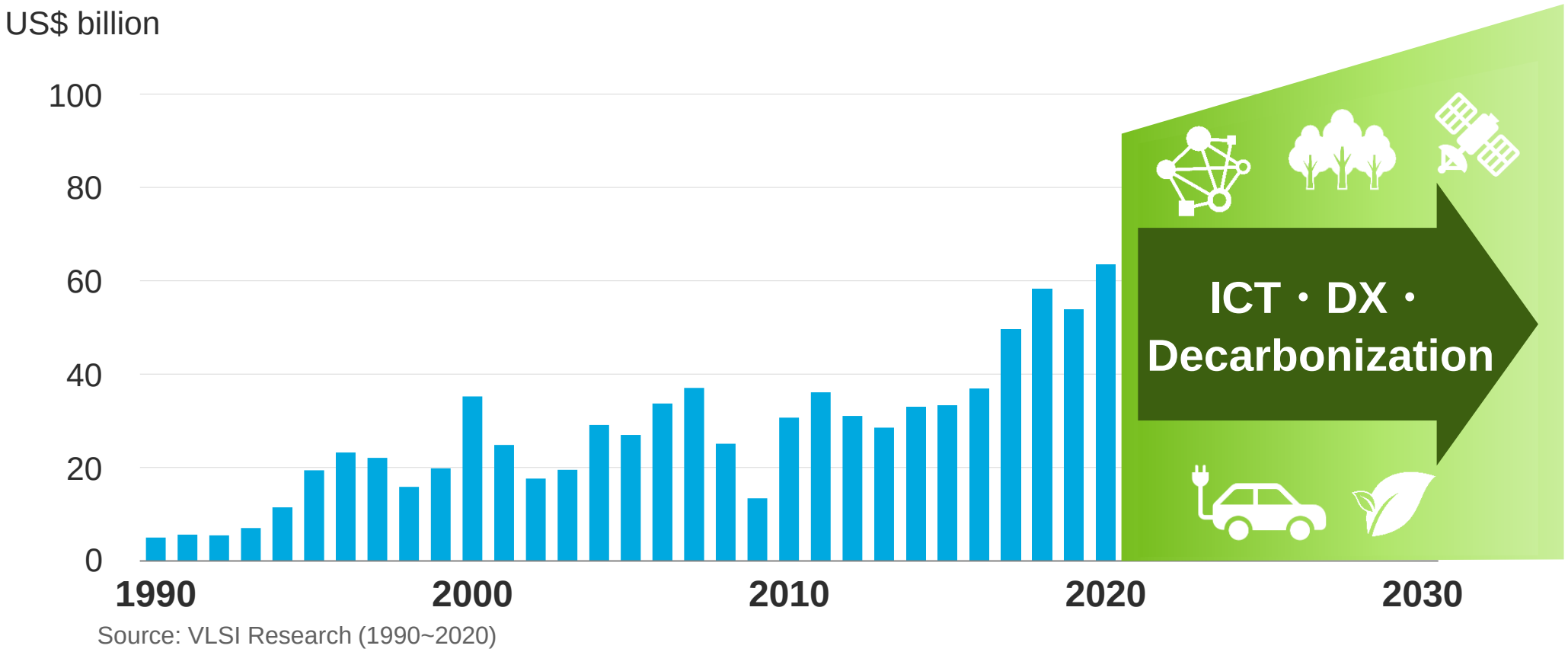
Outlook for the Semiconductor Market



Source: 1990~2020 (WSTS), 2021~2030 (IBS, April 2021)

To more than double in the next ten years

WFE* Market

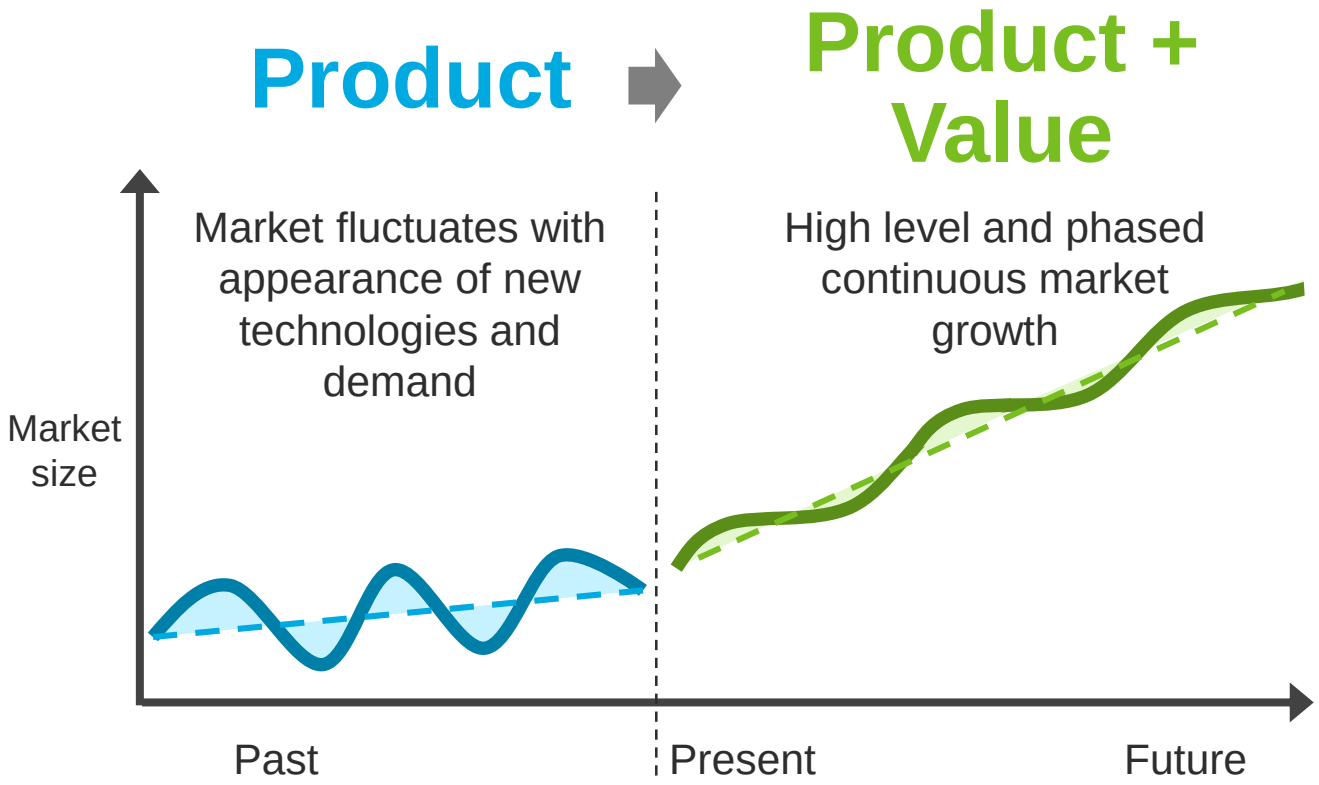


Source: VLSI Research (1990~2020)

Market being driven by technological innovation for ICT, DX and decarbonization

* WFE (Wafer fab equipment): Wafer fab equipment refers to the production equipment used in front-end production and in wafer-level packaging production.

WFE Market Trends



Background to changes in the market trend

1. From product to product + value
2. Diversification of applications
3. Continued innovation in semiconductor technology
4. Increased market visibility

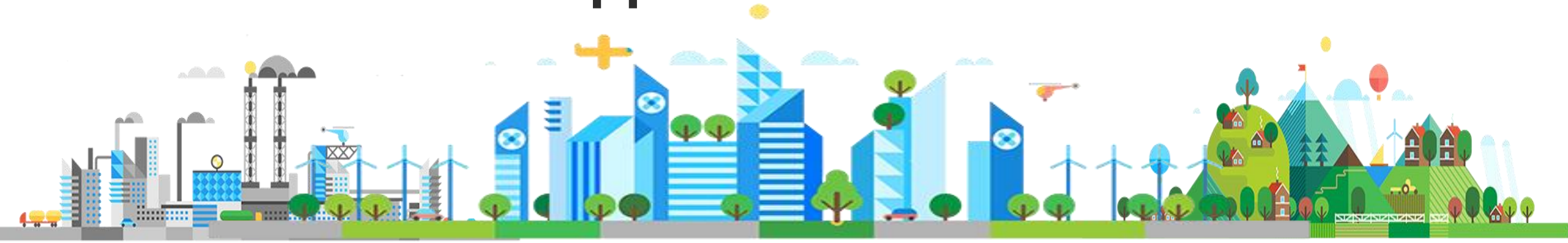
WFE market transitioning to a new growth phase

High expectations for semiconductors and production equipment market

TEL's role and responsibilities will grow further toward the future

Corporate Philosophy

We strive to contribute to the development of a dream-inspiring society through our leading-edge technologies and reliable service and support.



Practicing Our Corporate Philosophy (Creating Shared Value)

Applying our expertise developed as an industry leading equipment manufacturer and using all management resources – including our employees who both create and fulfill company values – we will contribute to realizing "Digital x Green" society through the pursuit of technological innovation in semiconductors

We will strive to expand profits in the medium to long term and continuously enhance our corporate value

to make people around TEL "Happy"

Integrated Report Published in August 2021

Report covering TEL's initiatives to achieve medium- to long-term profit growth and continuous improvement of corporate value

Important and Priority Material Issues

Leveraging Strengths

Only One

Have products in 4 sequential processes

Deposition | Coater/ developer | Etch | Cleaning

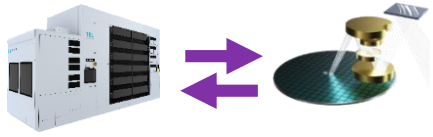
No.1

Products with the world's No. 1 or No.2 market share

Major products and market position

100%

Market share of coater/developer for EUVL



Coater/ developer | EUV lithography

No.1

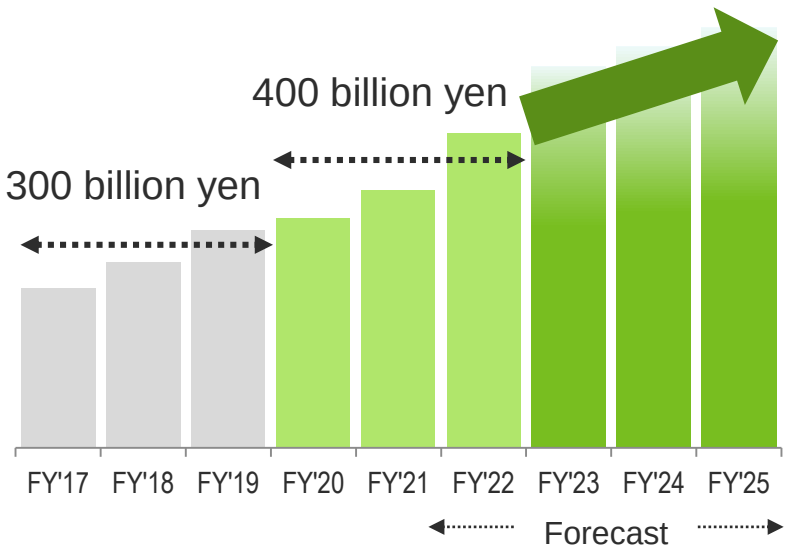
Worldwide install base

Annual increase by about 4,000 units

Industry's largest install base 78,000 units

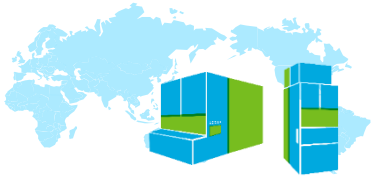
Aggressive Investment in R&D

Change in R&D Investment



- Have product lineup that drives semiconductor tech innovation
- Align tech roadmap spanning multiple generations with customers
- Offer optimal solutions for customers' both existing and upcoming lines through technical support

➔ Achieve high hit rate in product development



Contribute to realizing "Digital x Green" society by creating technologies that only TEL can provide

Building a Structure Ready for Business Expansion

Tohoku plant
new production building
Jul. 2020: began operation

Yamanashi plant
new production building
Aug. 2020: began operation

Miyagi plant
May 2021: acquisition of plant site

Building a structure for stable supply to respond to rapidly increasing demand for semiconductors

Building a Stable Supply Chain

Supply Chain Management

STQA: Supplier Total Quality Assessment

CSR and BCP Assessment

Investigation of conflict minerals, environmental laws and regulations, etc.

Miyagi Technology Innovation Center
(Construction completed Sep. 2021)

Support continuous industry growth through collaboration with partner companies

Value Chain Sustainability Initiatives

Global Initiatives

Sustainable Development Goals (SDGs)

Clarify initiatives through business by materiality and deploy company-wide

Tokyo Electron supports the SDGs

Participation in International Initiatives

Signed the UN Global Compact, joined the Responsible Business Alliance (RBA), endorsed the Task Force on Climate-related Financial Disclosures (TCFD)

WE SUPPORT UN GLOBAL COMPACT

Responsible Business Alliance
Affiliate Member

TCFD TASK FORCE ON CLIMATE-RELATED FINANCIAL DISCLOSURES

External Evaluation on our ESG Initiatives

Highly rated by evaluation organizations around the world

Member of
Dow Jones Sustainability Indices
Powered by the S&P Global CSA

FTSE4Good

2021 MSCI ESG Leaders Indexes Constituent

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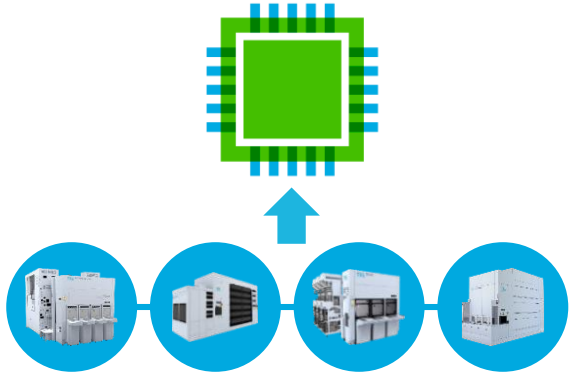
Environmental Approach

Innovation in Semiconductor

Contribute to higher performance and lower energy consumption



Product and Operation

Medium-term environmental goals for 2030 CO_2 emissions reduction targets

Products

30%reduction

Per wafer
(vs. 2018)

Facilities

70%reduction

of total emissions (vs. 2018)

Ratio of renewable energy 100%

Supply Chain

Pursue "Digital × Green" society throughout the supply chain

E-COMPASS

Environmental Co-Creation by Material, Process and Subcomponent Solutions

Best Products・Best Technical Service

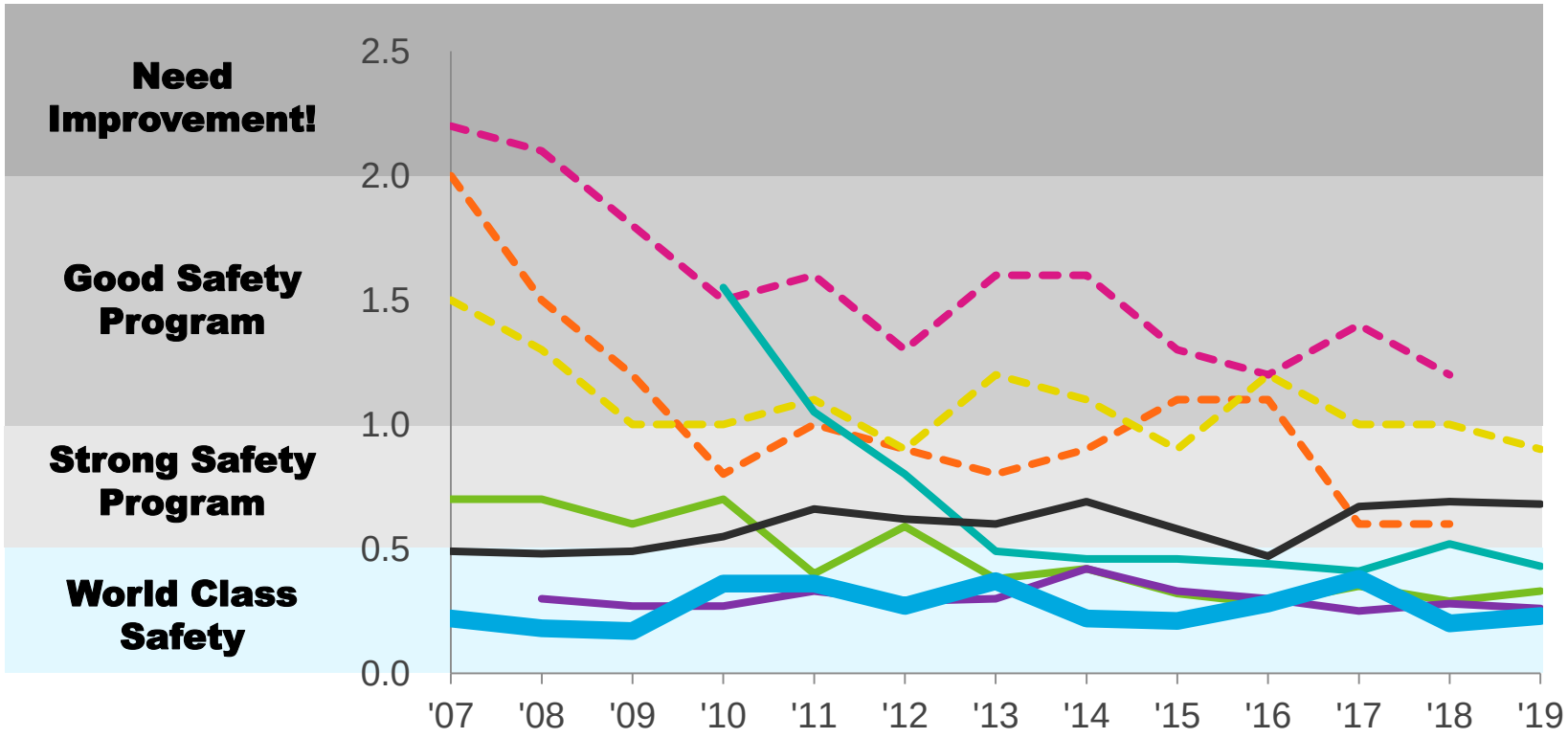
Environmental Performance

Strengthen initiatives throughout our business and supply chain toward realization of a carbon-free society

World Class Safety

TCIR (The number of workplace incident per 200,000 work hours)

TCIR: total case incident rate



Source: U.S. Bureau of Labor Statistics, or figures announced by each company (all except TEL use the calendar year)

Aiming for zero incidents

Corporate growth is about people
Employees both create and fulfill company values

TEL Values as Code of Conduct

Motivation-oriented Management

Diversity & Inclusion

3Gs

Global・Generation・Gender

TEL Values as Code of Conduct

Pride

We take pride in providing high-value products and services.

We offer our customers cutting-edge technological products, along with the highest level of quality and technical service, in the pursuit of total customer satisfaction.
We consider profit to be an important measure of value in our products and services.

Challenge

We accept the challenge of going beyond what others are doing in pursuing our goal of becoming number one globally.

We view changes as opportunities and respond to them flexibly and positively.
We are tolerant of failure and consider it important to learn from the process and results.

Ownership

We will keep ownership in mind as we think things through, and engage in thorough implementation in order to achieve our goals.

We always have an awareness of problems and tackle challenges with enthusiasm and a sense of responsibility.
We make decisions quickly and do what we consider to be the best course of action.

Teamwork

We respect each other's individuality and we place a high priority on teamwork.

We create a workplace with an open atmosphere and positive communication.
We establish relationships of trust with our business partners in order to facilitate mutual growth.

Awareness

We must have awareness and accept responsibility for our behavior as respectful members of society.

We strictly comply with laws and regulations and the rules of society.
We give top priority to safety, health and the global environment.
We strive to become a company that local communities hold in high esteem.

Human Rights

Global Reach	Employees	Suppliers
76 sites in 18 countries & regions	Approx. 15,000	Approx. 1,000

Contribute to developing a dream-inspiring society by emphasizing a way of thinking that respects human rights based on a high ethical standard throughout the supply chain

Further Increasing Corporate Value

Offence

Achieve world-class operating margin and ROE of over 30%

&

Offence

- Safety
- Quality
- Compliance
- Engagement
- Risk management & Security

Semiconductors/FPD = Future

Creating technologies that the world has never seen

Continue to take on challenges and evolve


Aiming to Be a Truly
Excellent Global Company

TOKYO ELECTRON

E-COMPASS

Supply Chain Initiatives for the Environment

October 12, 2021

Sumie Segawa
Vice Division GM, Corporate Innovation Division

Supply Chain Initiative Focused on the Environment

E-COMPASS

Environmental Co-Creation by Material, Process and Subcomponent Solutions

Infinity

Represents the sustainable use of resources and energy, and relationships with lasting relationship with stakeholders

Color gradation

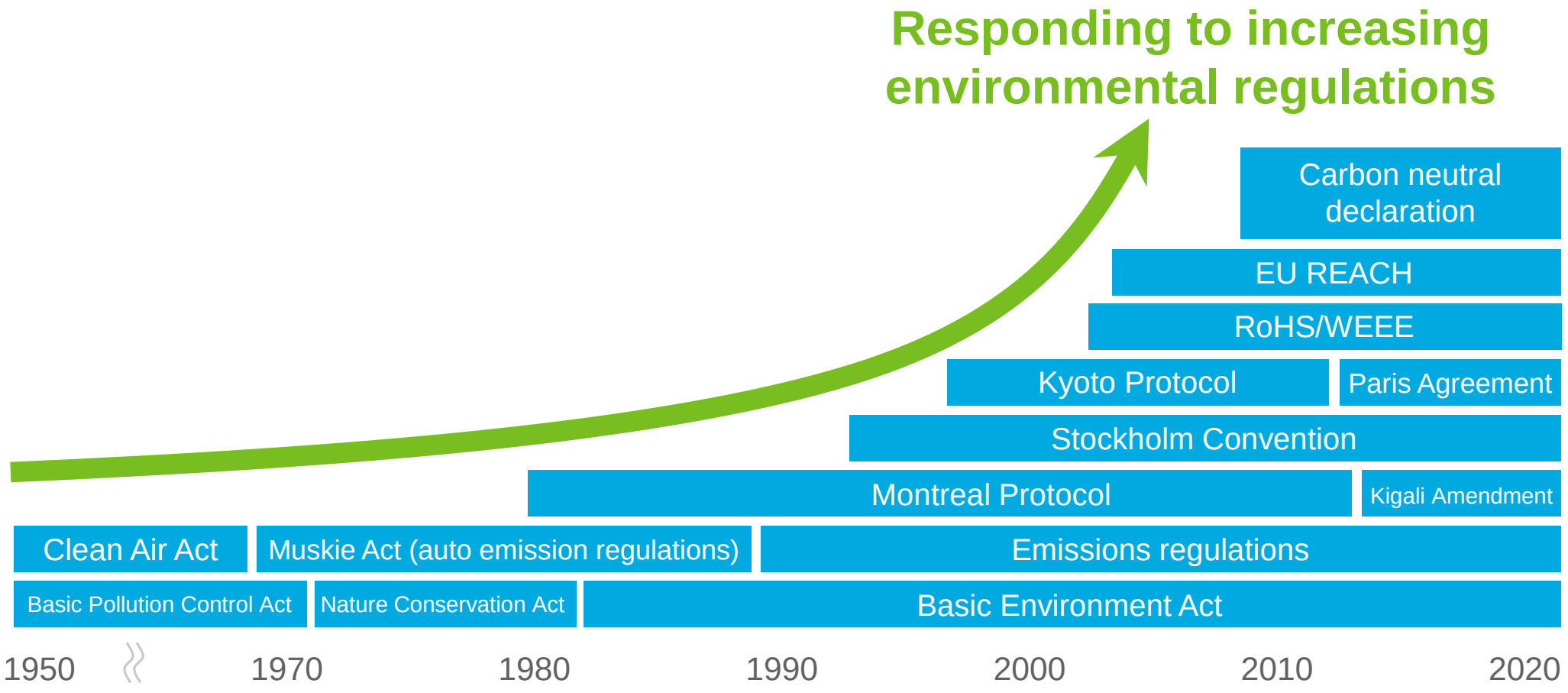
Represents the ongoing reforms to reduce environmental burdens via co-creation with partner companies in business activities

Important initiatives for realizing the “Digital × Green” society

Background 1: Disasters Caused by Climate Change

Multiple unprecedented natural disasters are occurring around the world and environmental consciousness is rising

Background 2:
Trend of Environmental Conventions and Regulations



Proactive response is essential to ensure sustainability of business activities

Background 3: TEL's Duty as an Industry Leader

Digital (ICT / DX) × **Green** (decarbonization)

TEL will assertively drive the industry toward a sustainable society

E-COMPASS Mission / Vision / Values

Mission	**Aim to reduce the environmental impact on the Earth** by raising the green performance of the microelectronics industry through collaboration with and encouragement of the entire supply chain
Vision	**Work with leading-edge environmental technology** throughout the supply chain to co-create a sustainable and prosperous future where humans and nature co-exist
Values	Provide microelectronics **manufacturing and equipment technologies** with excellent green performance, **regulatory compliance**, and **reduced environmental impact from operations**

Pursue the “Digital × Green” society

We strive to contribute to the development of a dream-inspiring society through our leading-edge technologies and reliable service and support

Activities of E-COMPASS

Activities

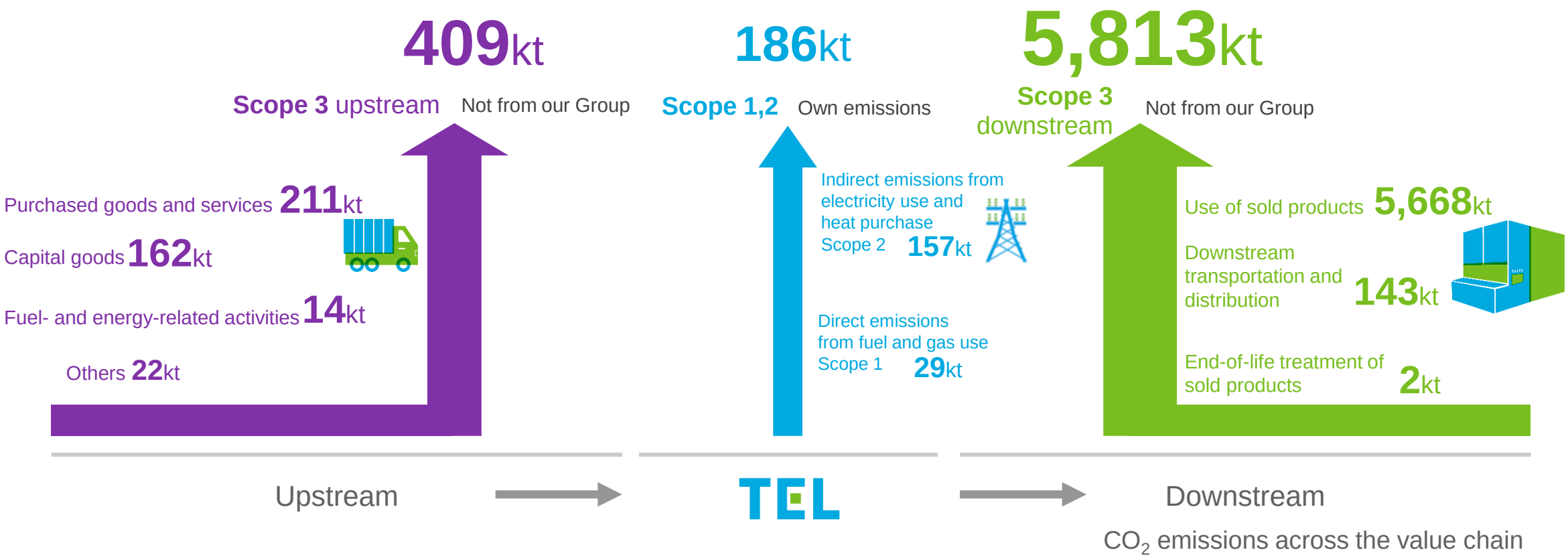
Partnership strengthening	Environmentally hazardous substances-free equipment	Development of equipment with proactive environmental performance

Results

Pursuing sustainability throughout the industry	Delivering environmental friendly products	Production technology innovation by environmental technology

Reducing environmental burden throughout the supply chain
and promoting innovations in environmental technology

Activity 1: Partnership Strengthening for Reducing CO_2 Emissions



Raising green performance of the semiconductor industry
through collaboration with and encouragement of the entire supply chain
to reduce environmental impact on the Earth

Case Study:
Initiatives to Reduce Environmental Impact in Supply Logistics

Shifting from truck to rail transport

TEL plants (Miyagi, Kumamoto prefectures) ⇔ Partner companies (Kansai region)

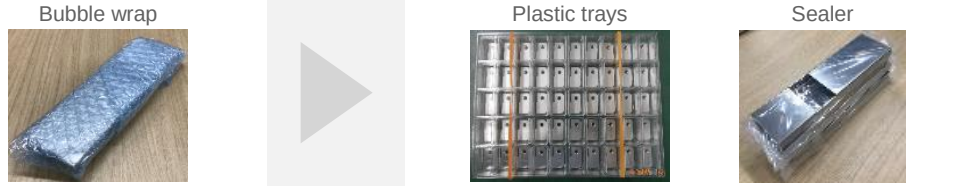
162t CO_2 emissions reduction

Efforts to reduce packaging materials

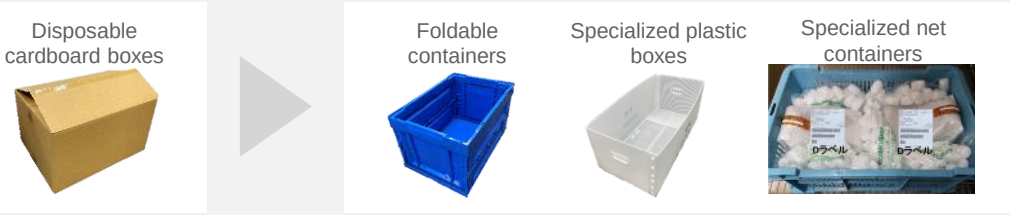
Cardboard box reduction: approx. 14,000/year

CO_2 emissions reduction: 10.6t-CO_2/year

①Reduced bubble wrap usage



②Reduced cardboard box usage



Reducing supply chain CO_2 emissions through modal shifts and packaging reform

Activity 2: Environmentally hazardous substances-free equipment

Build relationships of trust with stakeholders
by providing products that can be used safely long-term

Establish supply chain that provides products with minimal environmental impact

Case Study:
Identifying Future Trends and Establishing Alternative Methods

Proactively identifying substances of concern for adverse effects on the environment and human health, work with partner companies to determine alternatives and reduce environmental impact

Understanding future regulations	Identify substances of concern for adverse effects on the environment - Proactive response based on leading EU / US policy and regulatory trends
Examining alternative methods	Technological cooperation with partner companies - Evaluation/adoption of materials free of environmentally hazardous substances - Implement alternatives through technological innovation
Emissions reduction initiatives	Co-creation with suppliers - Pursue methods to maximize resources and minimize the release of hazardous substances to the environment

Equipment free of environmentally hazardous substances

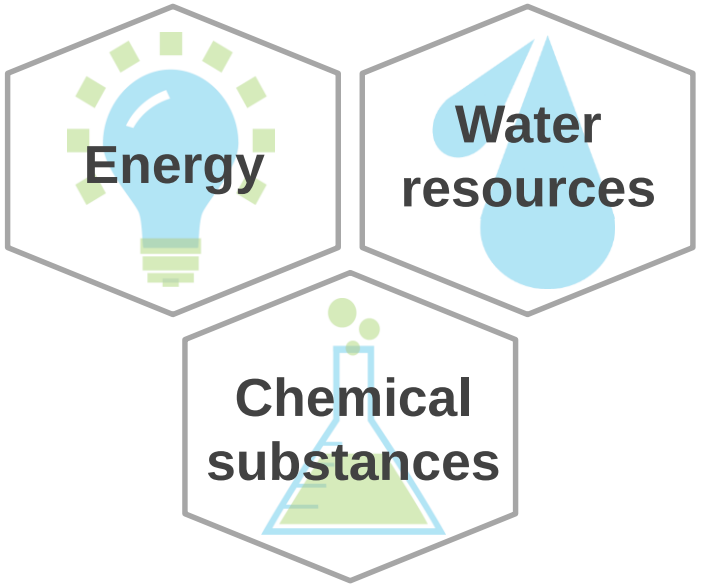
Promoting reduction of environmental impacts through identifying future trends and technological innovation

Activity 3:
Development of equipment with proactive environmental performance

**In addition to safety and performance specifications,
set environmental performance as a core, we will provide more value-add products**

Standardization of environmental specifications

Accelerate technological innovation in multiple fields



Accelerating technological innovation utilizing equipment
with environmental performance as new competitive edge

Miyagi Technology Innovation Center

Began operating a technology innovation center with the aim of innovation in next generation production technology

- Driving development of innovative production technology that improves the performance, quality and lead time of TEL products
- Promoting collaboration as a location for facilitating **co-creation with partner companies**
- Accelerating the **development of environmental technologies** focused on the future

Accelerating further evolution of manufacturing equipment through co-creation with partner companies

Pursuing Further Partnerships

Corporate Philosophy

“We strive to contribute to the development of a dream-inspiring society through our leading-edge technologies and reliable service and support”

Pursue “Digital × Green” society throughout the supply chain

E-COMPASS

Environmental Co-Creation by Material, Process and Subcomponent Solutions

Best Products・Best Technical Service

Environmental Performance

Accelerating global activities in pursuit of a wide range of partner companies and seed technologies

TOKYO ELECTRON

Technology trends and TEL's business opportunities

October 12, 2021

Akihisa Sekiguchi, Ph.D.
Deputy GM, Corporate Innovation Division

Overview

- Composition of market, semiconductor market, data processing and growth
  - Warm up
  - Accelerating Data Creation through data launching platforms, communication & Analytical Intelligence (AI, Quantum)
- Future device evolution and R&D trends
  - System integration
  - Device, design, technology co-optimization, and hybrid devices
- Current status and direction of logic, memory and CIS technology
  - Continuation of scaling but with higher technical hurdles
  - Alternative solutions, innovation needed but fundamentally evolution of current tool lineup covers
- Summary

Composition of Market, Semiconductor Market, Data Processing and Growth

Evolution of Automobiles

The advantage of the Ford Model T is that it works even without the use of semiconductors

Evolution of Automobiles as a Technology Platform

Semiconductors
- Logic: CPU, GPU, controller, AI
- Memory: NAND, DRAM
- Sensors: CIS, radar, vision, LIDAR
- Power: convertors, regulators, generators
- Communication: 5G
- Displays: projectors, panels

Material
- Body: lighter composite, recyclable

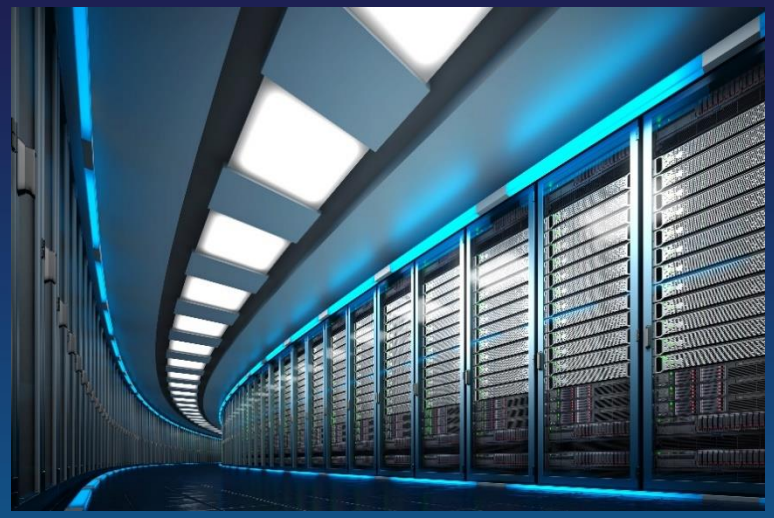
Communication and Decision Making
- Local vs. networked

Autonomous driving cars are already at the core of the technology platform

Evolution of Communication Networks

5G (cloud) and edge (local) data processing are indispensable for autonomous driving cars to become more widespread

Evolution of Servers and Accelerators

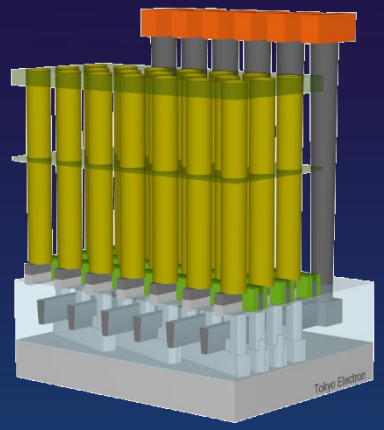


Source: Shutterstock

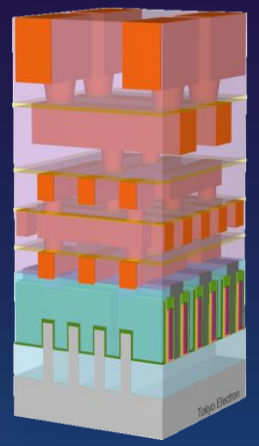
Cloud evolution is also essential for processing ever-growing data

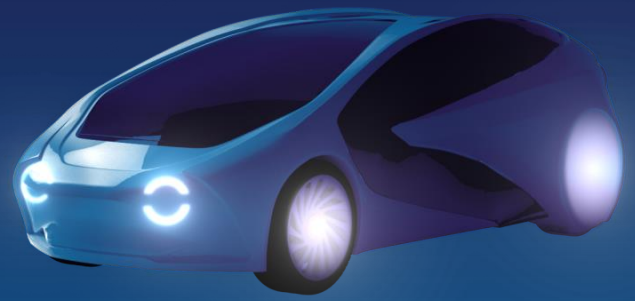
In-vehicle Semiconductors

Working memory



AI & Data processing





Storage memory

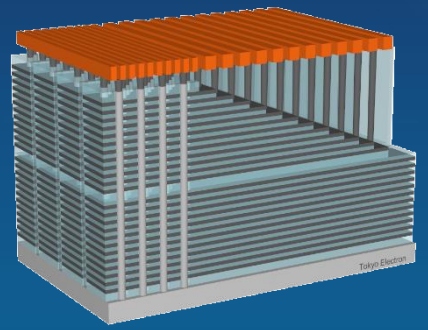
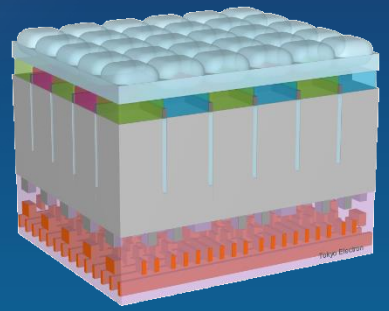


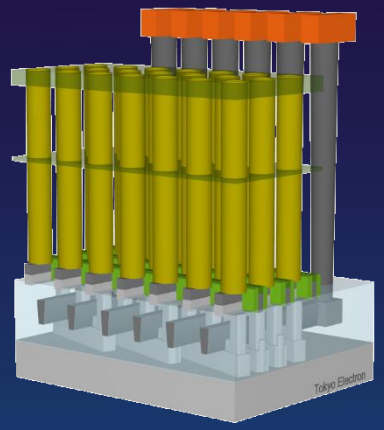
Image sensing



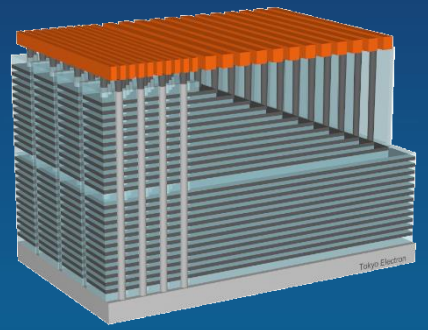
Platform (PF) needs drive system evolution

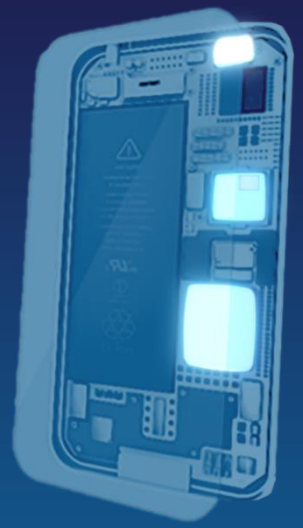
The Abundance of Advanced Semiconductors Found in Smartphones

Working memory



Storage memory





AI & Data processing

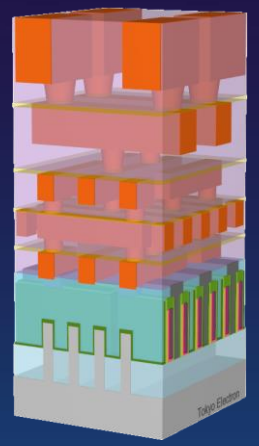
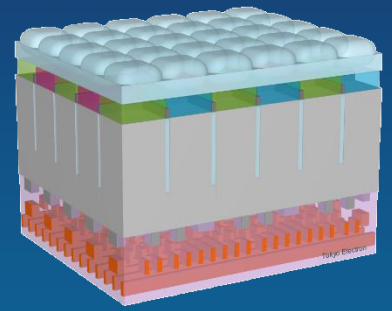


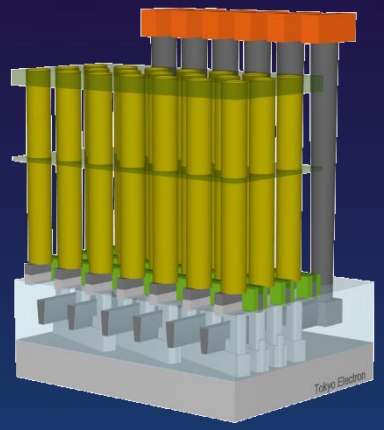
Image sensing

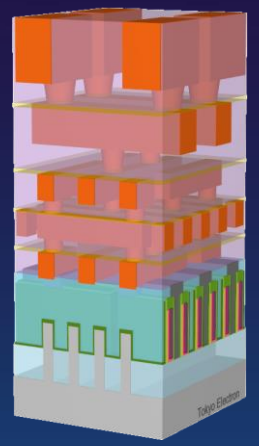


Smartphones still the representative portable and mobile platform

Internet of People

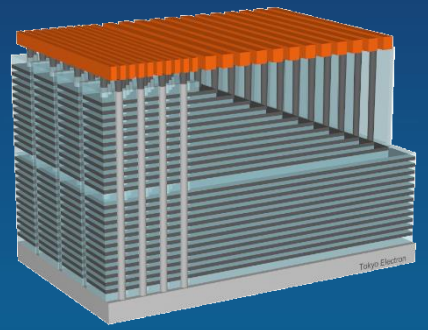
Working memory





AI & Data processing

Storage memory



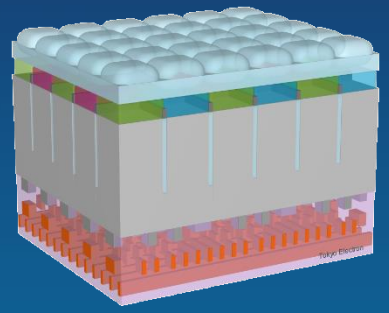
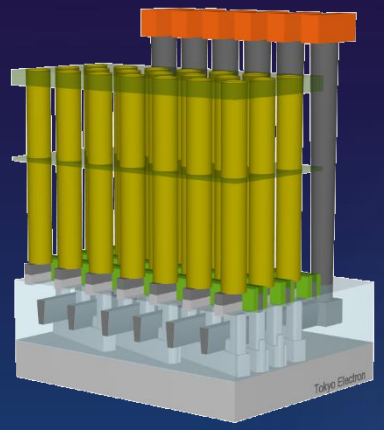


Image sensing

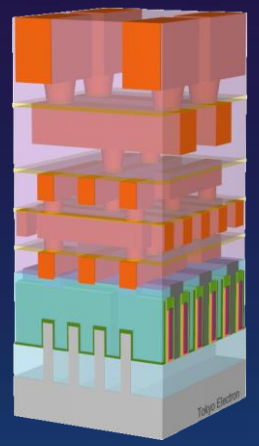
A tech platform by which even humans equip themselves with sensors, CPUs and comms systems

Internet of Animals? ...Bio-logging Technology

Working memory



AI & Data processing



Storage memory

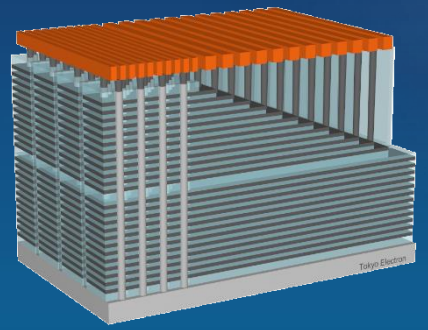
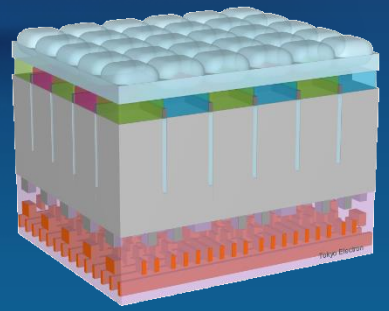


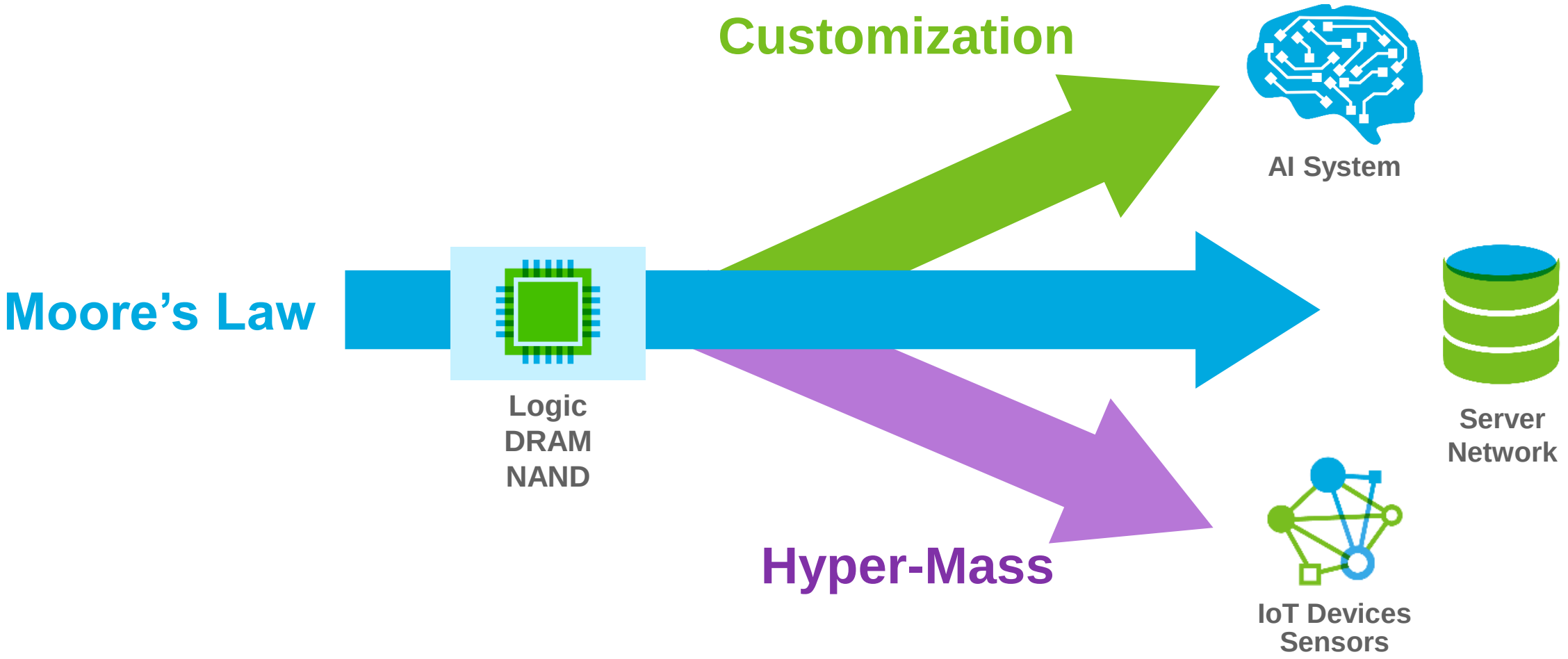
Image sensing



A by-product of the pet boom amid the coronavirus pandemic

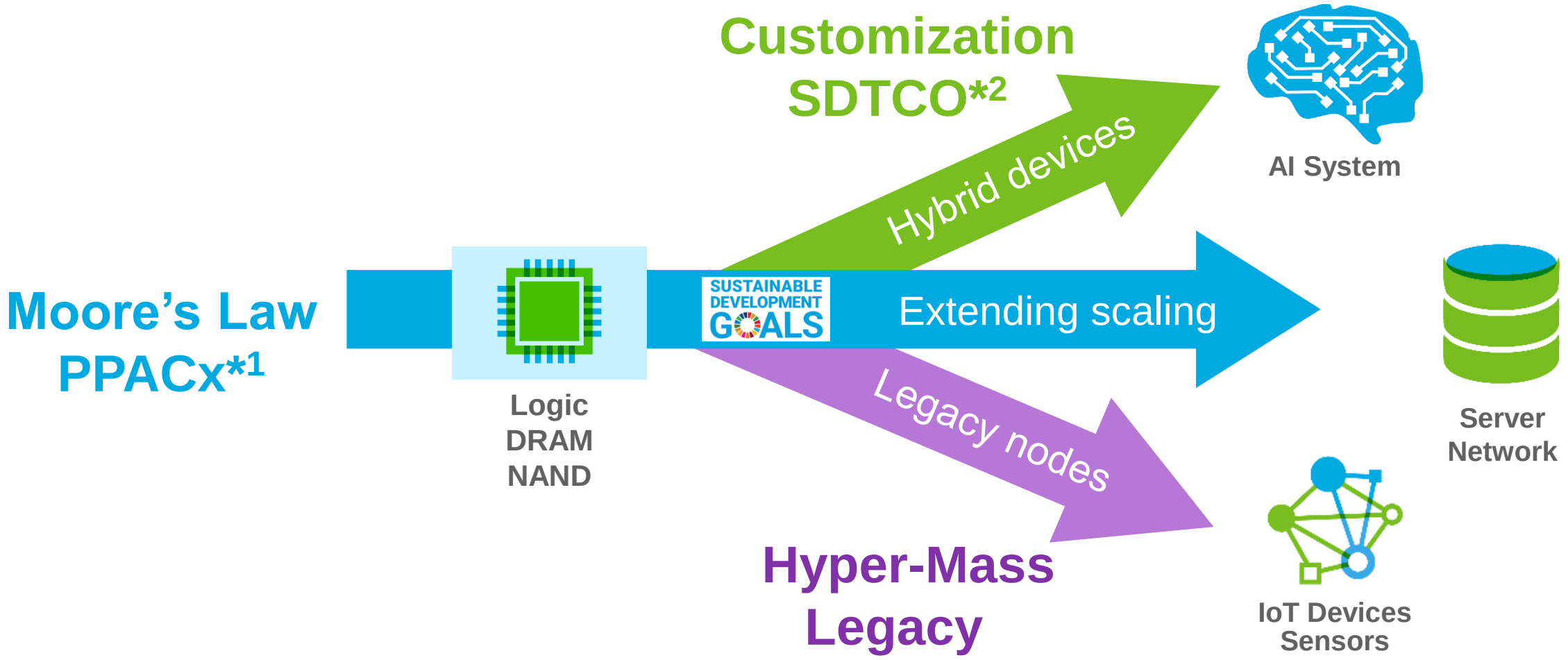
Future Device Evolution and R&D Trends

Previously Mentioned Trends Coming in the Next 10 Years



Response to diversifying applications

Roadmap for the Next 10 Years

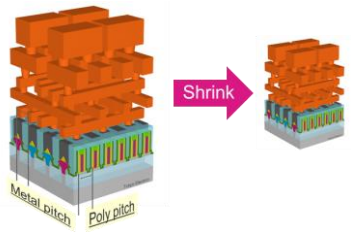


Development of SDGs-compatible technology for incorporation into diversifying applications

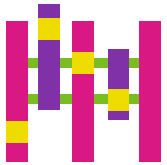
*1 PPACx: Power performance area cost, x
*2 SDTCO: System design technology co-optimization

Advances in System Integration

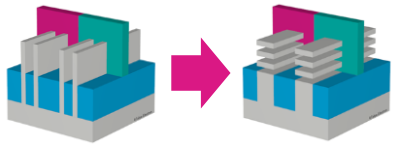
Logic: More transistors



2D shrink

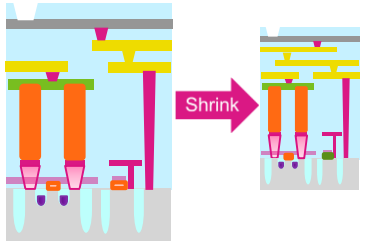


DTCO

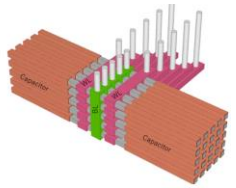


New structure

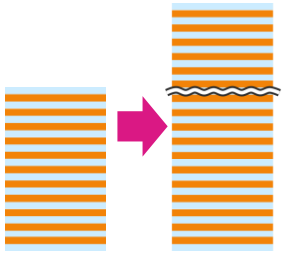
Memory: More bytes of DRAM, NAND



2D shrink

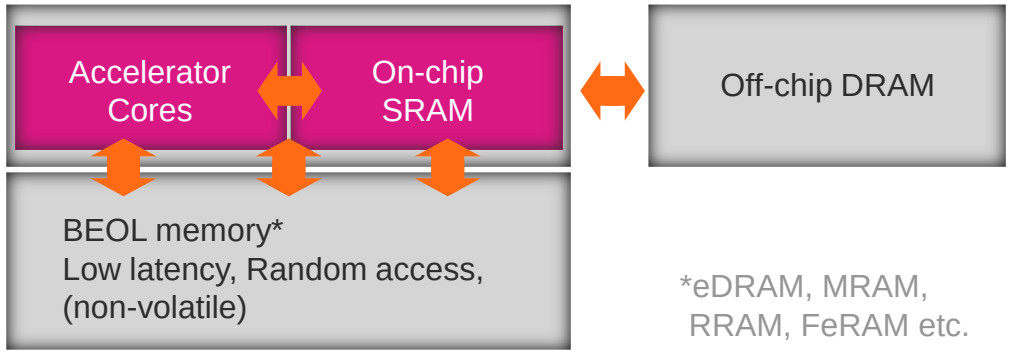


New structure



More stack

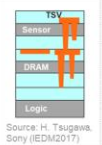
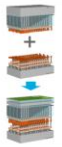
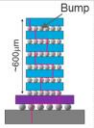
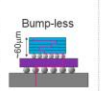
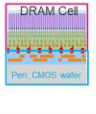
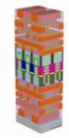
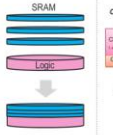
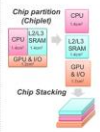
BEOL: More layers including memory



*eDRAM, MRAM,
RRAM, FeRAM etc.

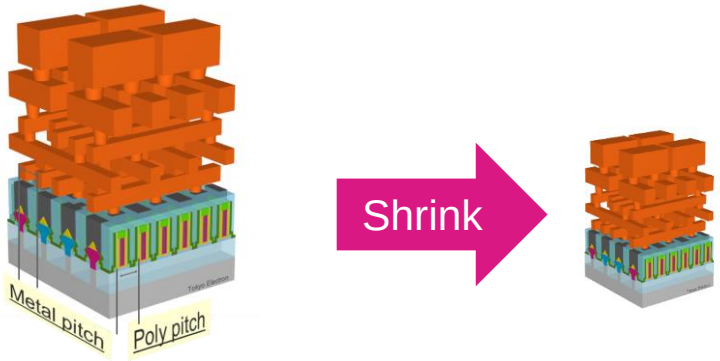
System Integration: More options

Source: TEL estimates

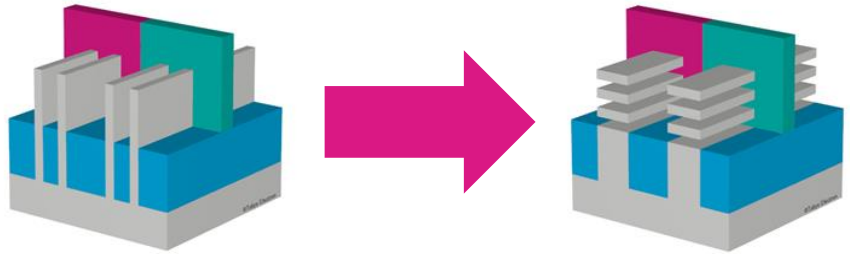
Device	CIS	3D NAND	DRAM			Logic		
Stacking	Sensor+ DRAM + Logic	Cell + Peri	HBM (w/ Bump)	HBM (Bump-less)	Cell + Peri	Backside PDN	Logic + SRAM Cell	3D Hybrid Logic + I/O + RF
Bonder Type	W-W	W-W	D-W	W-W		W-W	W-W/D-W	D-W
	Fusion (Permanent)	Fusion (Permanent)	Temporary (Bonding / De-bonding)	Fusion (Permanent)		Fusion (Permanent)		Temporary & Fusion
	Cu to Cu Hybrid	Cu to Cu Hybrid		Cu to Cu Hybrid		Ox to Ox	Cu to Cu Hybrid	
Wafer THK	3μm	4μm	10μm	3μm	2μm	1μm	2μm~1μm	2μm
Structure								
Status	HVM	R&D~MP	HVM	R&D	R&D	R&D	R&D	R&D

Advances in System Integration: Logic

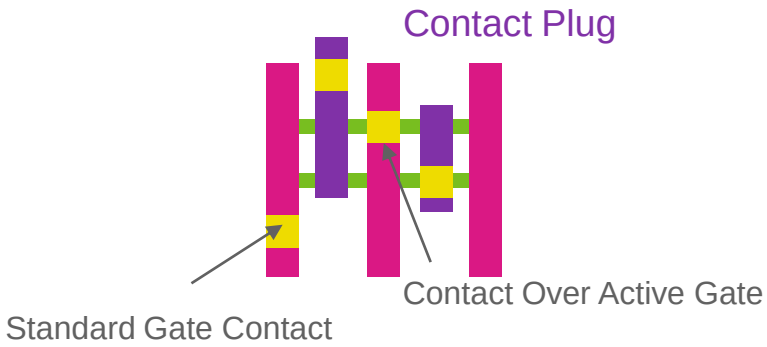
2D shrink



New structure



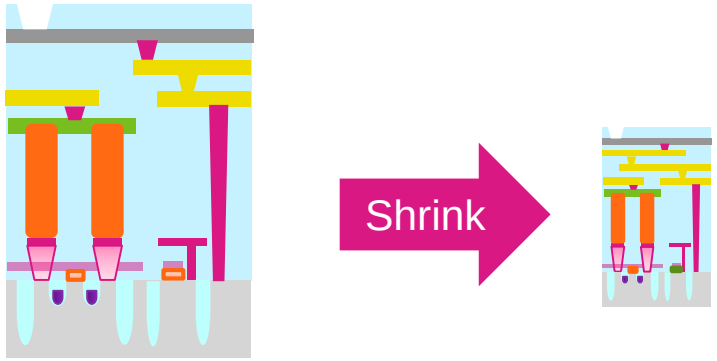
DTCO



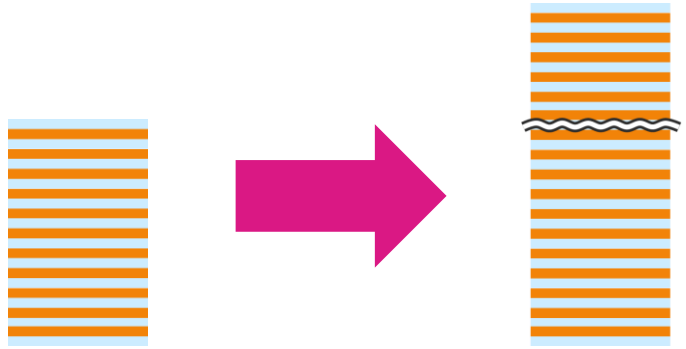
Miniaturization, optimization of design and technology, advances in fabrication, 3D-ification

Advances in System Integration: Memory

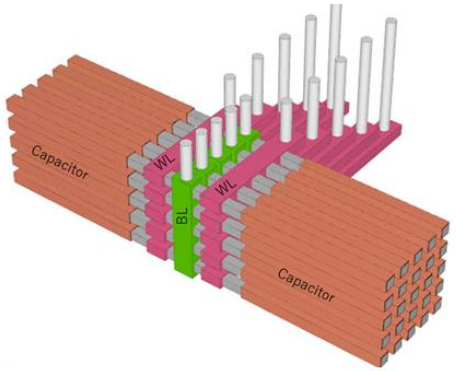
2D shrink



More stack

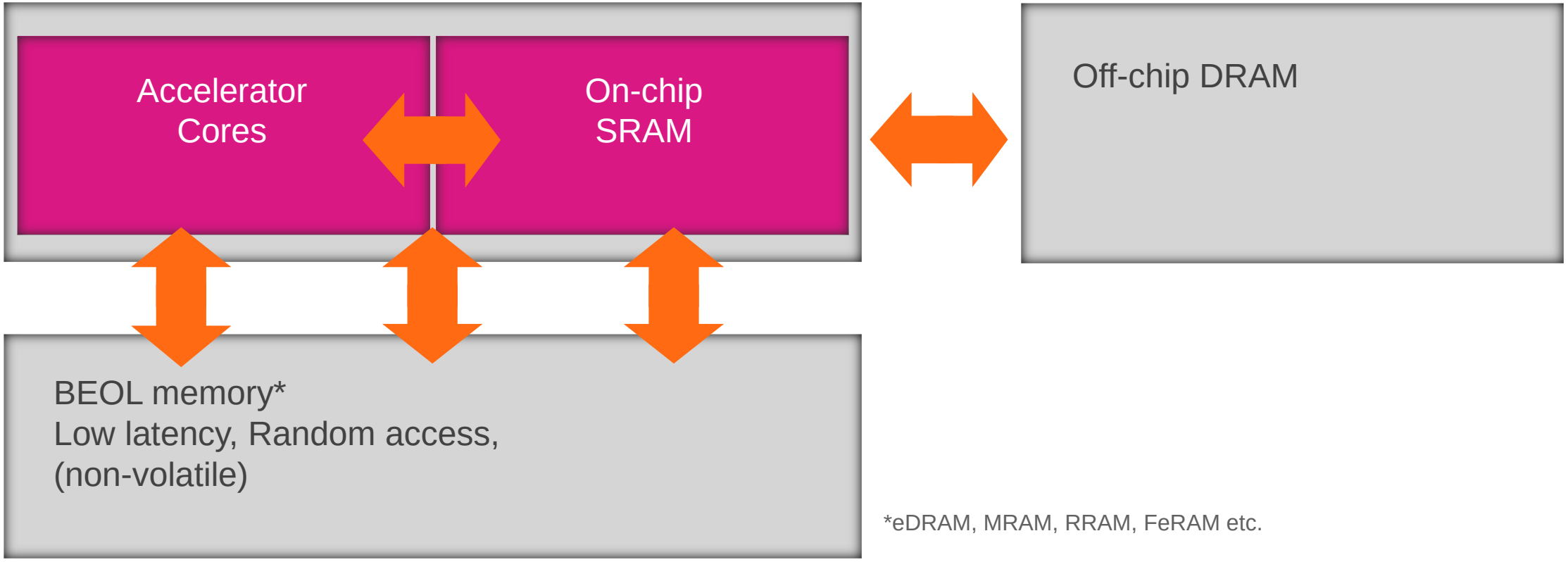


New structure



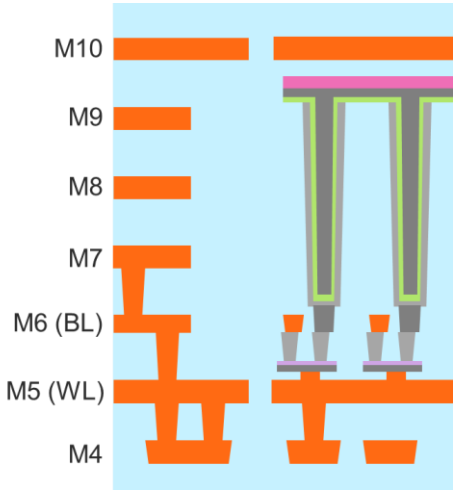
Toward miniaturization, new structure memory, and 3D stacking

Advances in System Integration: BEOL

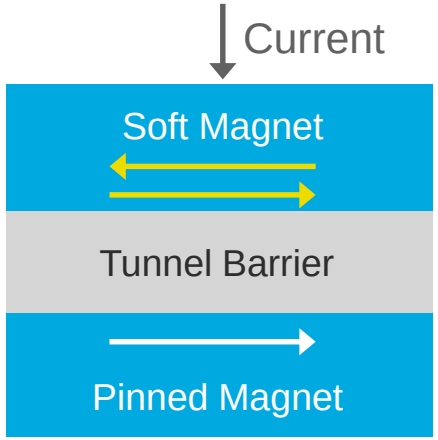


Multi-layered interconnect with built-in memory element

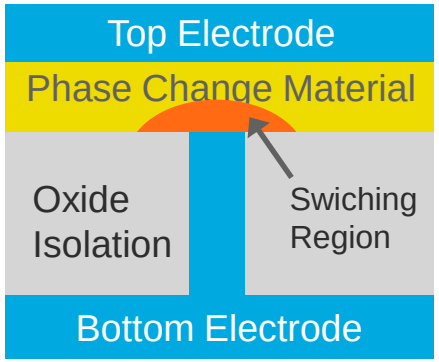
Semiconductor Devices: Direction of BEOL Memory Development



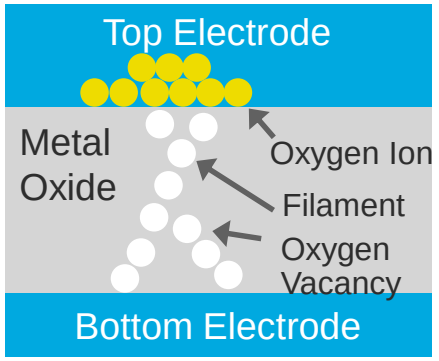
eDRAM



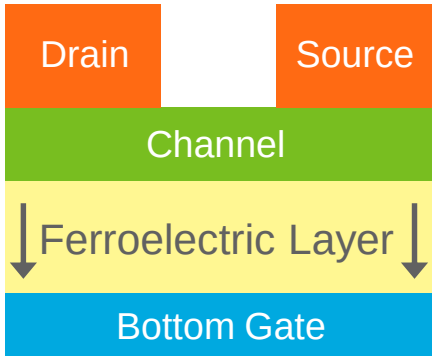
STT-MRAM



PCM



RRAM

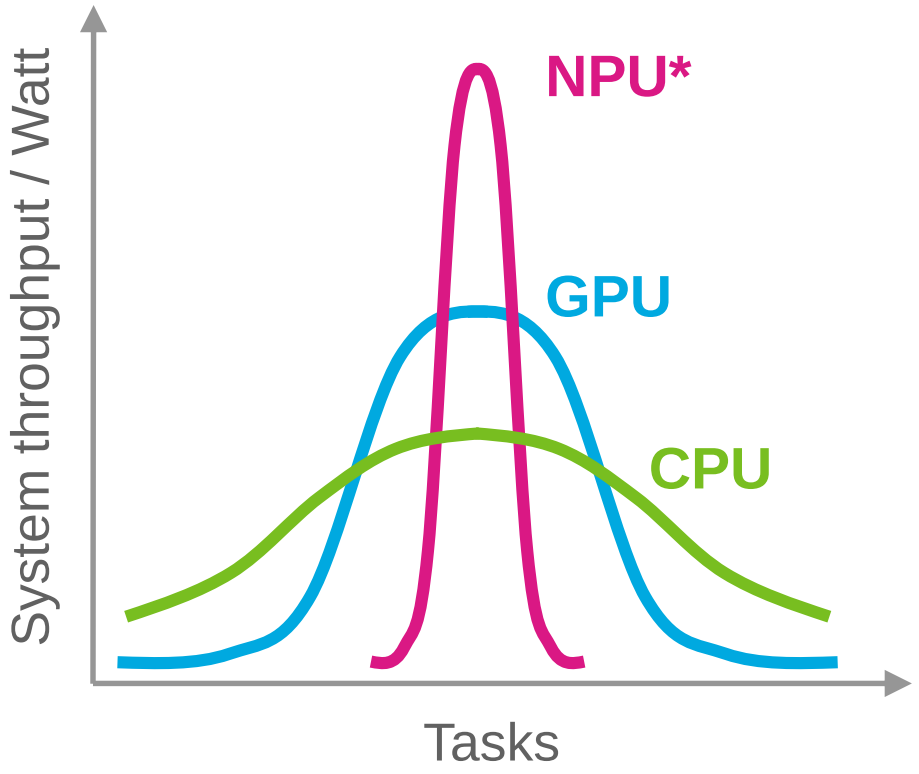


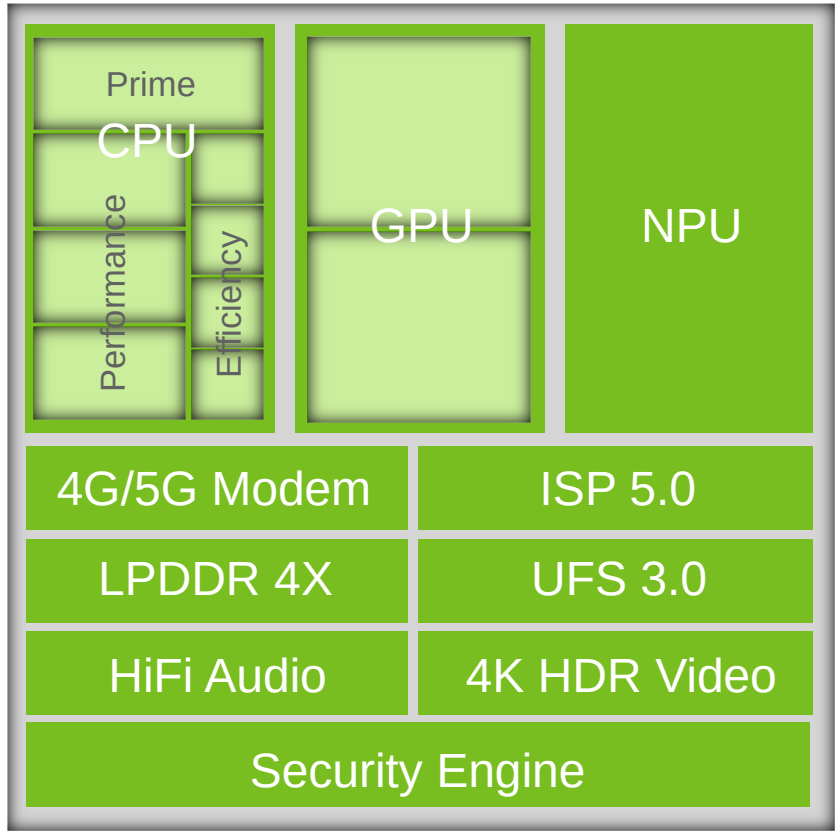
FeRAM

Various forms of memory have been developed and can be used in accordance with their intended purpose

Multi-functional Devices: Neural Processing Unit

*Neural Processing unit



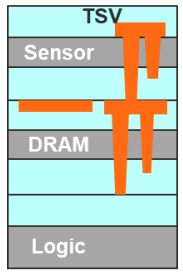
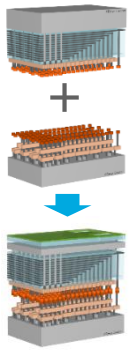
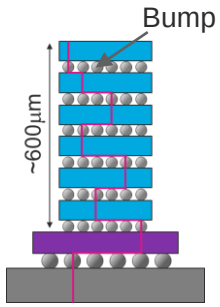
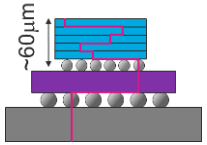
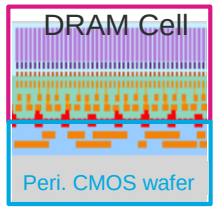
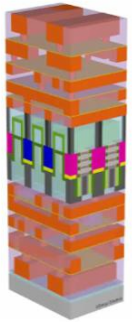
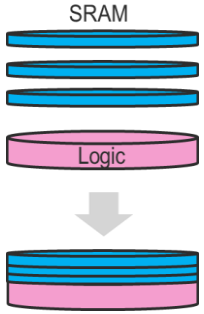
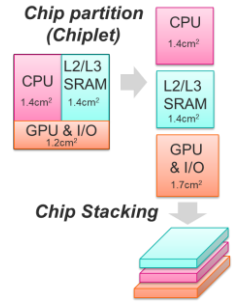


e.g., Leading edge mobile SoC

Performance improvements, miniaturization and reduced energy through the expansion of optimized functional blocks

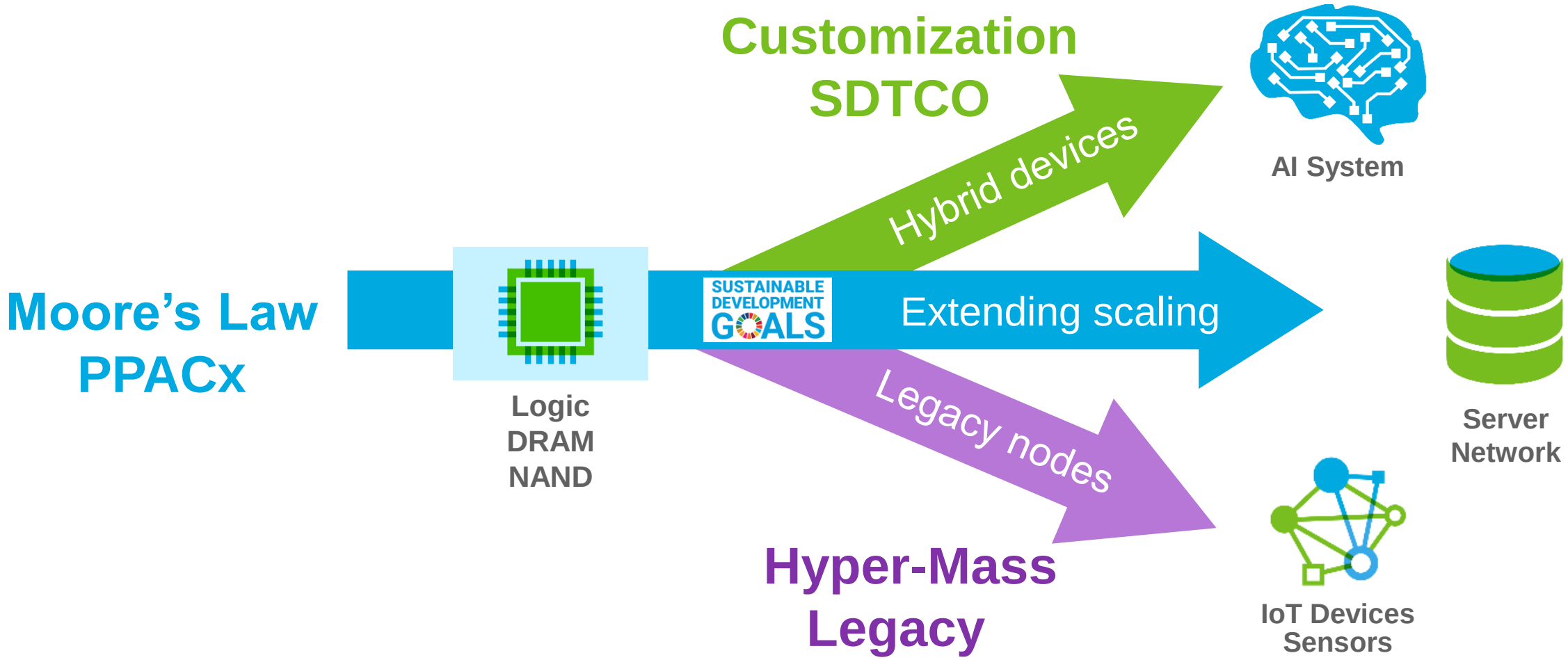
Advances in System Integration: More Options

Source: TEL estimates

Device	CIS	3D NAND	DRAM			Logic		
Stacking	Sensor+ DRAM + Logic	Cell + Peri	HBM (w/ Bump)	HBM (Bump-less)	Cell + Peri	Backside PDN	Logic + SRAM Cell	3D Hybrid Logic + I/O + RF
Bonder Type	W-W	W-W	D-W	W-W		W-W	W-W/D-W	D-W
	Fusion (Permanent)	Fusion (Permanent)	Temporary (Bonding / De-bonding)	Fusion (Permanent)		Fusion (Permanent)		Temporary & Fusion
	Cu to Cu Hybrid	Cu to Cu Hybrid		Cu to Cu Hybrid		Ox to Ox	Cu to Cu Hybrid	
Wafer THK	3μm	4μm	10μm	3μm	2μm	1μm	2μm~1μm	2μm
Structure	 Source: H. Tsugawa, Sony (IEDM2017)		 Source: Sakui, TIT (CICC2019)	 Source: Sakui, TIT (CICC2019)				
Status	HVM	R&D~MP	HVM	R&D	R&D	R&D	R&D	R&D

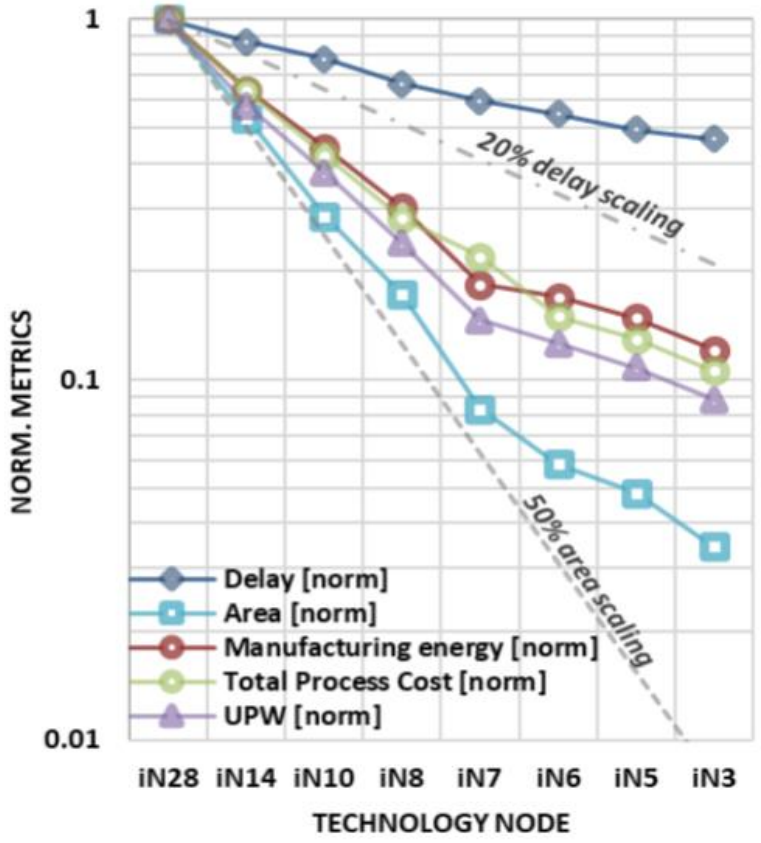
System integration techniques also optimized via PPACx

Roadmap for the Next 10 Years



Development of SDGs-compatible technology for incorporation into diversifying applications

Correlation b/w Environmental KPIs and Technology Node Migration



Graph courtesy of imec

Observations

- Performance is still improving node-over-node but at a reduced rate (delay)
- Area scaling is being achieved but slowing beyond IN7 (~ Foundry 5nm)
- Technology node still drives reduction in manufacturing energy per device
- Cost of manufacturing is still declining
- Water usage is still declining

Conclusion

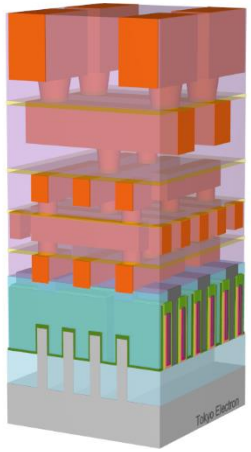
- Advancing technology nodes contributes towards SDGs
- But slowing pace of reduction implies that further innovation is needed
- Working on advanced node devices contributes to SDGs

Advanced technology development is directly linked to the SDGs

Development Trends for Key Devices

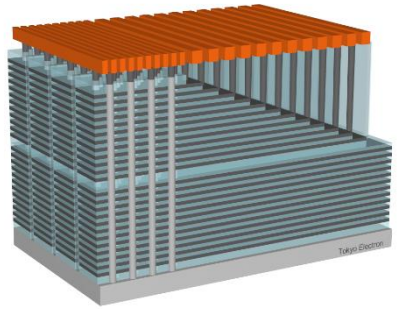
Semiconductor Devices: Direction of Development

Logic



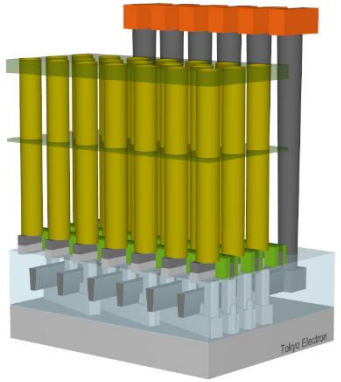
Through miniaturization with structural changes
- Lowered cost per transistor
- Lower power consumption
- Higher speed

NAND



Through high stacking
- Lower cost per bit

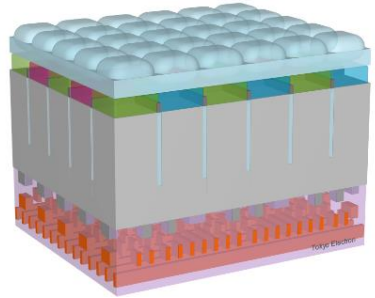
DRAM



Through miniaturization
- Lower cost per bit
- Lower power consumption
- Higher speed

Through new structures
- Lower cost per bit

CIS



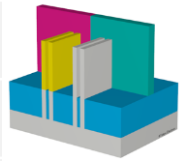
Through miniaturization
- Increased number of pixels
- Higher speed

Through new structures, new materials
- Greater image quality

Logic Trends and Business Opportunities

Advances in Smartphone CPUs

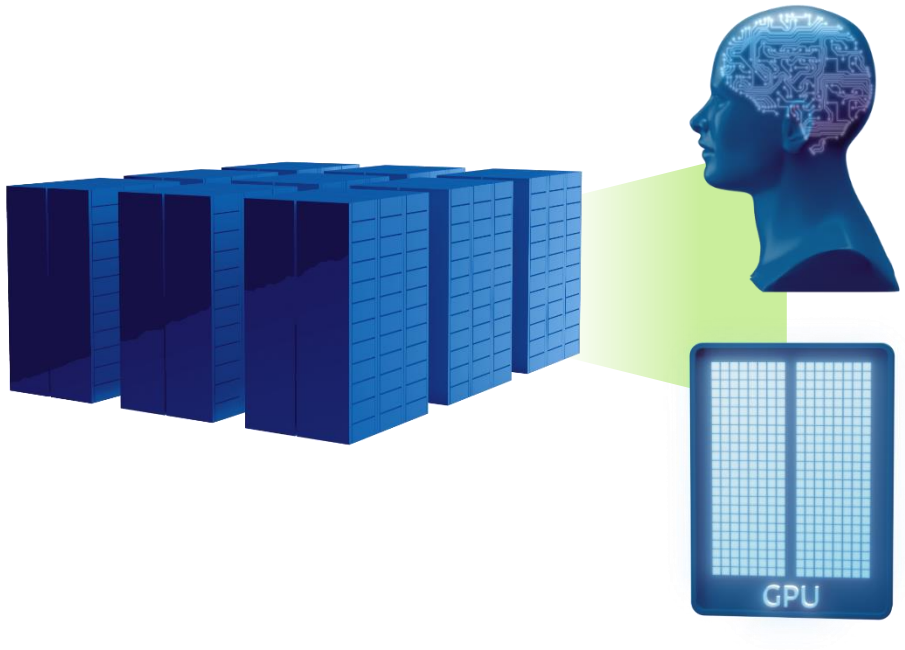
Product Year	2014		2020
Tech. Node	20nm		5nm
Transistor	Last Gen. Planar		4th Gen. FinFET
Adv. Litho	ArFi		EUV
Die Size	89mm^2		88mm^2
Transistor#	2B	×5.9	11.8B
CPU Cores#	2	New architecture Many cores New function	6
GPU Cores#	4		4
NPU Cores#	N/A		16
L2/L3 Cache	5MB	×5.6	28MB



Source: Wikipedia

With advances in transistor fabrication, materials and lithography,
can improve integration by increasing transistor numbers, expanding functions, etc.

Advances in GPU (Operational Accelerator)



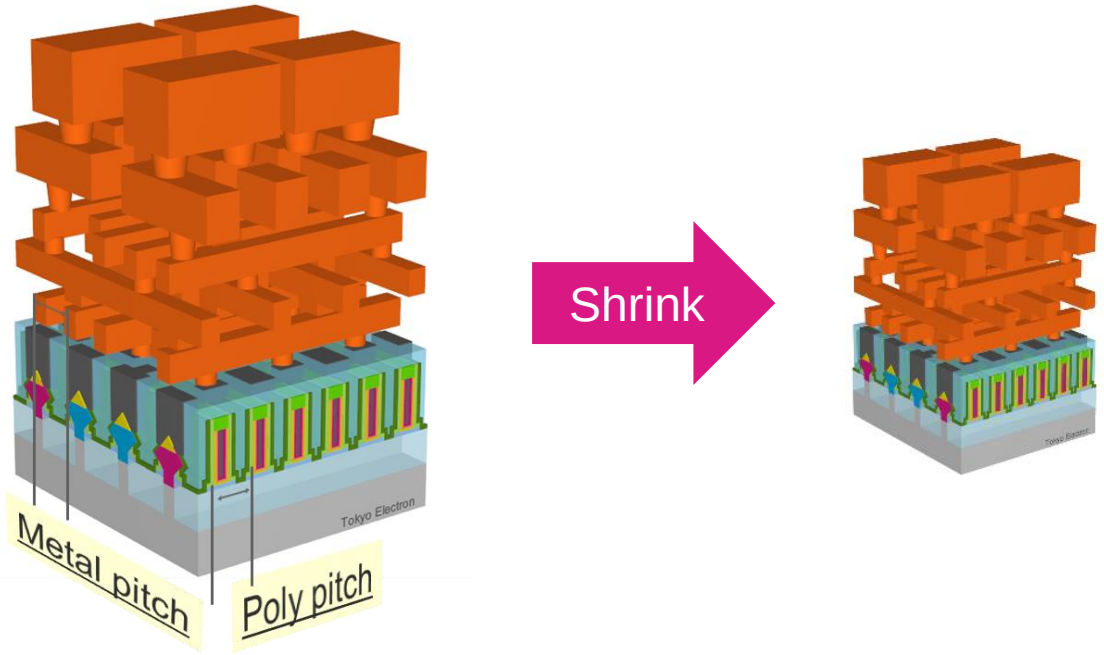
Product Year	2016		2020
Tech. Node	16nm		7nm
Transistor	1st Gen. FinFET+		3rd Gen. FinFET
Adv. Litho	ArFi		ArFi
Die Size	610mm^2		826mm^2
Transistor#	15.3B	×3.5	54.2B
FP32 Cores#	3584		6912
FP64 Cores#	1792	New architecture Many cores New function	3456
INT32 Cores#	N/A		6912
L2/L3 Cache	5.440MB	×11.3	61.696MB

Source: Wikipedia

Number of transistors increasing in HPC too, visible trend toward expansion of functions
Higher integration also sought

Advances in Logic Integration Density

Pitch shrink



Key enablers

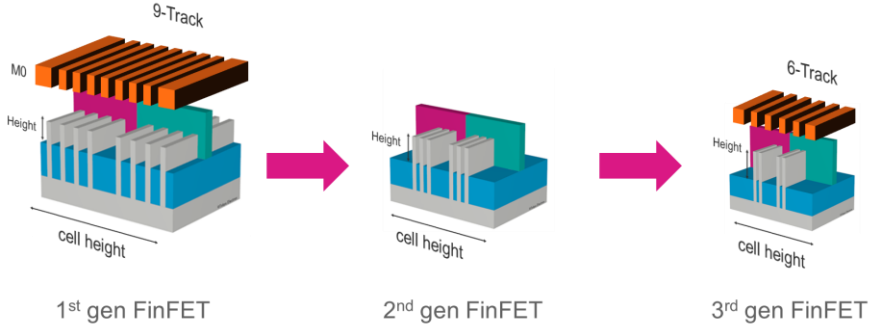
- EUV patterning
- Small area gap filling
- High selective etch
- Pattern collapse free drying

Further advances in lithography, etch, thin film deposition and cleaning technologies needed for miniaturization

Advances in Logic Integration Density

Design Technology Co-optimization: DTCO

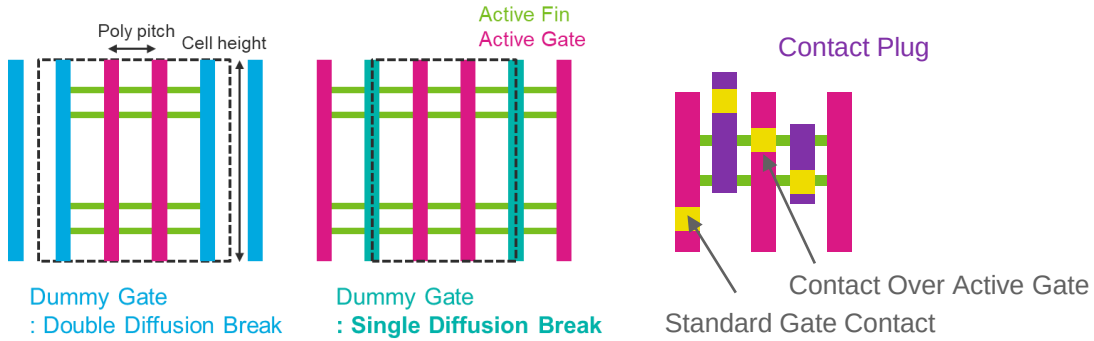
① Cell height scaling: Fin depopulation, Metal track# reduction



Key enablers

- Narrow, straight etch
- Loading free recess etch
- Fin capping to prevent oxidation
- Low resistance silicide, metal

② Cell width scaling: Single Diffusion Break, Contact Over Active Gate etc.



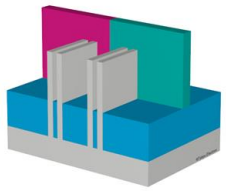
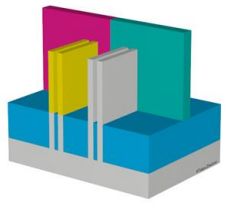
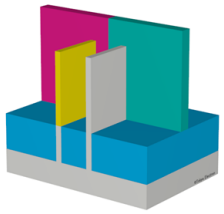
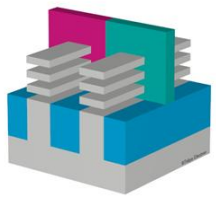
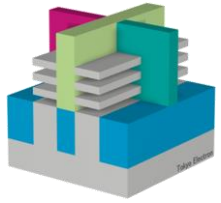
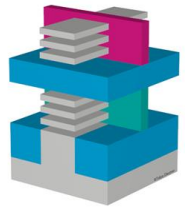
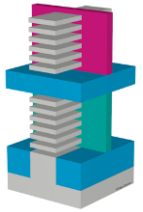
Key enablers

- Small hole, trench etch
- Low stress gap filling
- Multi-color films for etch
- High selective etch

Further advances in process technology for DTCO sought

Logic Technology Roadmap

*Assume new knob will be created in each node
**Single Diffusion Break, ***Self Align Gate Contact

Year of HVM (20k/month)	2018	2020	2022	2024	2026	2028	2030
Node	N7	N5	N3	N2	N1.4	N1	N0.7
Device	3~2 Fin 	2 Fin 	2~1 Fin 	GAA NS 	Forksheet 	CFET 	2nd Gen. CFET 
Poly pitch (PP)	56	48	45	42	39	36	33
Min. MP [nm]	40	28	22	20	18	16	12
Cell height (CH)	240 (2Fin)	210 (2Fin)	176 (2Fin)	120 (NS)	90 (NS)	64 (CFET)	48 (CFET)
Density (a.u.) PP x CH x DTCO*	1	1.73 (vs. N7)	1.53 (vs. N5)	1.81 (vs. N3)	1.65 (vs. N2)	1.75 (vs. N1.4)	1.67 (vs. N1.0)
Scaling booster	EUV SDB**	High μ channel	SAGC*** Dipole eWF	Backside PDN		Heterogeneous channel	2D material

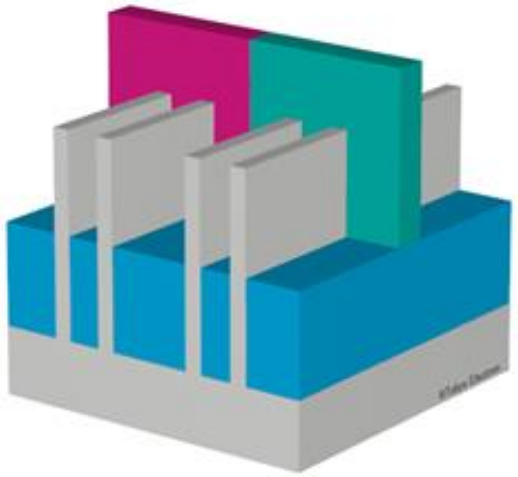
Source: iedm 2020[1], IRDS2020 with TEL's update [1] imec, S. B. Samavedam et al.

Aiming for 1.6-1.8x increase in logic density along with pitch scaling, DTC and scaling booster

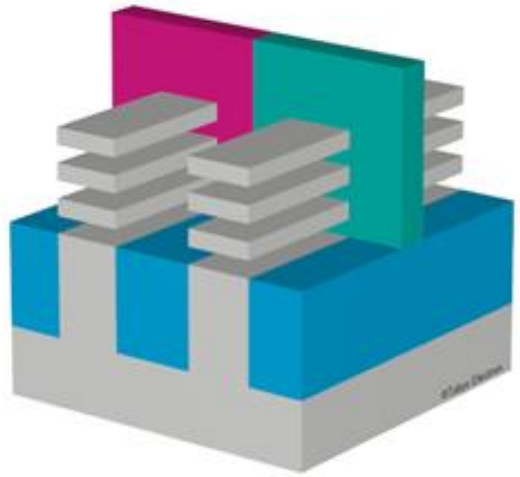
GAA Nanosheet Device (Gate All Around Nanosheet)

$$L_{g,min} \geq \beta(T_{ch} T_{ox} \varepsilon_{ch} / \varepsilon_{ox})^{1/2}$$

$L_{g,min}$: Minimum gate length with good device electrostatics
β : Constant > 2.5
T_{ch} : Channel thickness
T_{ox} : Gate oxide thickness
ε_{ch} : Dielectric constant of channel
ε_{ox} : Dielectric constant of gate oxide



Lay down



FinFET

Patterning defined Fin width: 3σ 1.1nm*

Nanosheet

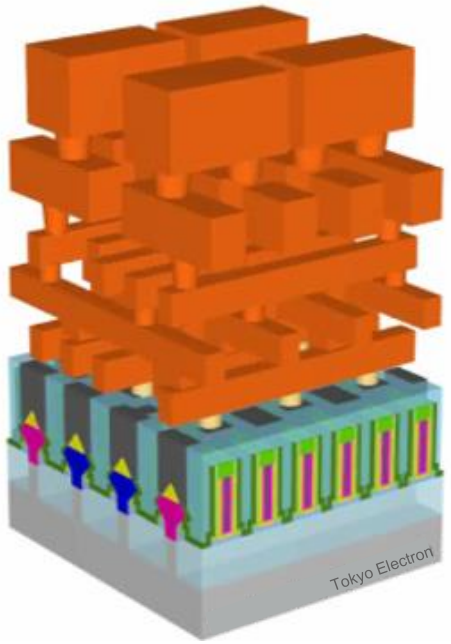
Si EPI thickness defined sheet thickness: 3σ 0.4nm*

*Source: SC Song (Qualcomm) et al. VLSI 2019

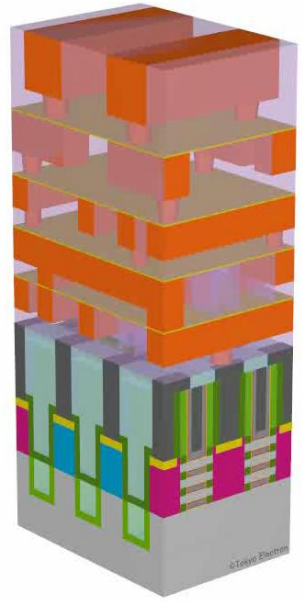
Improved controllability of channel width by nanosheet structure, increased channel width through stacking → Low leak, high on current

GAA Device Process Flow

FinFET



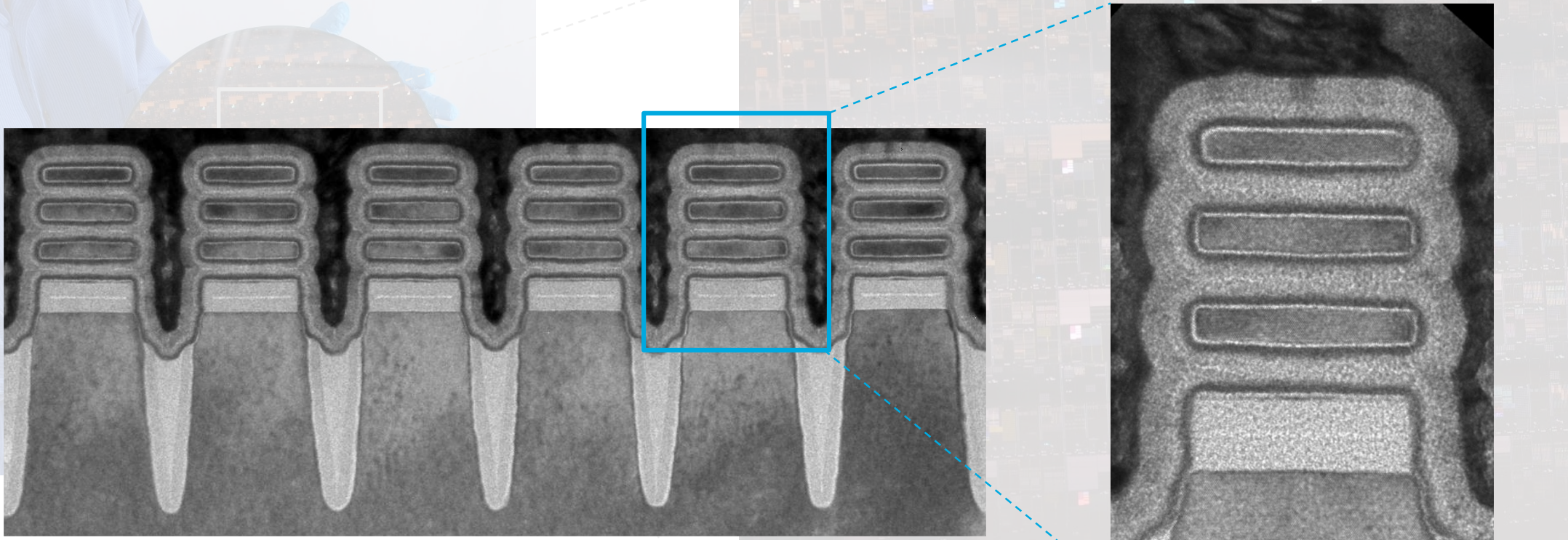
GAA FET



Source: TEL

TEL's wafer fab equipment is essential for creating complex GAA structures

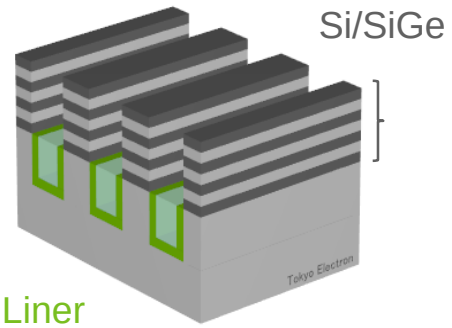
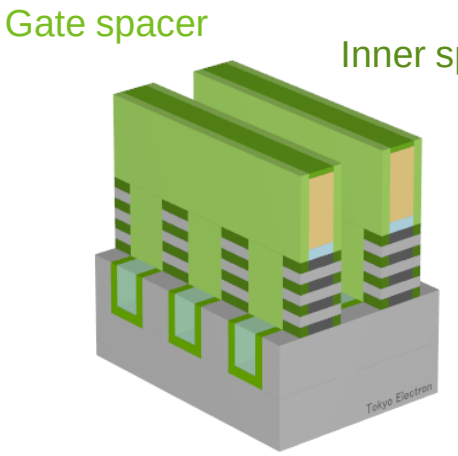
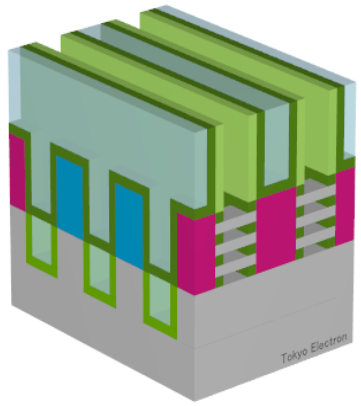
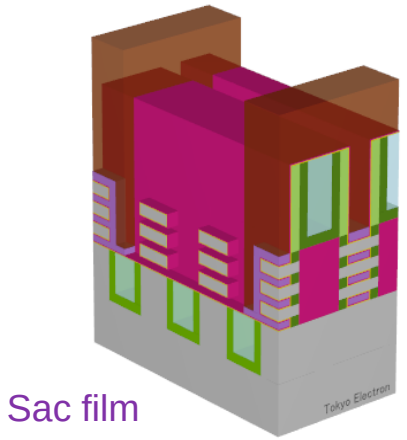
2 nm GAA Technology



Cross section TEM of 2nm GAA device courtesy of IBM Research

TEL's wafer fab equipment is essential for creating complex GAA structures

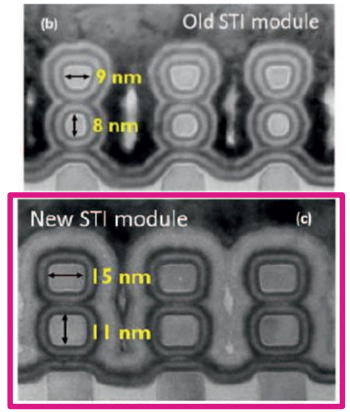
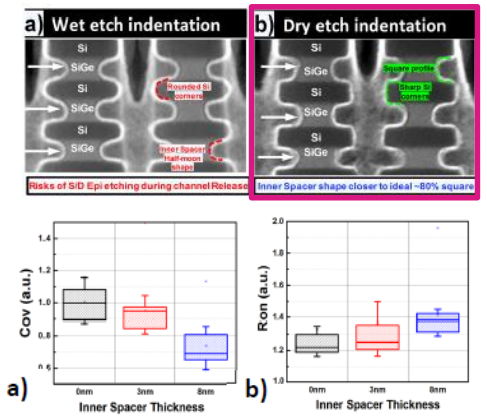
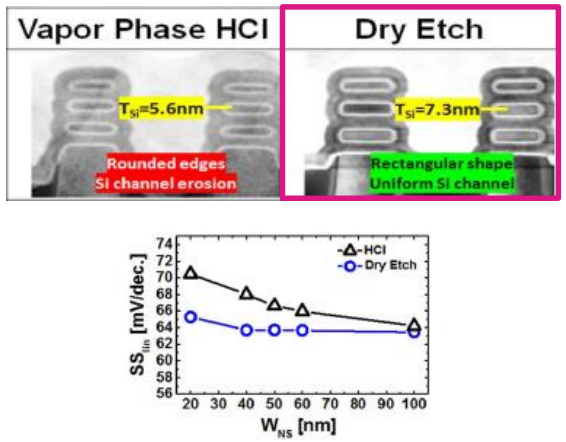
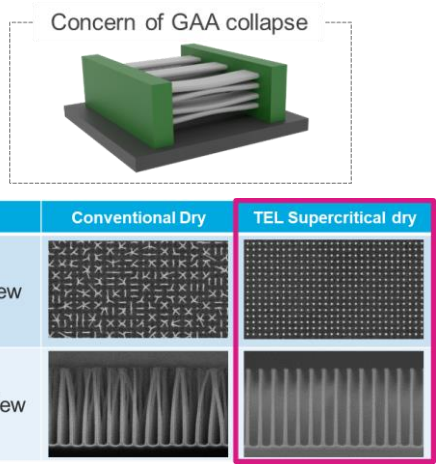
GAA Related Process Modules

Mold stack & Etch	Inner spacer	Nanosheet release	Replacement gate
			
• SiGe/Si: Defect free, Uniform EPI • Trench etch: Vertical profile • STI Liner: Prevent oxidation • STI OX: Low temp. • STI recess: Loading less	• Fin recess: Vertical profile • Indent etch: Loading less • Inner spacer dep: Low-k (k<5) • Inner spacer etch: High selective	• Full channel etch: High selective	• Reliability Si etch: High selective • Advanced drying: Collapse free • Sac film: Conformal • WFM/Dipole film: Conformal • WFM/Dipole etch: High selective

Source: TEL

Offering new solutions for critical modules in nanosheet devices

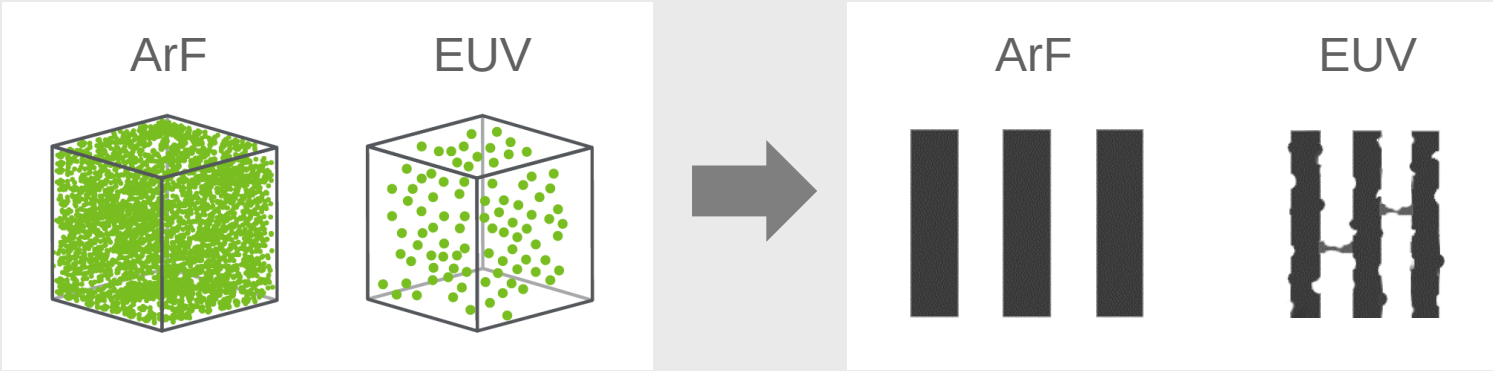
GAA Related Process Modules

Mold stack & Etch	Inner spacer	Nanosheet release	Replacement gate
			
R. Ritzenthaler (imec) et al., iedm 2018	N. Loubet (IBM) et al., iedm 2019	N. Loubet (IBM) et al., iedm 2019	Source: TEL
• SiGe/Si: Defect free, Uniform EPI • Trench etch: Vertical profile • STI Liner: Prevent oxidation • STI OX: Low temp. • STI recess: Loading less	• Fin recess: Vertical profile • Indent etch: Loading less • Inner spacer dep: Low-k (k<5) • Inner spacer etch: High selective	• Full channel etch: High selective	• Reliability Si etch: High selective • Advanced drying: Collapse free • Sac film: Conformal • WFM/Dipole film: Conformal • WFM/Dipole etch: High selective

Key points are preventing oxidation of Si/SiGe trench, high selectivity and precisely controllable SiGe etch, and preventing pattern collapse

Miniaturization: EUV Lithography Technology Challenges

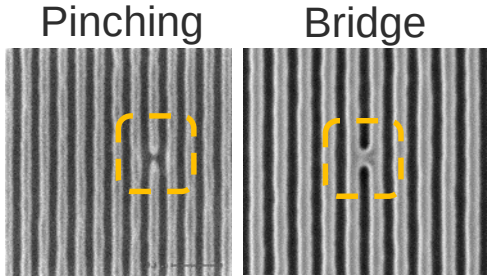
Stochastic noise



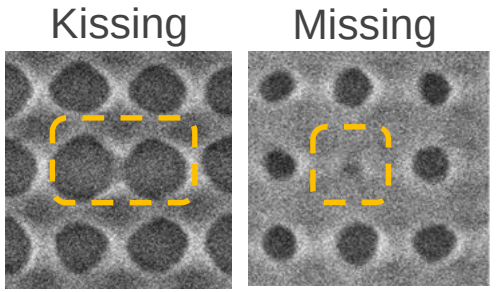
- The number of EUV photons is only **1/14** compared to ArF at the same dose.
- Photon absorption of EUV resist is lower than that of ArF resist.
- These cause large edge roughness, resulting in one of the sources of pattern defects.

Performance

Line : LER, Pinching, Bridge



Hole : L-CDU, Kissing, Missing

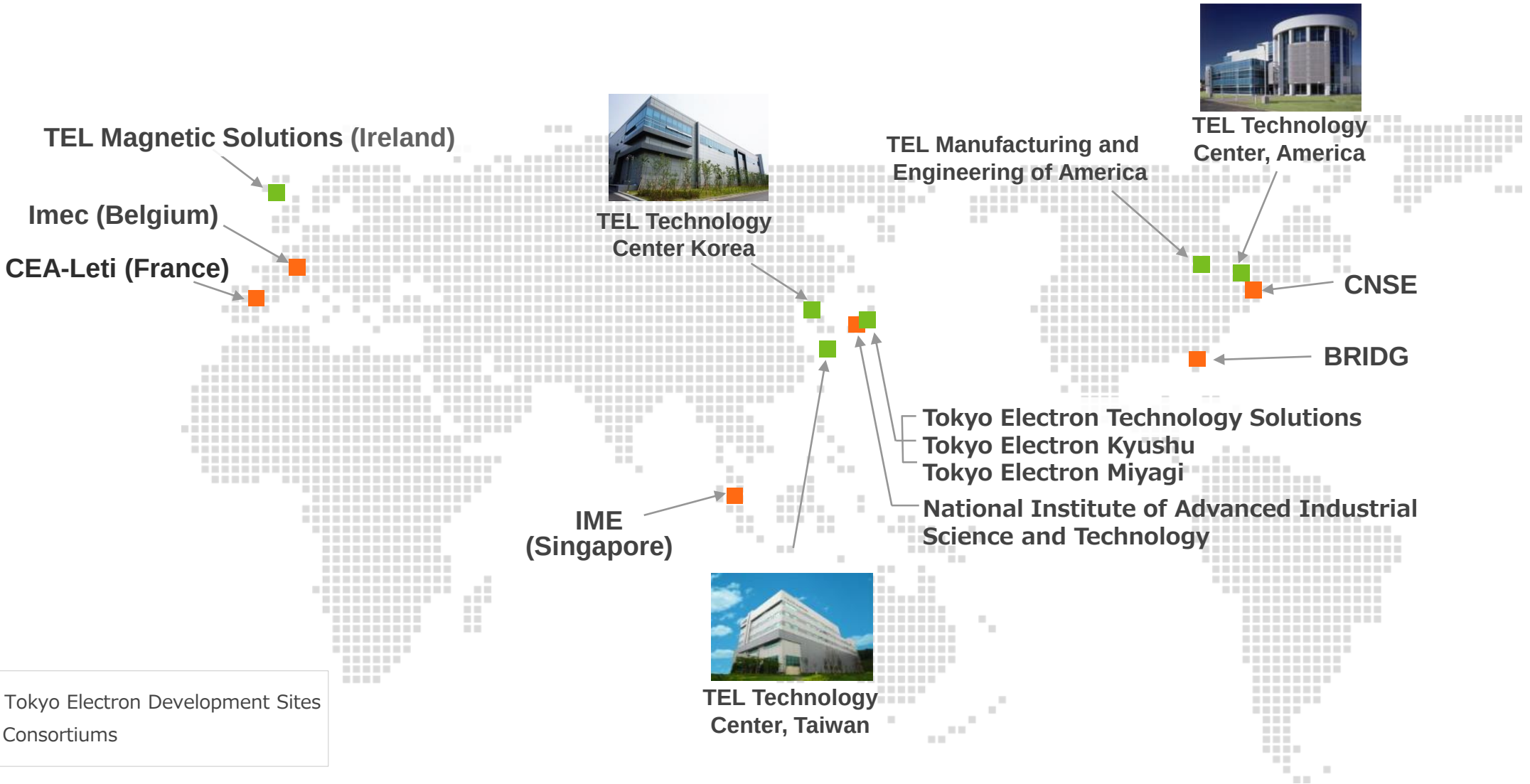


Source: S. Morikita, et al., Tokyo Electron Miyagi (DPS2018)

Resist stack and etching co-optimization necessary
for realizing high productivity, precise control and low defects

Global Development Facilities

(As of June 1, 2021)

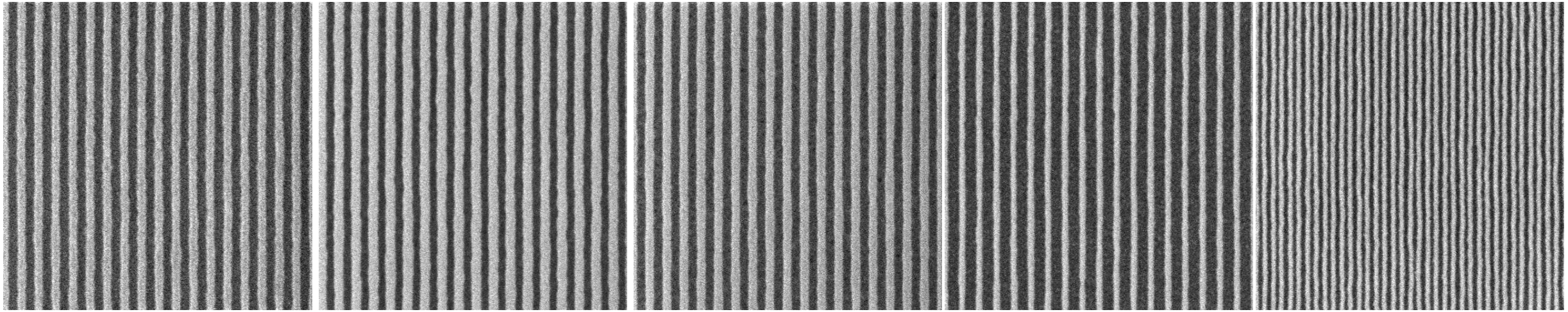


15 nm Pitch L/S Fabrication Using EUV SADP

Litho Pitch: 30nm
CDSEM CG6300
512*512/250k

Demonstrated on TEL tools

Lithography	Trilayer + Plasma Treatment	Tone Inversion	Mandrel	SEMP



CD: 14.7nm	CD: 16.1nm	CD: 15.6nm	CD: 10.6nm	CD: 7.7nm
LER: 2.25nm	**LER: 2.0nm**	**LER: 1.89nm**	**LER: 1.71nm**	**LER: 1.57nm**

-11%

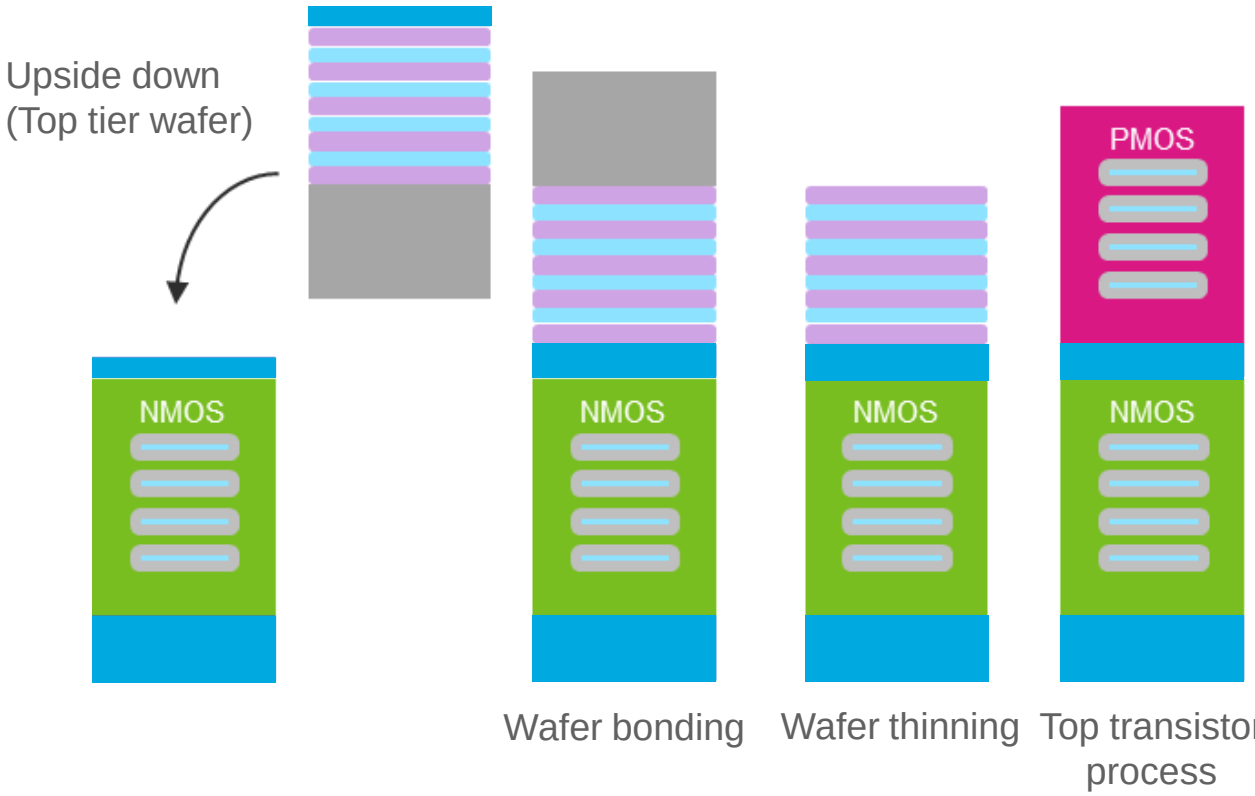
-24%

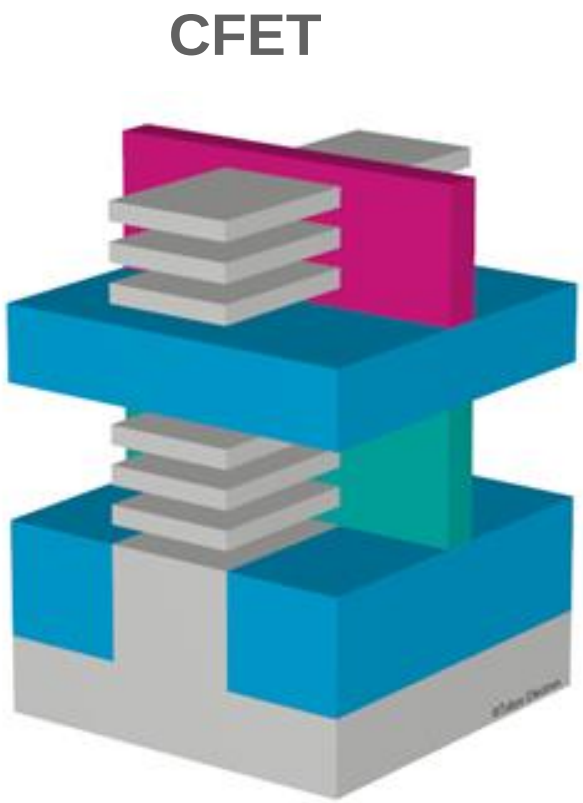
-30%

Source: Eric Liu et al., TEL Technology Center, America SPIE 2021 Advance Lithography

Achieve industry-leading 15 nm pitch line and space pattern

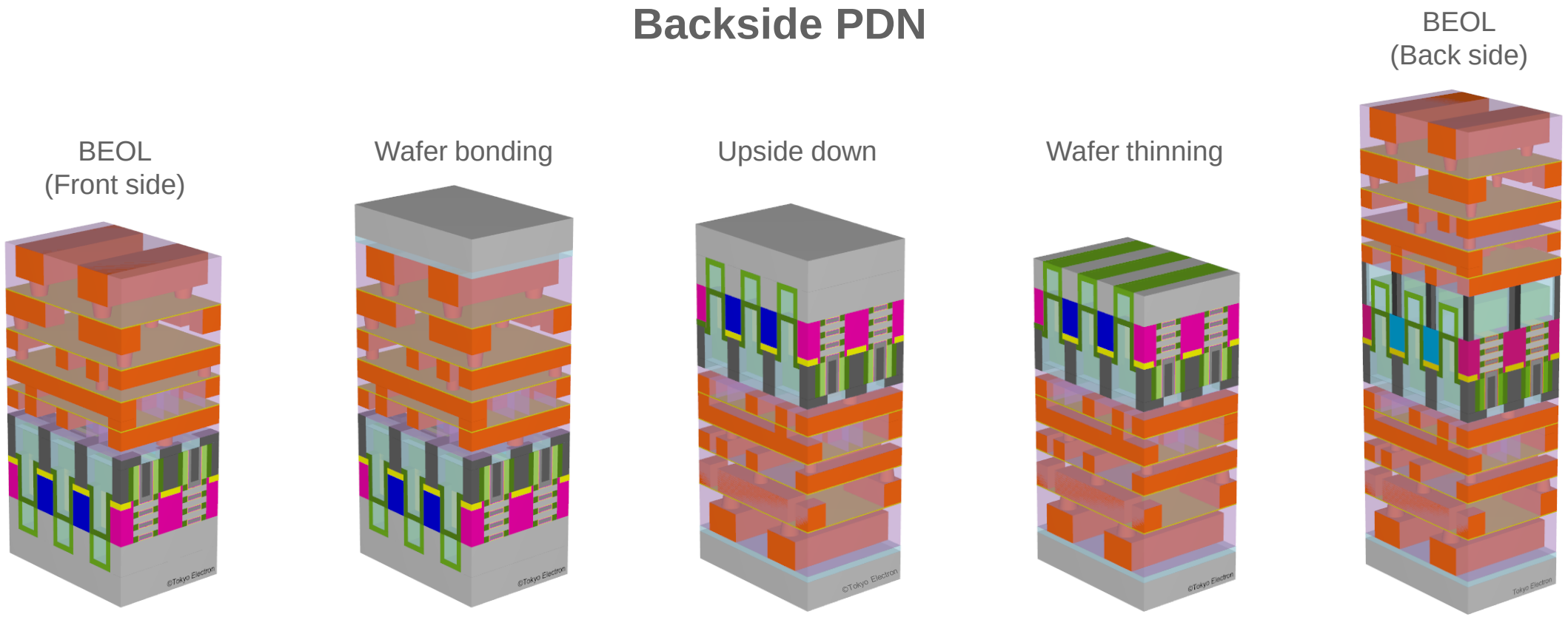
Back End: Wafer Bonding and Thinning Technology for CFET





Low distortion wafer-to-wafer bonding technology and substrate film thinning technology are necessary for scaling booster technology

Back End: Wafer Bonding and Thinning Technology for BSPDN



Low distortion wafer-to-wafer bonding technology and substrate film thinning technology are necessary for scaling booster technology

Back End Advances: Bonding

Wafer Level Fusion Bonder Synapse™ Si

Key Features

- Designed for high volume manufacturing
- High availability for production
- Excellent alignment accuracy
- Realized high volume manufacturing with Cu Hybrid Bonding technology

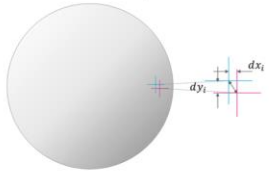
Applications

- Fusion Bonding for C-MOS Image Sensor
- Any application requires Cu Hybrid Bonding

Alignment Accuracy (Total Overlay)

Two wafers are bonded together

After bonding, alignment accuracy is measured by IR camera at each point



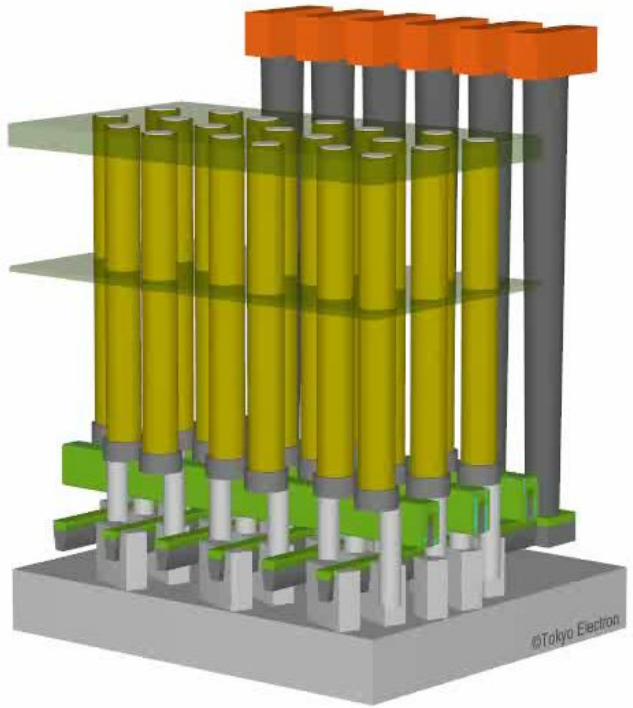
Experimental Data (TEL TEG Wafer)

	1	2	3	4	5	6	7	8	9	10	11	12
[Dx] Max(nm)	59	59	58	70	67	66	74	74	70	62	63	63
[Dy] Max(nm)	56	57	50	56	69	62	70	71	67	44	47	49
DxDy Map												
Residental Map												

3D integration drives device hybridization

DRAM Trends and Business Opportunities

DRAM Structure and Process Flows



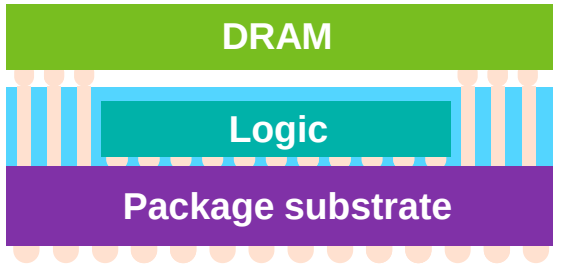
Source: TEL

High aspect ratio structure is fabricated with sophisticated patterning technology

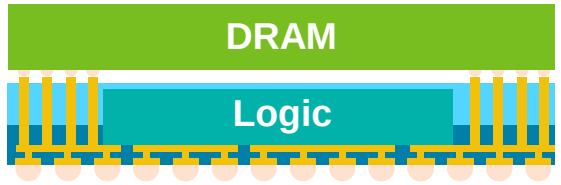
Advances in DRAM for Smartphones

Product Year	2014	2020
Tech. Node	25nm	1ynm
DDR	LPDDR3	LPDDR4X
Data Rate	1.333Gbpps	4.266Gbpps
Capacity	1GB ×4 or 6	4GB or 6GB
	(4Gb ×2)	(8Gb or 12Gb×4)

Source: Wikipedia



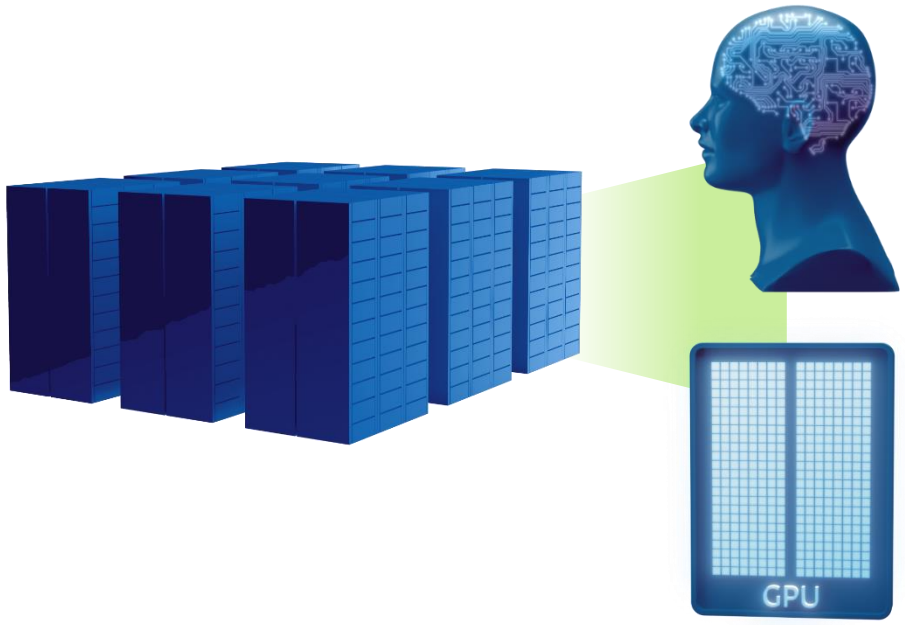
Flip Chip Package on Package



Integrated Fan-Out

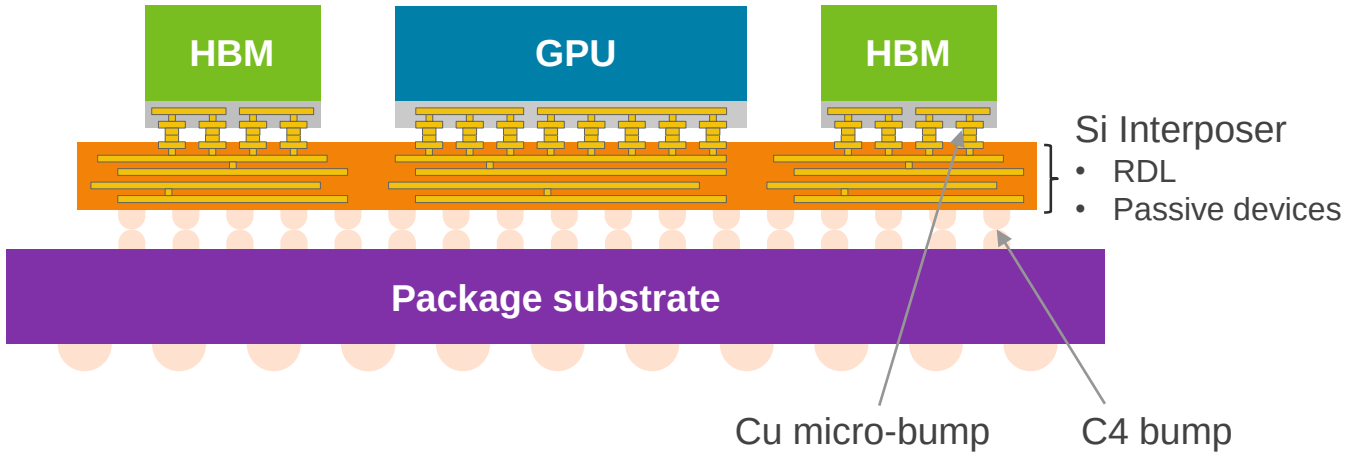
With the increase in data handling volumes, packaging has advanced with expanded capacity, accelerated processing and further integration

GPU (Operational Accelerator) and HBM DRAM



Product Year	2016		2020
Capacity	16GB HBM2	×5	80GB HBM2e
	(HBM2×4)		(HBM2e×6)

Source: Wikipedia

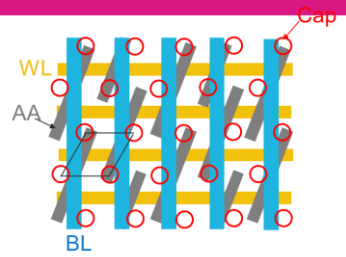


Data volumes are also increasing in HPC, driving packaging advances with increased integration, higher capacity and faster processing

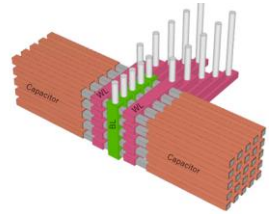
DRAM Technology Roadmap

Source: TEL estimates

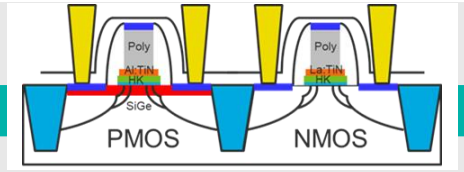
Year of HVM (20k/month)	2020	2021	2022	2023	2024	2025	2026	2027~28	2029~30
F* [nm]	16	15~14		13~12		12~11		≦10	<10
Cell / Peri. layout	$6F^2$							3D	
Patterning	193i SAQP, DP (+ EUV)								
Pillar cap. A.R.	>40		>45		>50		>55	>60	
Capacitor	ZAZ CIP							Alternative: STO etc.	
Peri. CMOS	Poly SiON			High-k Metal Gate				FinFET	



*Feature size: STI hp along WL = STI hp / COS(21°)

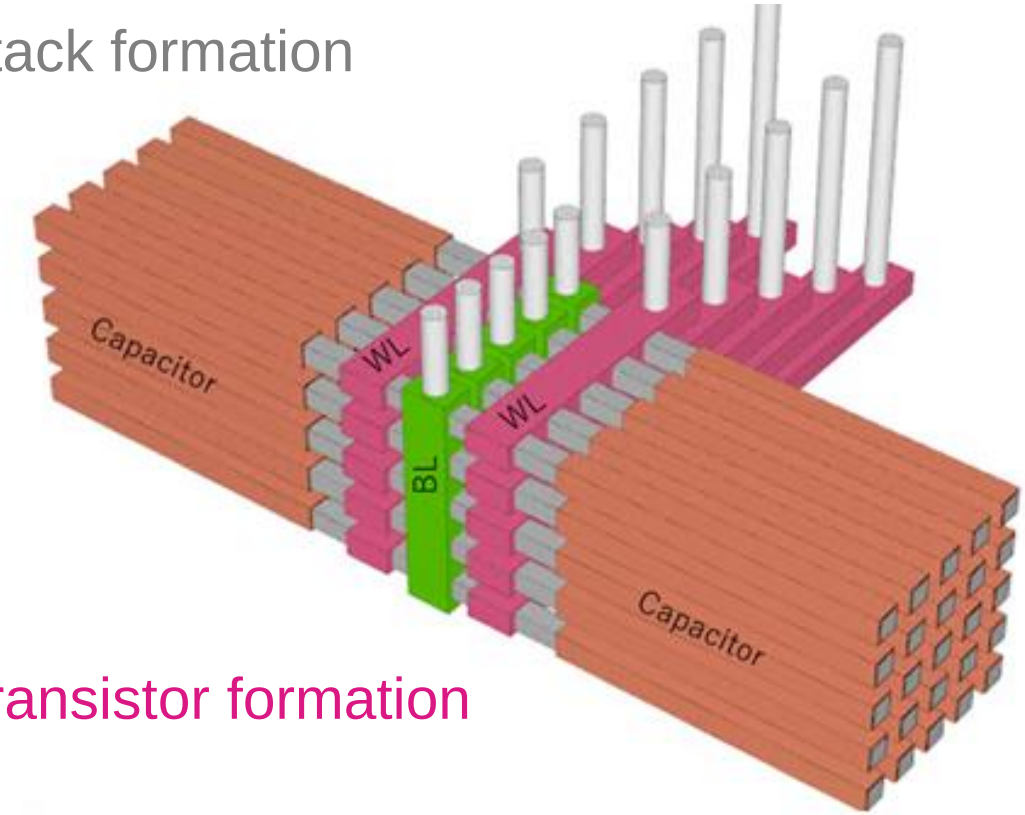


M. Popovici (imec) et al. IEDM 2018
Schematic by TEL

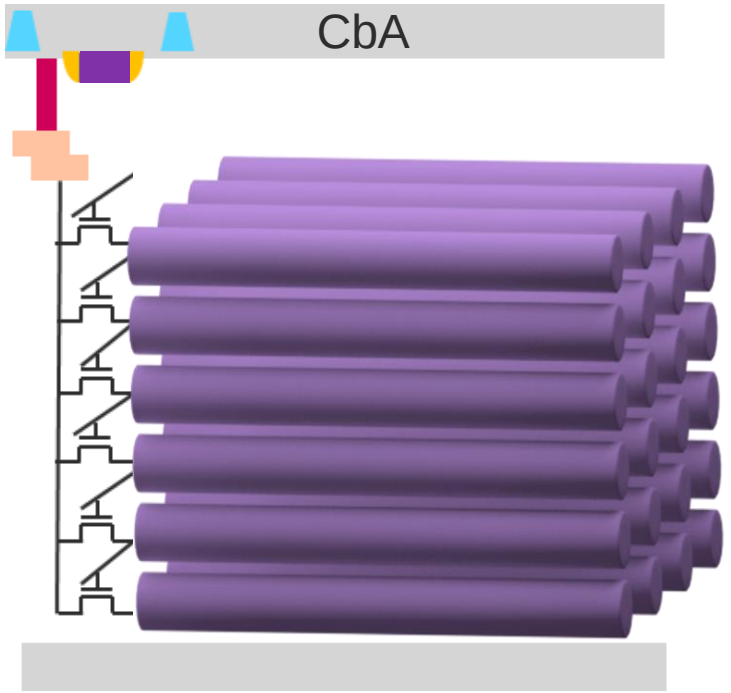


Key Modules in 3D DRAM

Stack formation



CMOS wafer bonding to enable CbA



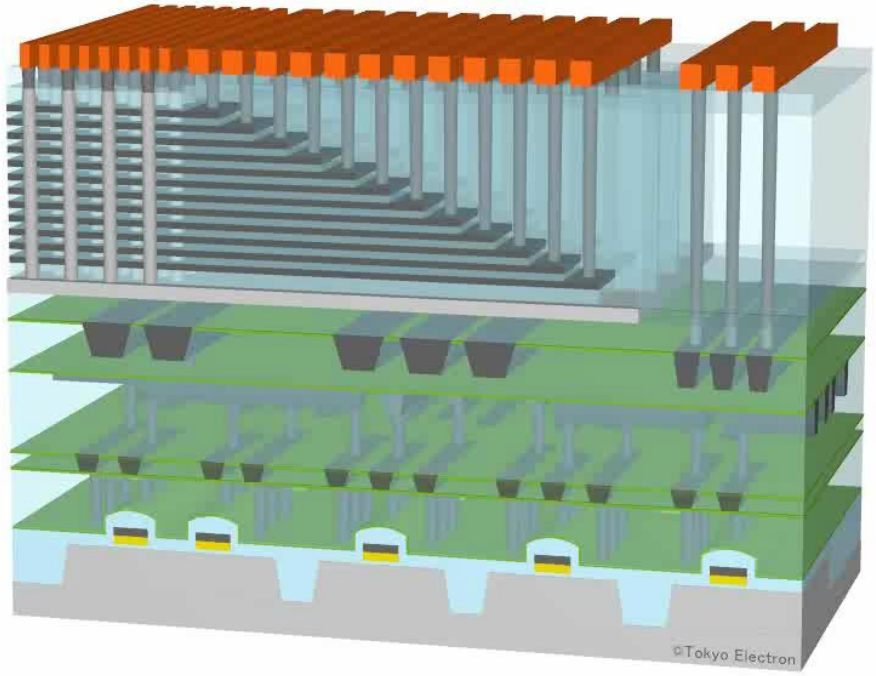
Cell Transistor formation

Capacitor formation

Currently evaluating multiple options

NAND Trends and Business Opportunities

Advances in 3D NAND Bit Density



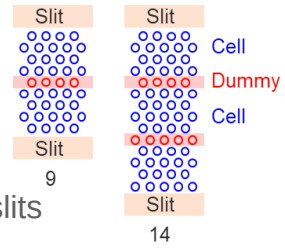
Source: TEL

Reduced device footprint achieved by allocating logic under memory

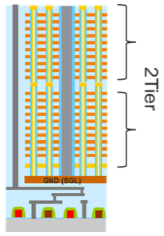
NAND Technology Roadmap

Source: TEL estimates

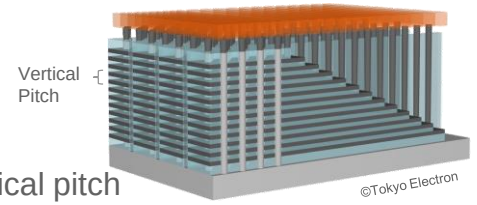
Year of HVM (20k/month)	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Stack (~1.6x/3years)	128L	16x~19xL (176)		22x~25xL (240)	28x~32xL (304)		35x~4xxL (368)	41x~45xL (440)		5xxL (512)	
Tier	1 or 2	2		2	2		2 or 3	3		3 or 4	
Vertical pitch	50~55nm	45~55nm		40~50nm	35~45nm		35~45nm	35~45nm		35~40nm	
Memory height	7~8μm	8.5~10.5μm		10~12.5μm	11~14μm		13.5~17μm	16~20.5μm		18.5~21μm	
Channel		Poly Si grain CIP			incl. MILC Si						
WL metal	W	W		W	Mo		Mo	Mo		Mo	
#of memory holes b/w slits	9	9		9~24	14~24		19 or 24	19 or 24		19 or 24	
Peri. CMOS (In general)	Under array or Next array	Under array		Under array or Bonding	Under array or Bonding		Under array or Bonding	Under array or Bonding		Under array or Bonding	



#of memory holes b/w slits

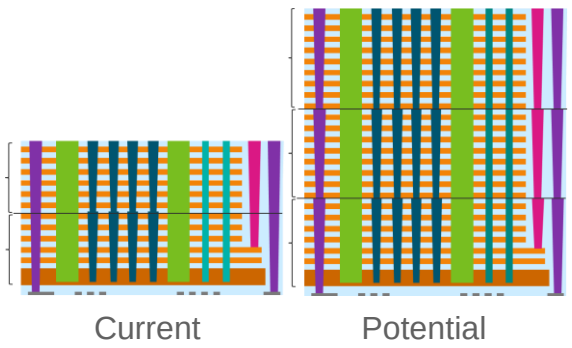
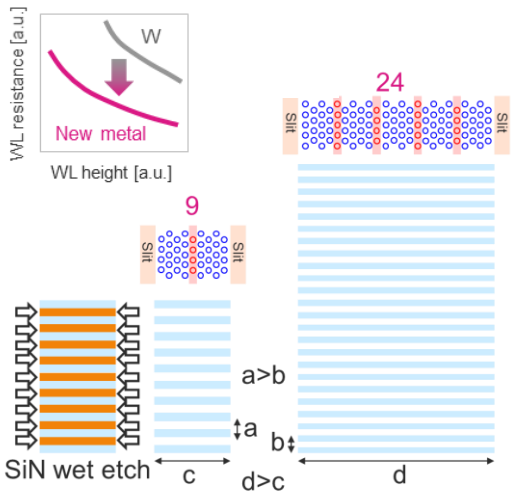
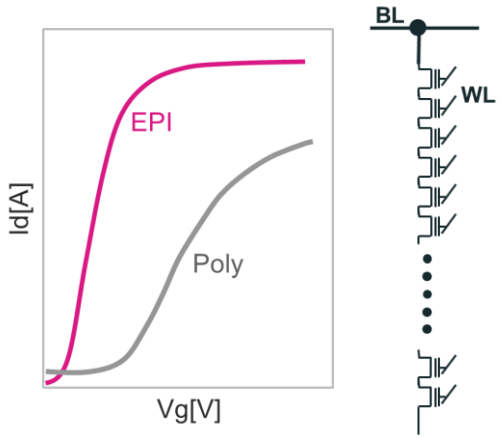
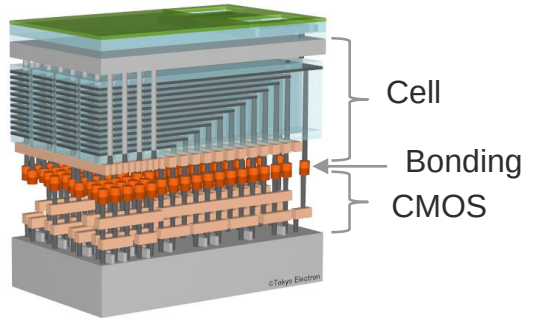


Tier



Vertical pitch

3D NAND Technology Challenges and Solutions

HARC	Replacement gate: WL	Channel Si	Peri. CMCO bonding
			
・HARC etch: Pluralization of each process (multi-level contact/slit/channel, etc.)	・SiN wet etch: High selective ・Advanced drying: Collapse free ・Mo CVD: Low R WL metal	・CVD Si CIP: Large grain size → EPI like	・Cu hybrid bonding

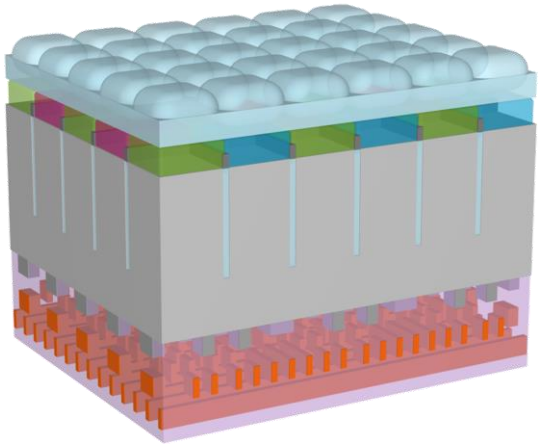
Source: TEL

Processing technology advances essential for enabling further high value-add in NAND devices

CIS Trends and Business Opportunities

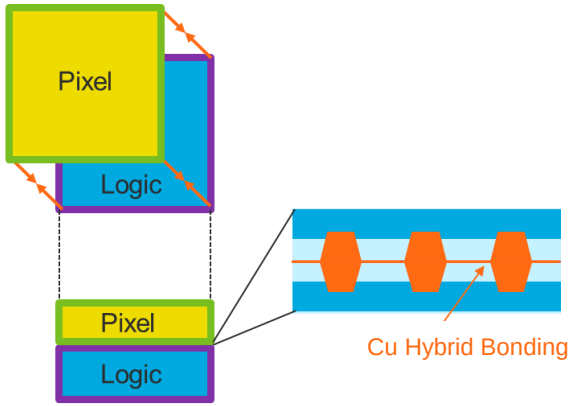
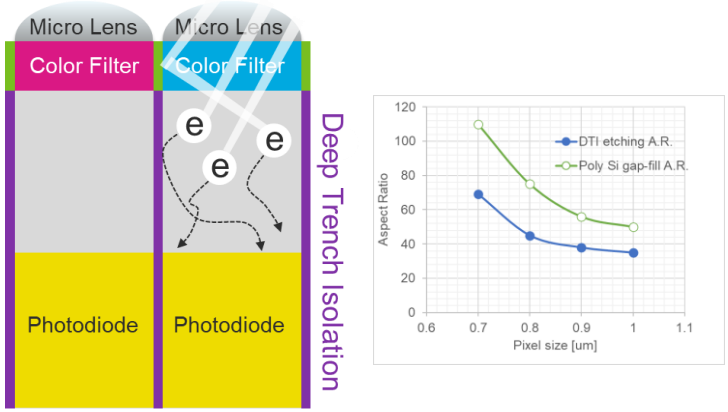
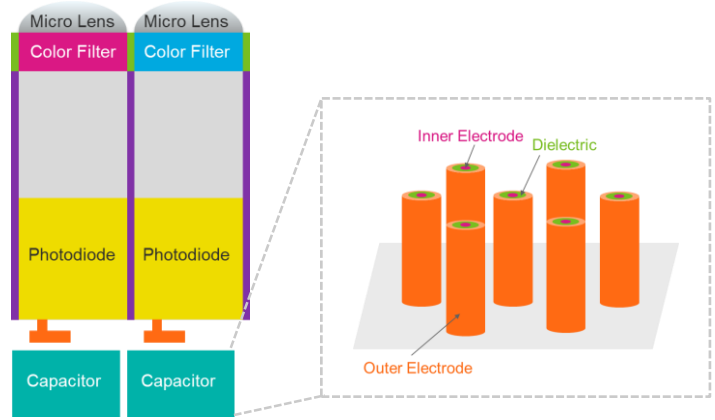
CIS Has Expanded Sensor Functions With Onboard AI

Image sensor × **AI** = **Applications**



Hybridization of devices is progressing and creating further added-value

CIS Technology Challenges and Solutions

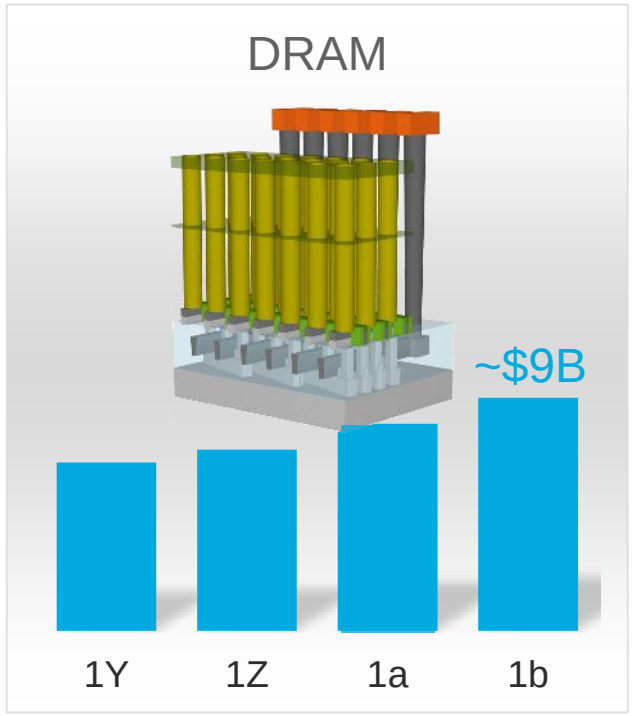
Wafer bonding: 3D stacked BSI	Deep Trench Isolation: Pixel scaling	Capacitor: Global Shutter
 Back-illuminated CMOS image sensor	 H. Kim (Samsung) et al. ISSCC 2020 Data edit by TEL	 Jae-kyu Lee (Samsung) et al. ISSCC 2020 Schematic by TEL
・Wafer level Cu to Cu hybrid bonding	・Si deep trench etch: High A.R. etch ・Poly Si gap-fill: Depo-Etch-Depo for void free fill	・Capacitor etch ・Dielectric deposition ・Metal deposition

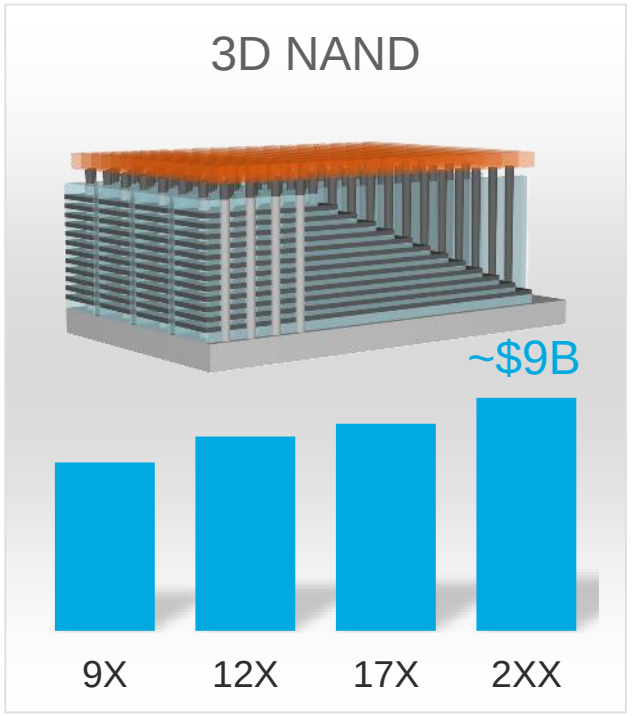
Increased importance of bonding technology, as well as etch and thin film deposition technology

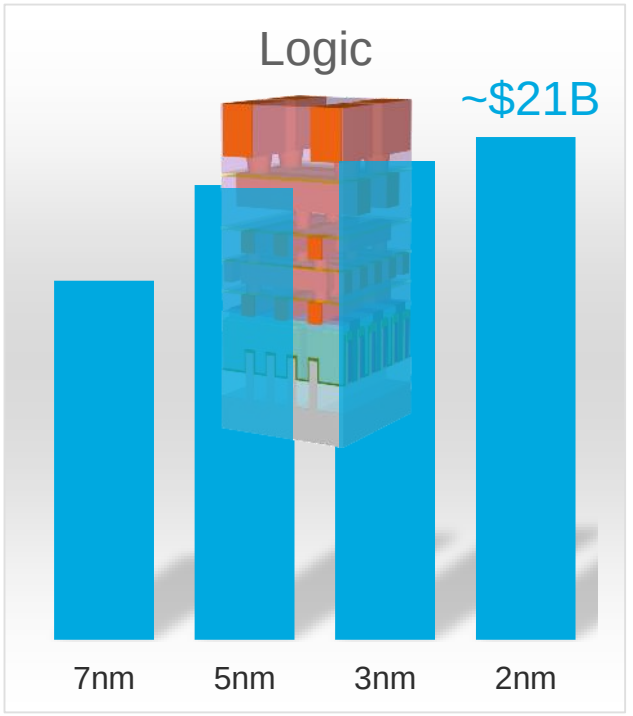
Summary

Raising Added-value in SPE

WFE investment (100k WSPM*, greenfield/TEL estimates)







Expanding business opportunities for SPE manufacturers on arrival of new applications and rising level of technological difficulty

 * WSPM: Wafer starts per month

Summary

- Market demands are becoming more complex
- To meet these needs, the evolution of devices is accelerating, including multifunctional devices
- Most of the multifunctionalization can be covered by existing process and system technologies, but technological evolution is also essential
- Technology development must be undertaken in alignment with environmental issues (SDGs)
- Development of advanced devices leads directly to the SDGs
- TEL's process development is conducted on a worldwide basis, and the company is strongly promoting the development of leading-edge devices through global collaboration both internally and externally
- Specific examples will be included in the following business unit announcements

TOKYO ELECTRON

Challenges and solutions for advanced EUV resist process technology

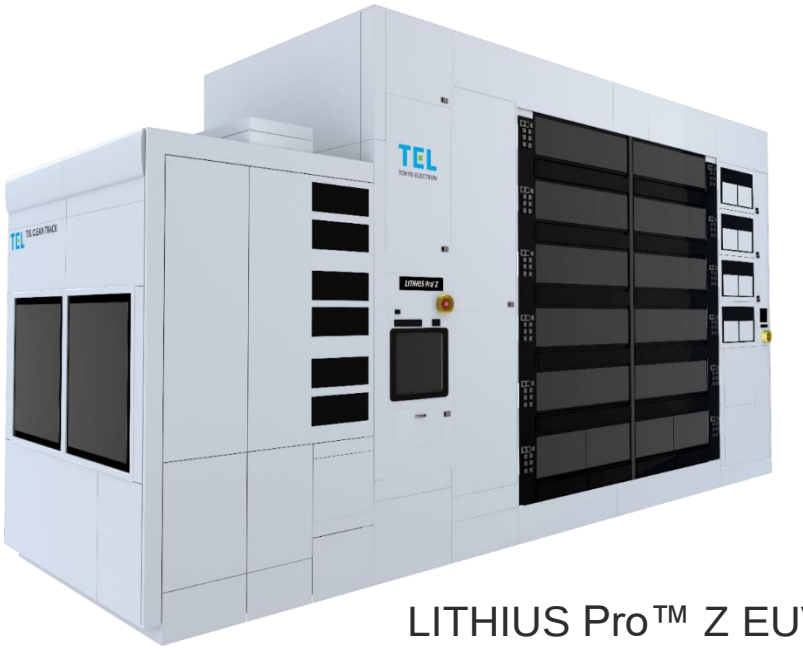
October 12, 2021

Keiichi Akiyama
VP & General Manager, CTSPS BU

CLEAN TRACK™ LITHIUS Pro™ Z EUV Coater/Developer for EUV

LITHIUS Pro™ Z released in 2012 (Total shipment > 1600 systems)

Releasing new EUV CAR/MOR compatible features



LITHIUS Pro™ Z EUV
Total shipment > 100 systems

High Reliability

100% market share in in-line coater/developer for EUV

High Productivity

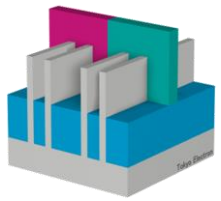
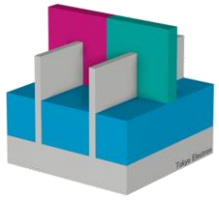
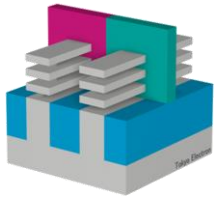
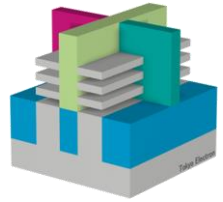
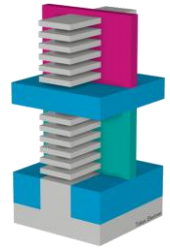
Maximizes EUV exposure tool performance

High Versatility

Applicable to Metal Oxide Resists and underlayers in addition to Chemically Amplified Resists

The LITHIUS Pro™ Z platform, which has a long track record of mass production for exposure tools with a variety of light sources, ensures high reliability and high productivity for EUV exposure tools. Also offers high versatility for next generation EUV

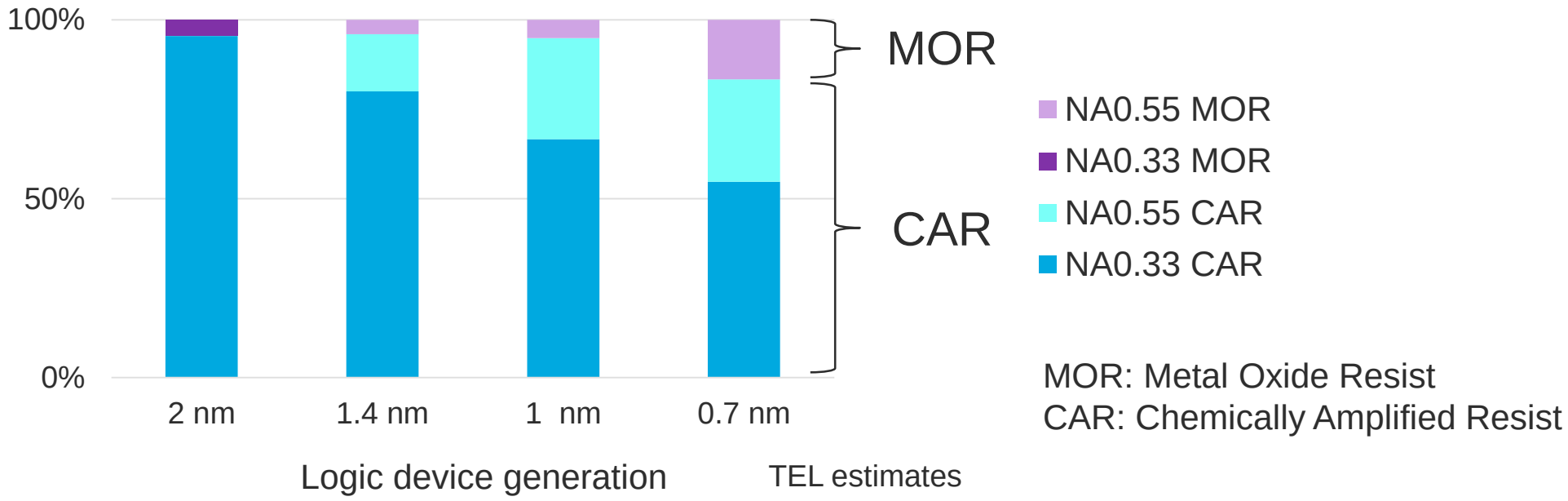
EUV Lithography Technology Roadmap in Logic

High volume production year	2020	2022	2024	2026	2028	2030
Node	5 nm	3 nm	2 nm	1.4 nm	1 nm	0.7 nm
Device	2 Fin 	2~1 Fin 	GAA NS 	Forksheet 	CFET 	2nd Gen. CFET 
Minimum metal pitch [nm]	**28**	**22**	**20**	**18**	**16**	**12**
EUV patterning technology	EUV MP	EUV MP	EUV MP	EUV MP **high-NA EUV**	EUV MP **high-NA EUV MP**	EUV MP **high-NA EUV MP**
Resist	**CAR**	**CAR (+MOR)**	**CAR (+MOR)**	**CAR+MOR**	**CAR+MOR**	**CAR+MOR**

CAR: Chemically Amplified Resist, MOR: Metal Oxide Resist, MP: Multi-patterning

Enhancing versatility of coater/developer to respond to future EUV lithography technologies including MOR and high-NA EUV

Forecast of EUV CAR/MOR Application Layer Counts in Logic Device

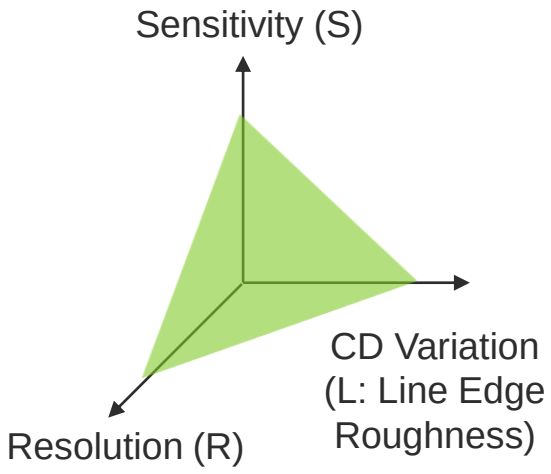


MOR ratio is gradually rising, but CAR ratio remains high.
Our coater/developer achieves high versatility by handling MOR and CAR in one system.
Technologies for high-NA (NA0.55) lithography are under development as it is expected to increase application

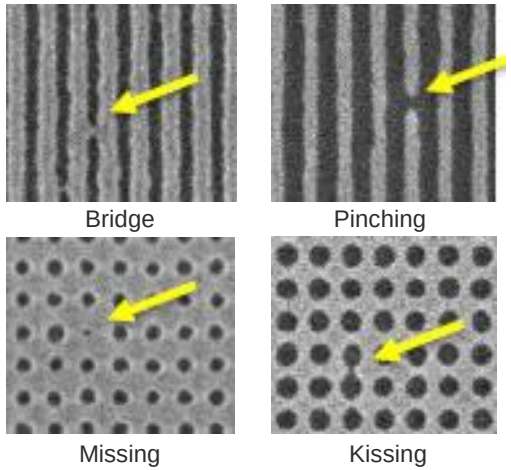
EUV Lithography Process Roadmap and Challenges

Line pitch (nm)	34	32	30	28	26	24	22	20
Hole pitch (nm)	42	40	38	36	34	32	30	22
Trend of EUV exposure equipment and resist technology	0.33 NA EUV				0.55 NA EUV (High-NA EUV: Higher resolution)			
	Chemically Amplified Resist (CAR)							
			Metal Oxide Resist (MOR)					

RLS trade off

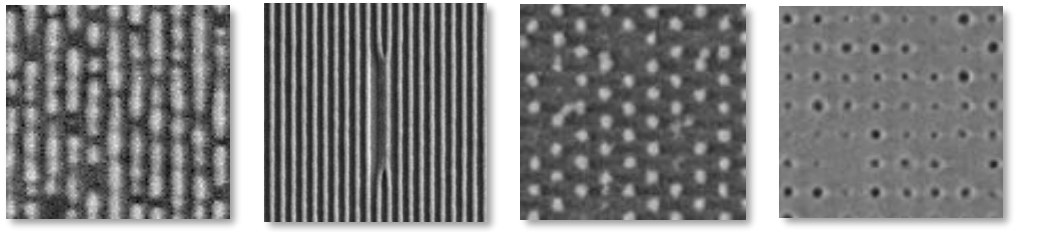


Defects induced by variation in EUV lithography



P. De Bisschop, Proc. SPIE, 10957-10 (2019)

Issue of securing required resist film thickness



Challenges for Thinning Resist Film ⟷ Challenges for Thickening Resist Film

EUV Lithography Process Roadmap and Challenges

Line pitch (nm)	34	32	30	28	26	24	22	20
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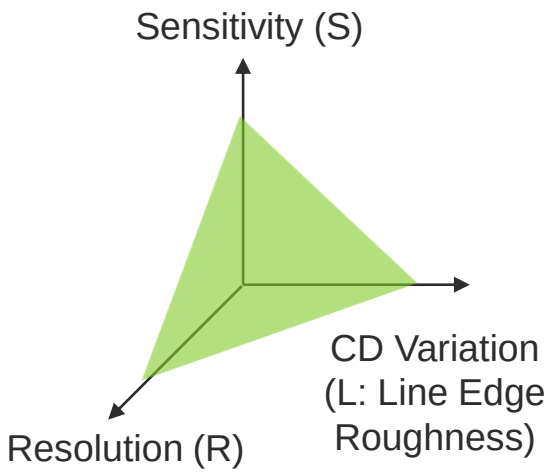
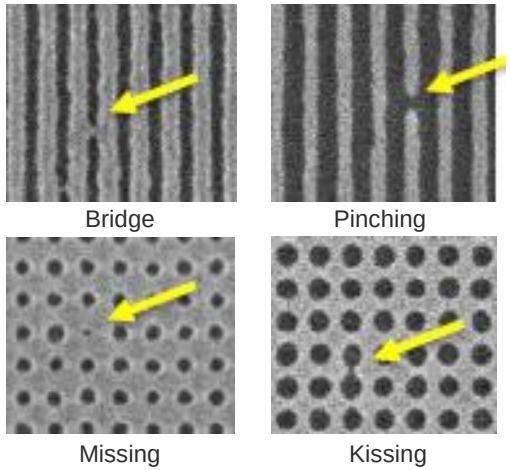
Trend of EUV exposure equipment and resist technology	0.33 NA EUV				0.55 NA EUV (High-NA EUV: Higher resolution)			
	Chemically Amplified Resist (CAR)							
			Metal Oxide Resist (MOR)					

RLS trade off

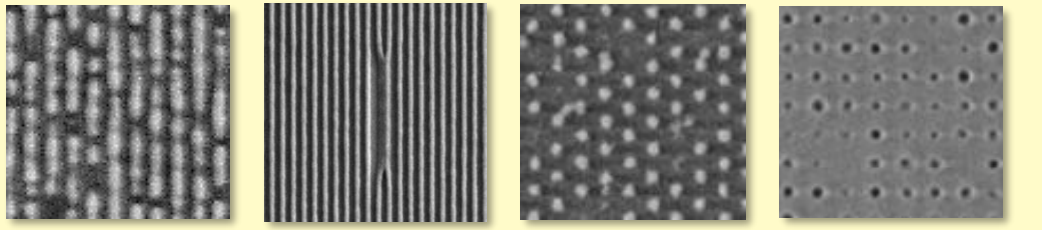


Defects induced by variation in EUV lithography



P. De Bisschop, Proc. SPIE, 10957-10 (2019)

Issue of securing required resist film thickness



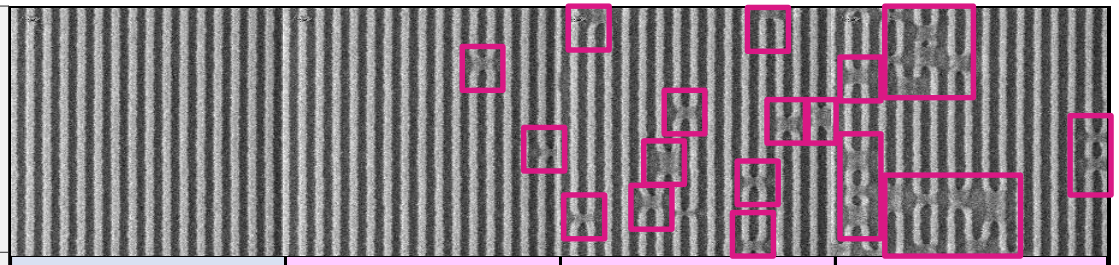
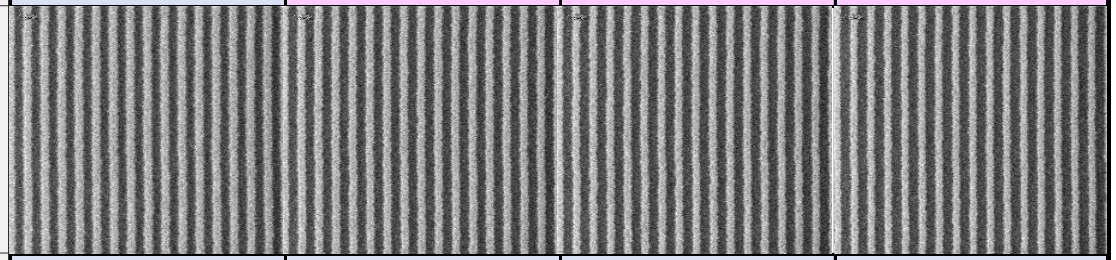
Challenges for Thinning Resist Film ⟷ Challenges for Thickening Resist Film

Solution Example for CAR Technology Mass Production Challenge:

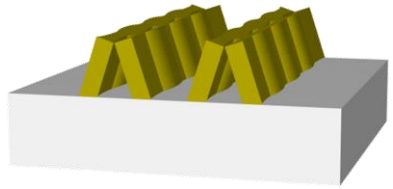
Technology to Prevent Collapse of Extremely Miniaturized Resist Line Patterns in Wet Development

Example of 28 nm pitch 14 nm line formation with 38 nm resist film thickness

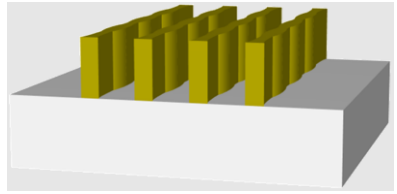
EUV exposure dose

Existing post development rinse process				
Resist CD (nm)	**14.0**	13.4	12.5	11.7
New post development rinse process				
Resist CD (nm)	14.0	13.1	12.4	**11.8**

Resist Collapse



No Resist Collapse



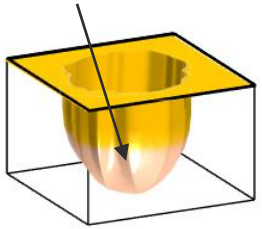
New technology prevents pattern collapse even at 11.8 nm pattern size

New post-development rinse technology prevents pattern collapse for high aspect ratio CAR, realizing wide margin for high volume production process

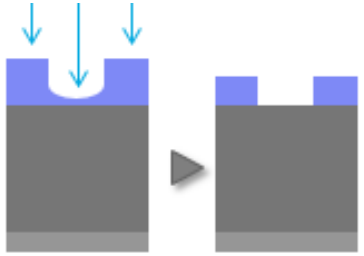
Solution Example for CAR Technology Mass Production Challenge:

Nanohole Formation Through Optimization of Lithography and Etch Technology

Issue of Residue
Inside Hole

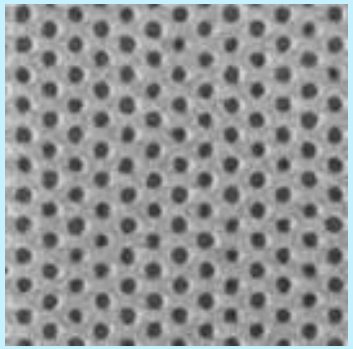


Removal of Residue
Inside Hole by Etch



36 nm pitch 18 nm hole
Dense contact hole patterning

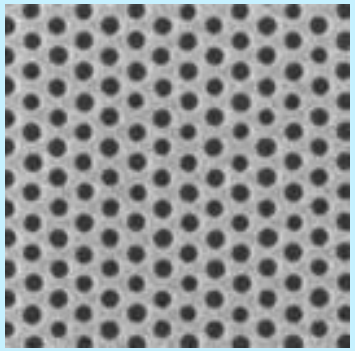
After lithography



Source: imec

18 nm hole size

After etch



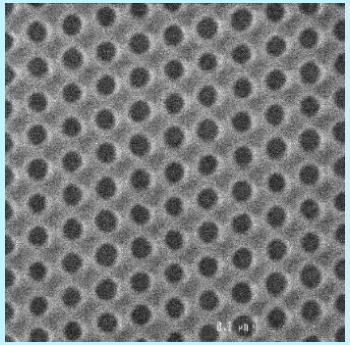
Source: imec

20 nm hole size

Size expansion

46 nm pitch 23 nm hole
13 nm contact hole patterning

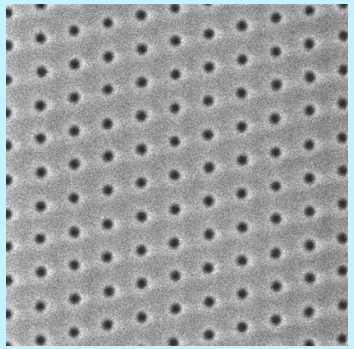
After lithography



Source: TEL

23 nm hole size

After etch



Source: TEL

13 nm hole size

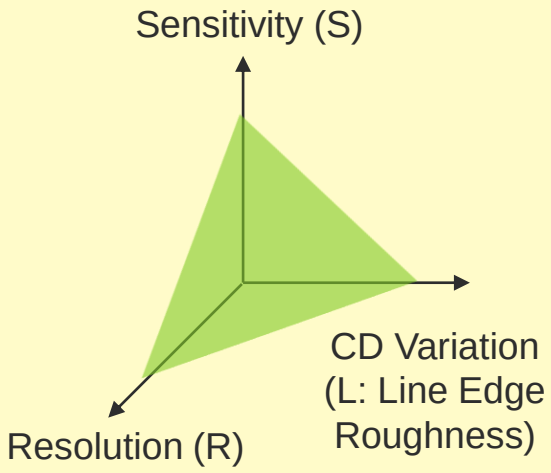
Size reduction

Resolving issue of residue from resist development by optimization through integrating EUV lithography and etch process technologies

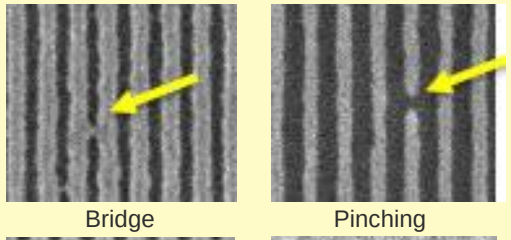
EUV Lithography Process Roadmap and Challenges

Line pitch (nm)	34	32	30	28	26	24	22	20
Hole pitch (nm)	42	40	38	36	34	32	30	22
Trend of EUV exposure equipment and resist technology	0.33 NA EUV				0.55 NA EUV (High-NA EUV: Higher resolution)			
	Chemically Amplified Resist (CAR)							
	Metal Oxide Resist (MOR)							

RLS trade off

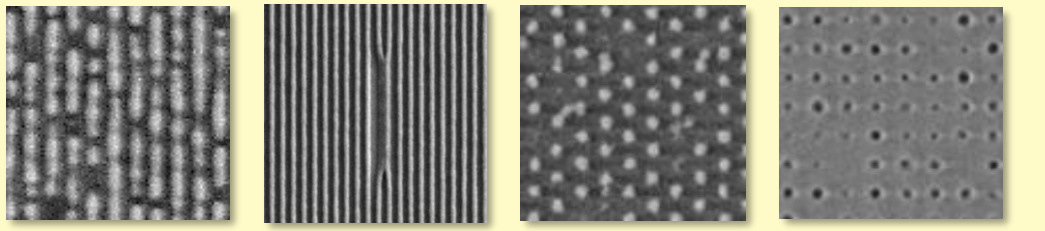


Defects induced by variation in EUV lithography



P. De Bisschop, Proc. SPIE, 10957-10 (2019)

Issue of securing required resist film thickness

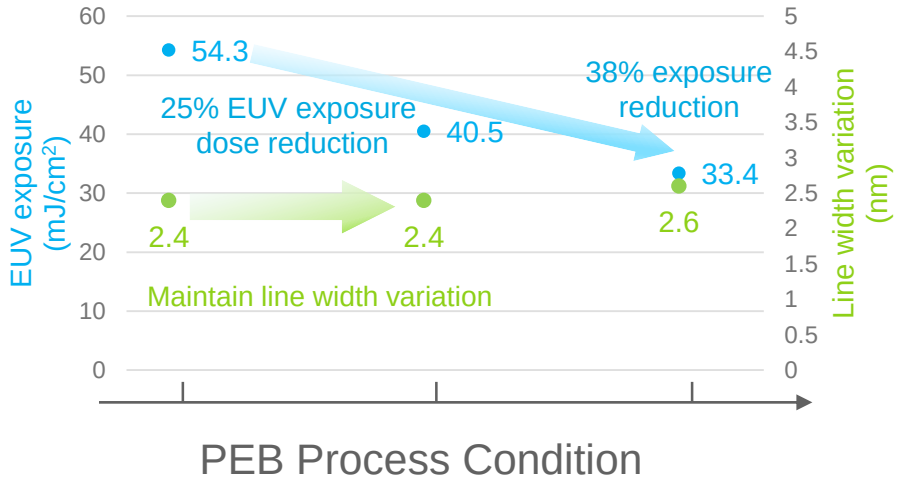


Challenges for Thinning Resist Film ⟷ Challenges for Thickening Resist Film

Solution Example for MOR Technology Mass Production Challenge:

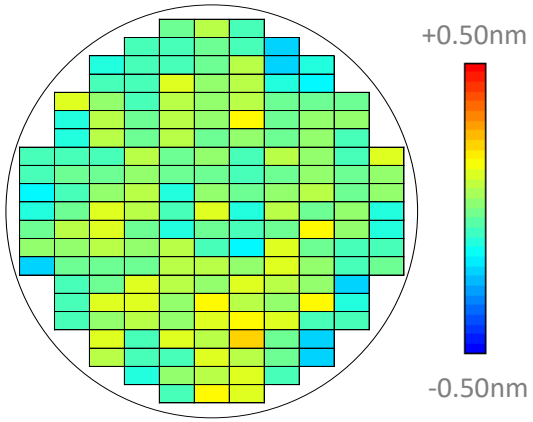
Introduction of Newly Developed Post Exposure Bake (PEB) Oven for MOR

32 nm pitch 16 nm line Increased sensitivity through PEB process



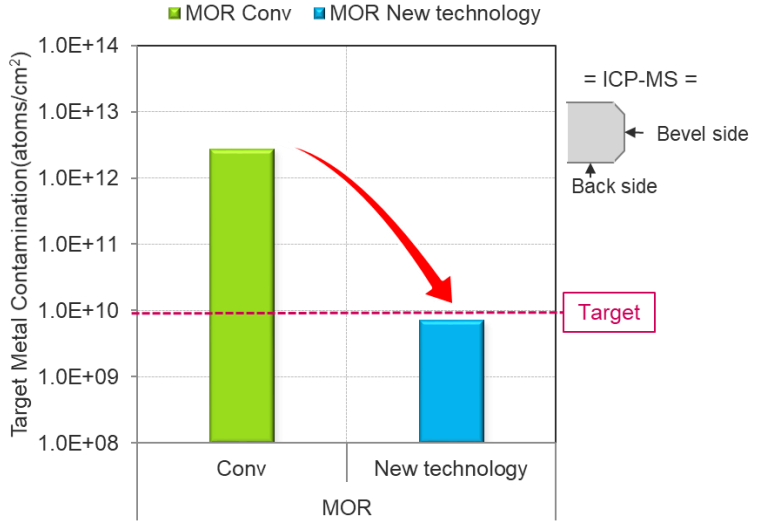
EUV sensitivity > 20% (<40 mJ/cm²)

High-precision resist thickness control through new PEB oven



Resist uniformity of ~0.2 nm within wafer

Measures against metal contamination using new PEB oven



Low metal contamination <1E10 atoms/cm²

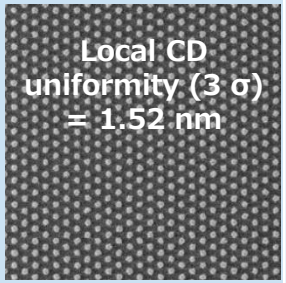
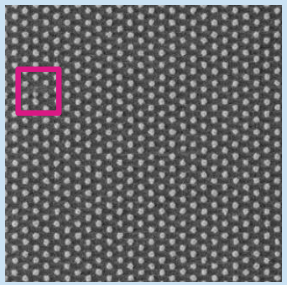
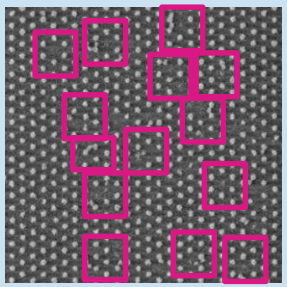
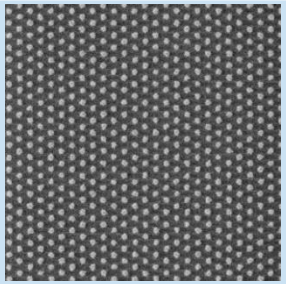
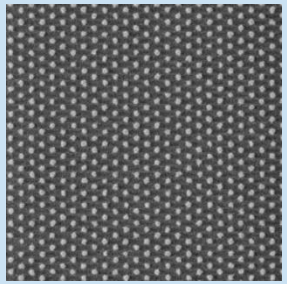
Newly developed MOR-compatible PEB oven enables process for mass production

Solution Example for MOR Technology Mass Production Challenge:

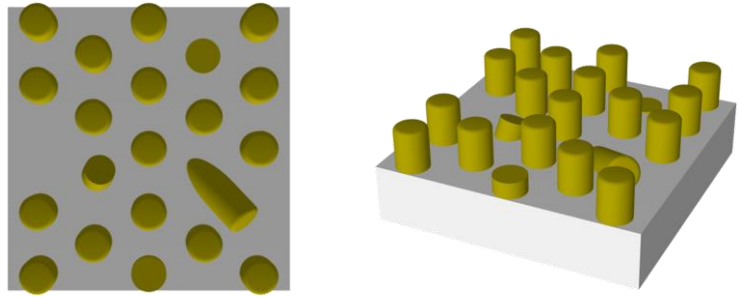
Newly Developed Wet Development Technology

36 nm pitch 18 nm pillar for DRAM (after lithography)

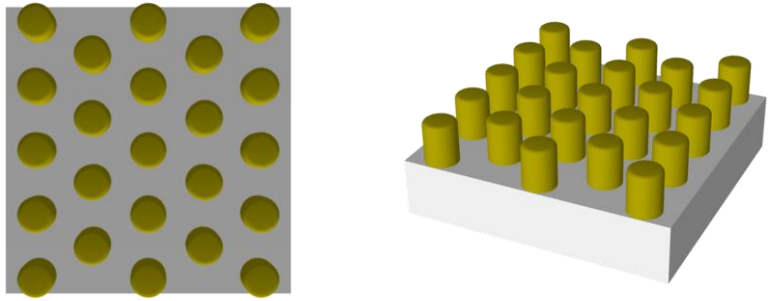
Resist film thickness: 22 nm

Existing wet development technology	 Source: TEL	 Source: TEL	 Source: TEL
	CD 18.0 nm EUV exposure 99.5 mJ/cm²	16.8 nm 93.5 mJ/cm²	15.1 nm 86.0 mJ/cm²
Newly developed wet development technology	 Source: TEL	 Source: TEL	 Source: TEL
	CD 18.0 nm EUV exposure 75.5 mJ/cm²	16.7 nm 69.5 mJ/cm²	15.2 nm 66.5 mJ/cm²

Resist collapse with existing development technology



New wet development technology prevents resist collapse



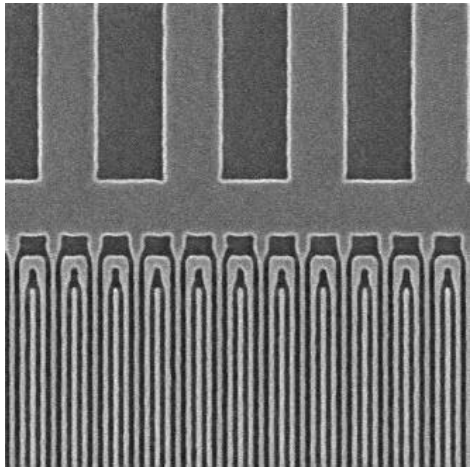
New wet development technology prevents resist collapse, reduces EUV exposure dose by 25% and decreases thickness variations

Solution Example for MOR Technology Mass Production Challenge:

Module Solution Integrated with Etch

Roughness after etch

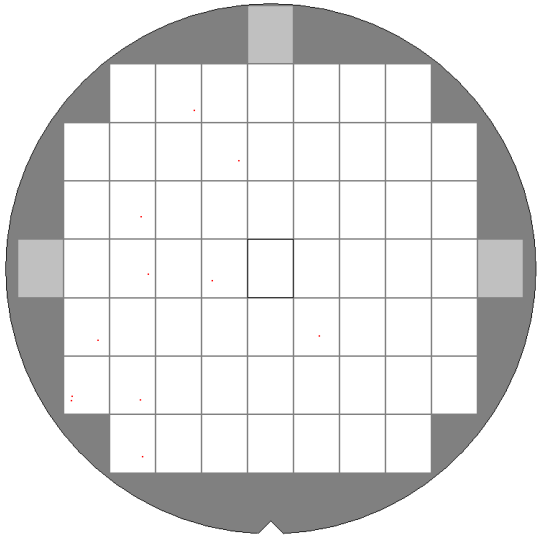
30 nm pitch 15 nm line

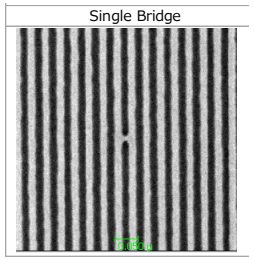


Source: TEL

Bridge defect after etch

32 nm pitch 16 nm line



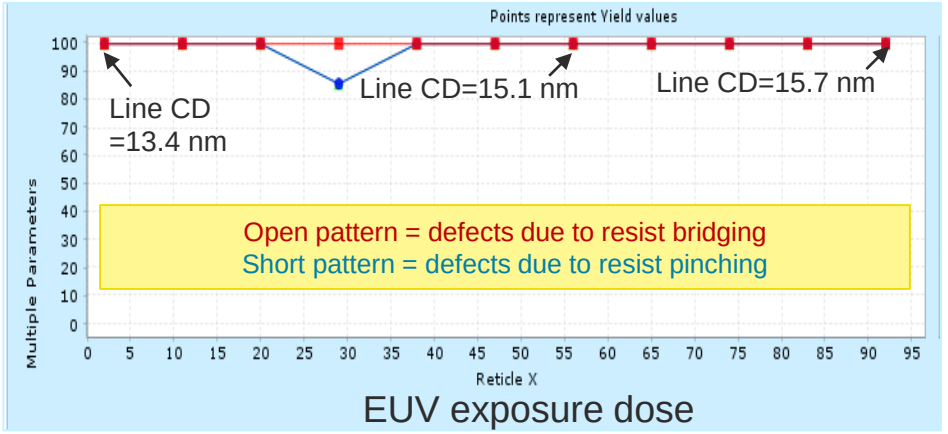


Source: TEL

Electric characteristics data

30 nm pitch 15 nm line interconnects pattern

1 mm length macro



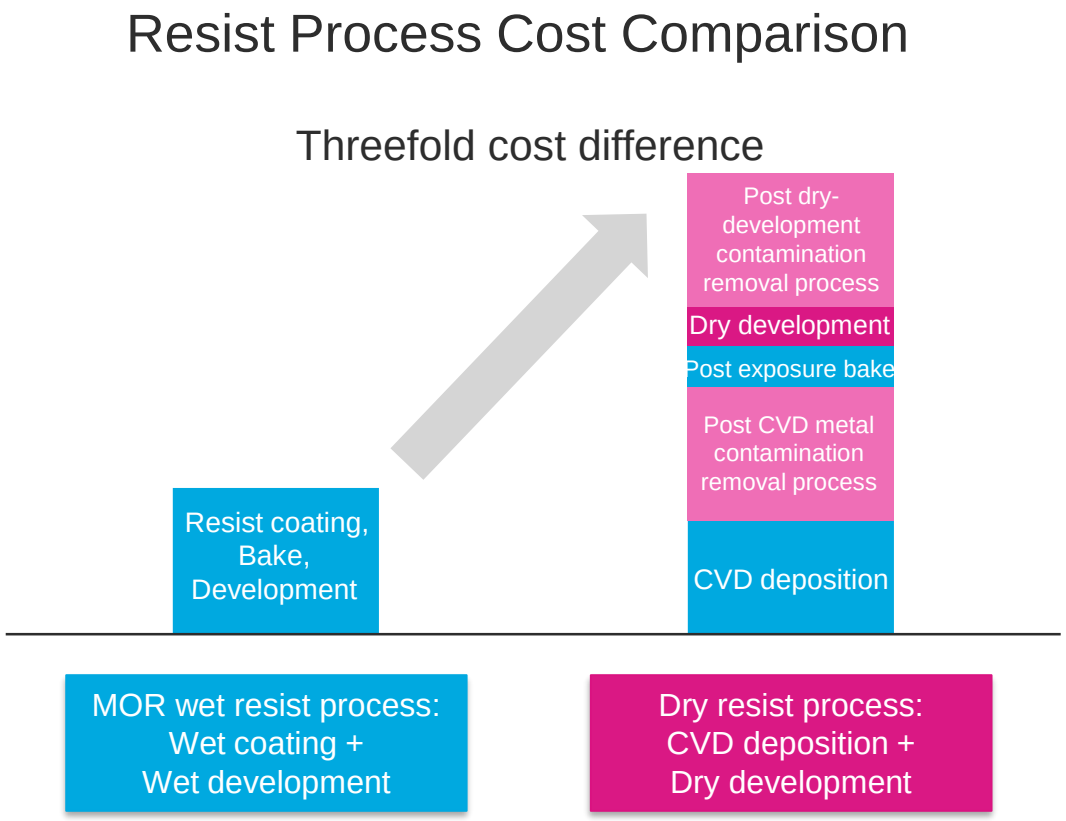
After etch LWR <1.8 nm
(imec standard SEM recipe)

Bridge defect density DD: < 0.1 /cm^2

Achieved almost 100% yield on test pattern

MOR enabled low defects, low roughness and high yield at device mass production level

MOR Wet Resist Process and Dry Resist Process Cost Comparison



Dry film deposition and dry development process CoO is around three times higher than for wet coating and development

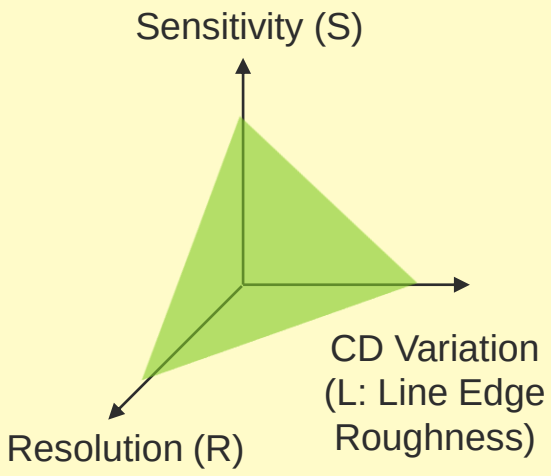
TEL estimates

MOR wet resist process is superior to dry resist process (CVD＋dry development) not only in terms of operational advantages including cost, TAT, queue time management, equipment footprint and power consumption, but the wet process also demonstrates superior data in terms of process performance

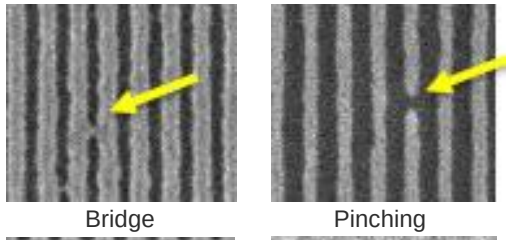
EUV Lithography Process Roadmap and Challenges

Line pitch (nm)	34	32	30	28	26	24	22	20
Hole pitch (nm)	42	40	38	36	34	32	30	22
Trend of EUV exposure equipment and resist technology	0.33 NA EUV			0.55 NA EUV (High-NA EUV: Higher resolution)				
	Chemically Amplified Resist (CAR)							
			Metal Oxide Resist (MOR)					

RLS trade off

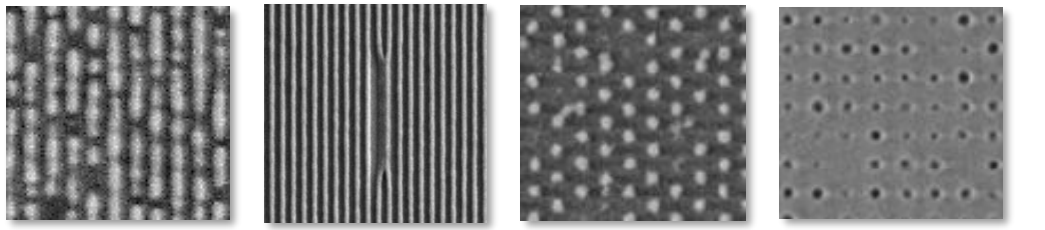


Defects induced by variation in EUV lithography



P. De Bisschop, Proc. SPIE, 10957-10 (2019)

Issue of securing required resist film thickness



Challenges for Thinning Resist Film ⟷ Challenges for Thickening Resist Film

Preparing for High-NA EUV Generation:
Working with Partners to Address Challenges

Notification Jun 8, 2021

Tokyo Electron to Collaborate with imec-ASML Joint High NA EUV Research Laboratory

Tokyo Electron (TEL; Head Office: Minato-ku, Tokyo; President: Toshiki Kawai) announced today the company will introduce its leading-edge Coater/Developer to the imec-ASML joint high NA EUV research laboratory (joint high NA lab) in Veldhoven, the Netherlands. The equipment will be integrated inline* with EXE:5000, ASML's next-generation high NA EUV lithography system with a 0.55 numerical aperture (NA), scheduled to be operational in 2023. By collaborating with imec and ASML, TEL will continue to pursue technological development to meet the ongoing scaling needs of its customers.

High NA EUV lithography is expected to provide more advanced pattern scaling solutions compared to conventional EUV lithography. The Coater/Developer being introduced to the joint high NA lab will feature advanced capabilities which are not only compatible with widely used chemically amplified resists and underlayers, but are also compatible with spin-on metal-containing resists. Spin-on metal-containing resists have demonstrated high resolution and high etch resistance, and are expected to enable finer patterning. However, metal-containing resists also require sophisticated pattern size control as well as metal contamination control on the backside and bevel of the wafer. To meet these challenges, the Coater/Developer being installed at the joint high NA lab comes with leading-edge process modules capable of handling metal-containing resists.

Combined with the new process modules, a single unit of TEL Coater/Developer can process a wide variety of materials inline, including chemically amplified resists, metal-containing resists, and underlayers. This will enable flexible fab operation, while also realizing increased productivity and high availability that are among the advantages of a Coater/Developer.

Taking advantage of the breadth of its products spanning several adjacent processes, TEL is forming a partnership with resist materials suppliers to provide comprehensive patterning solutions covering etch processes as well as Coater/Developer for lithography processes.

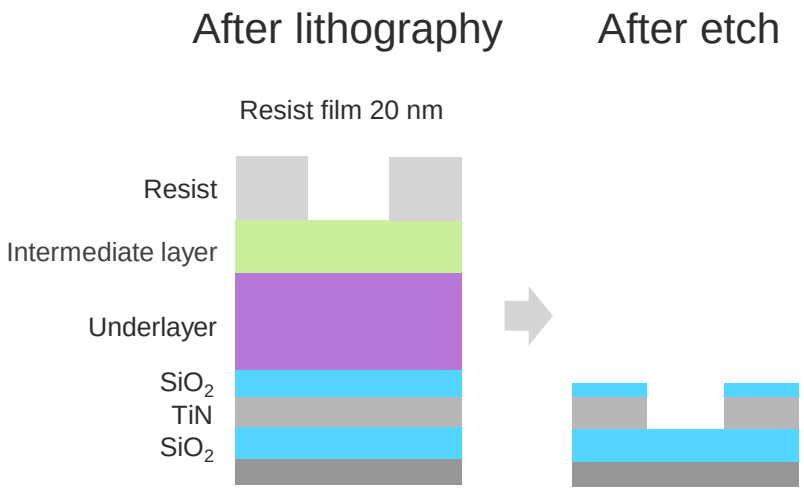
Inline coater/developer into high-NA EUV exposure tool

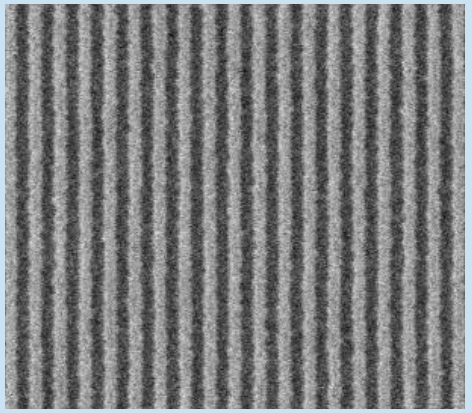
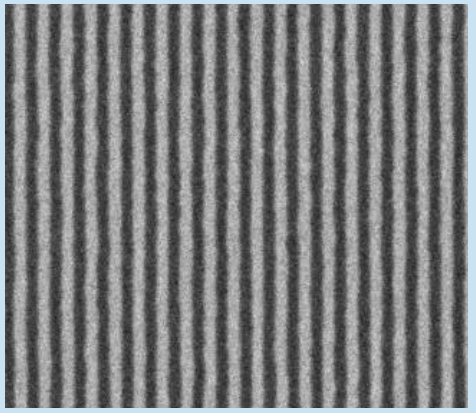
Plan to build nano patterning technology with high-NA EUV in cooperation with imec and ASML

https://www.tel.com/news/topics/2021/20210608_001.html

Preparing for High-NA EUV Generation:
Demonstration of Nano Patterning with MOR

24 nm pitch 12 nm line



	After lithography	After etch
EUV exposure pattern	 Source: imec	 Source: imec
CD (nm)	12.7	12.1
LER (nm)	2.13	1.56
LWR (nm)	2.88	1.94

imec standard SEM recipe, demo with NA0.33

Wet development achieves 12 nm line pattern without collapse with roughness (LER/LWR) of less than 2 nm

Summary

- Realize new technology for EUV utilizing Chemically Amplified Resist (CAR) by the synergies between lithography and etch

- Introduce Metal Oxide Resist (MOR) technology for mass production.
  Achieve high performance/low cost process.
  Perform both CAR and MOR in one system

- Toward high-NA EUV lithography technology, collaborate with partners and provide leading-edge coater/developer process solutions for the mass production of future generations of devices

CLEAN TRACK™ LITHIUS Pro™ Z EUV

TOKYO ELECTRON

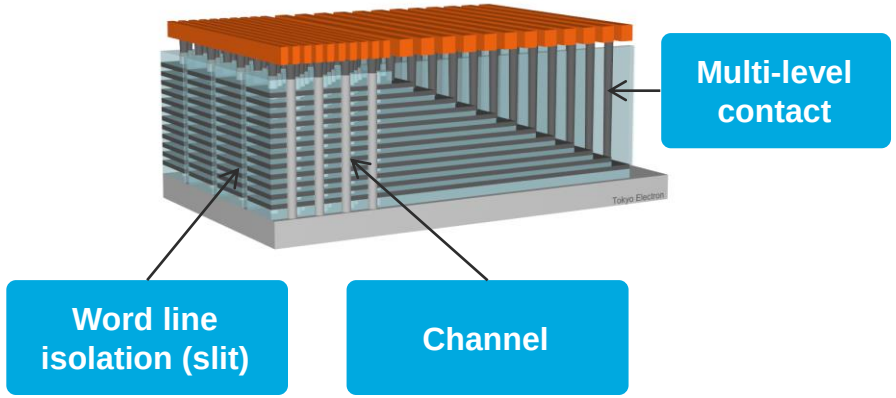
Latest technological challenges and TEL's activities in etch

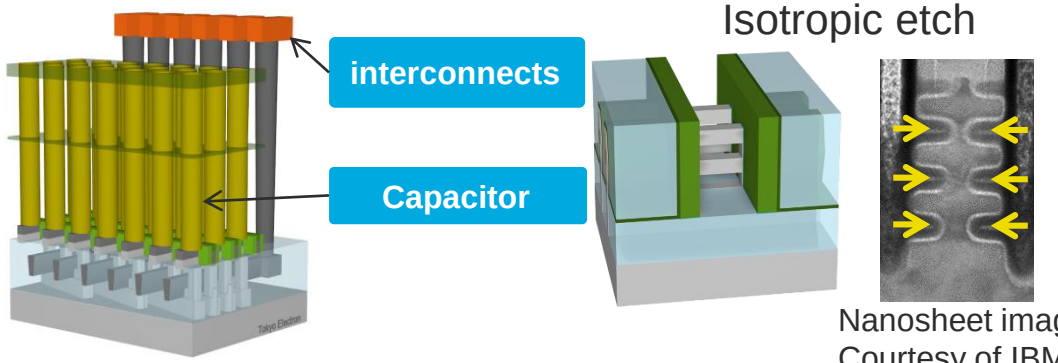
October 12, 2021

Isamu Wakui
VP & General Manager, ES BU

Etch System Strategy

- HARC process
  - 3D NAND (multi-level contact, word line isolation), DRAM (capacitor): Continue to differentiate through process performance and productiv
  - 3D NAND (channel): Launch new systems that can differentiate by providing both precise process controllability and even higher productivity
- Patterning process
  - DRAM: Differentiate with reduced manufacturing costs for customers through process control and combining etch steps
  - Logic: Differentiate through integration of etch and deposition technologies
- Interconnect/contact process
  - Apply knowledge cultivated in logic to DRAM
- Gas chemical etch process
  - Create a new market through plasma assist technology



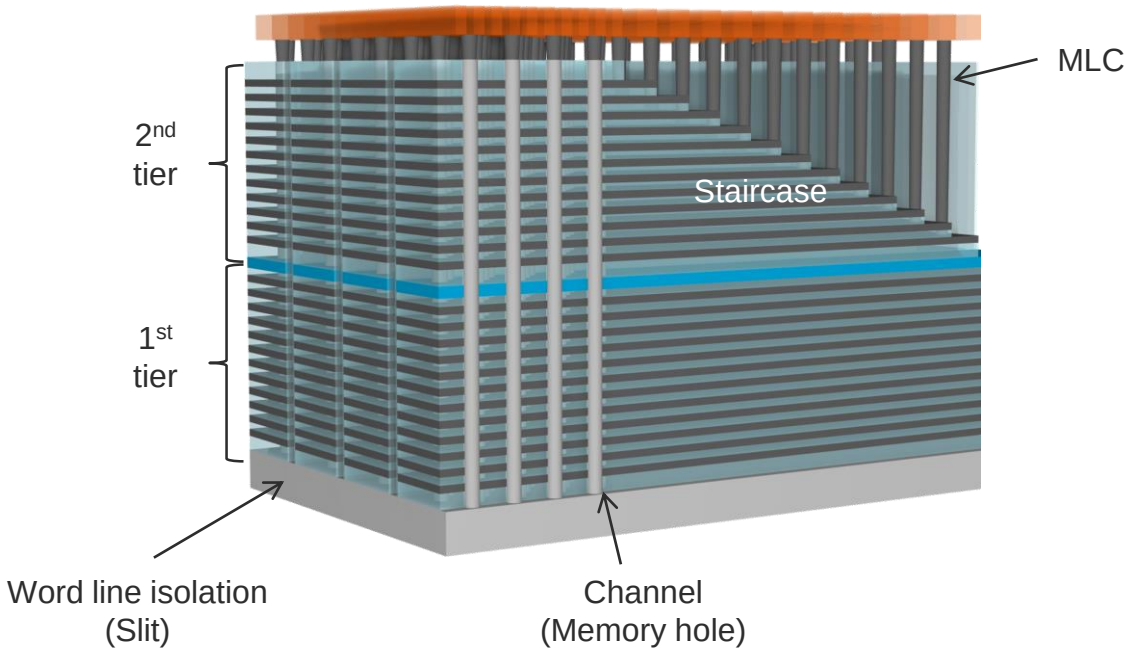


Nanosheet image: Courtesy of IBM

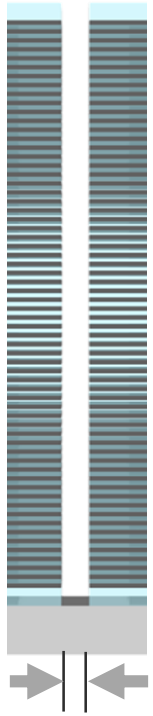
Source: N. Loubet, *et al.*, Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET

Business Opportunities in Memory

3D NAND

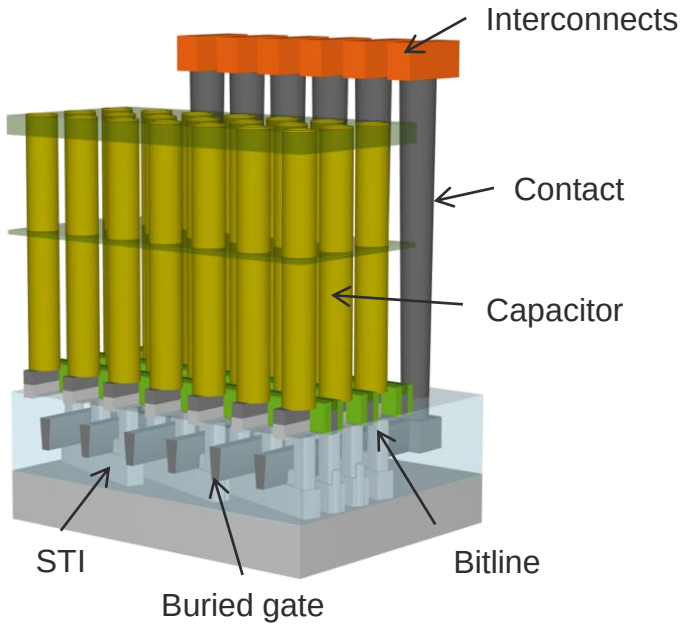


Aspect ratio 70:1



Diameter 100 nm

DRAM

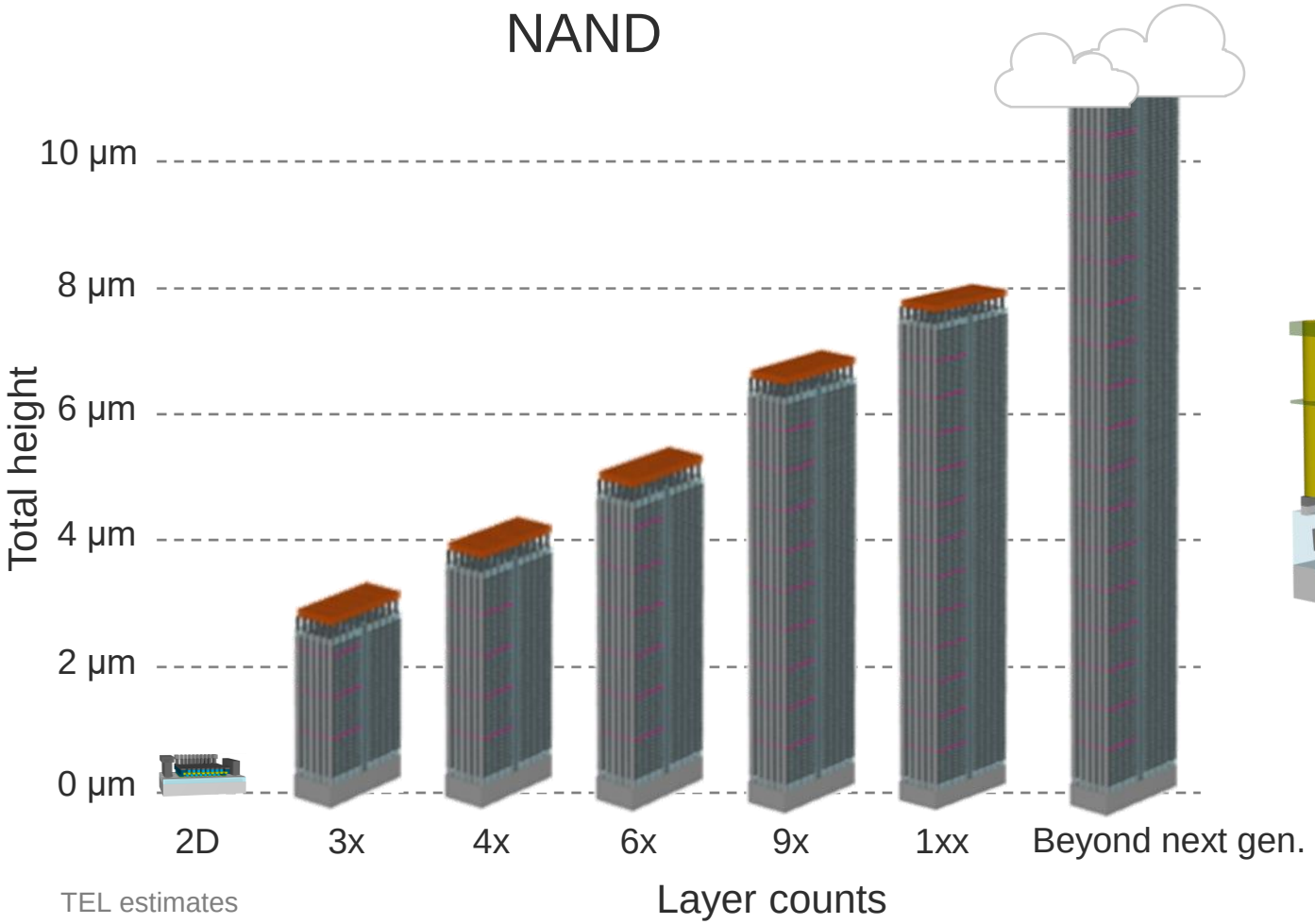


Respond to growing dry etch business opportunities in NAND/DRAM

- Etch performance that corresponds with higher aspect ratios
- Contribution to improvement of customers' productivity

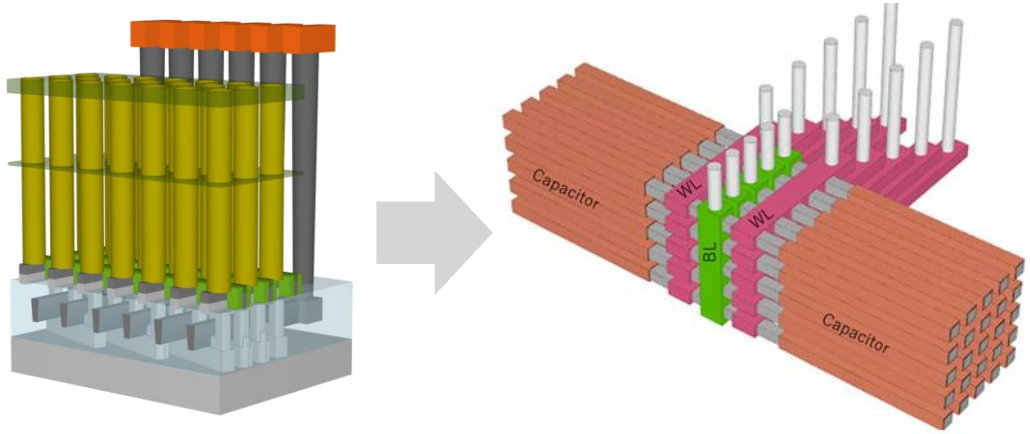
Multi-layering in Memory

NAND



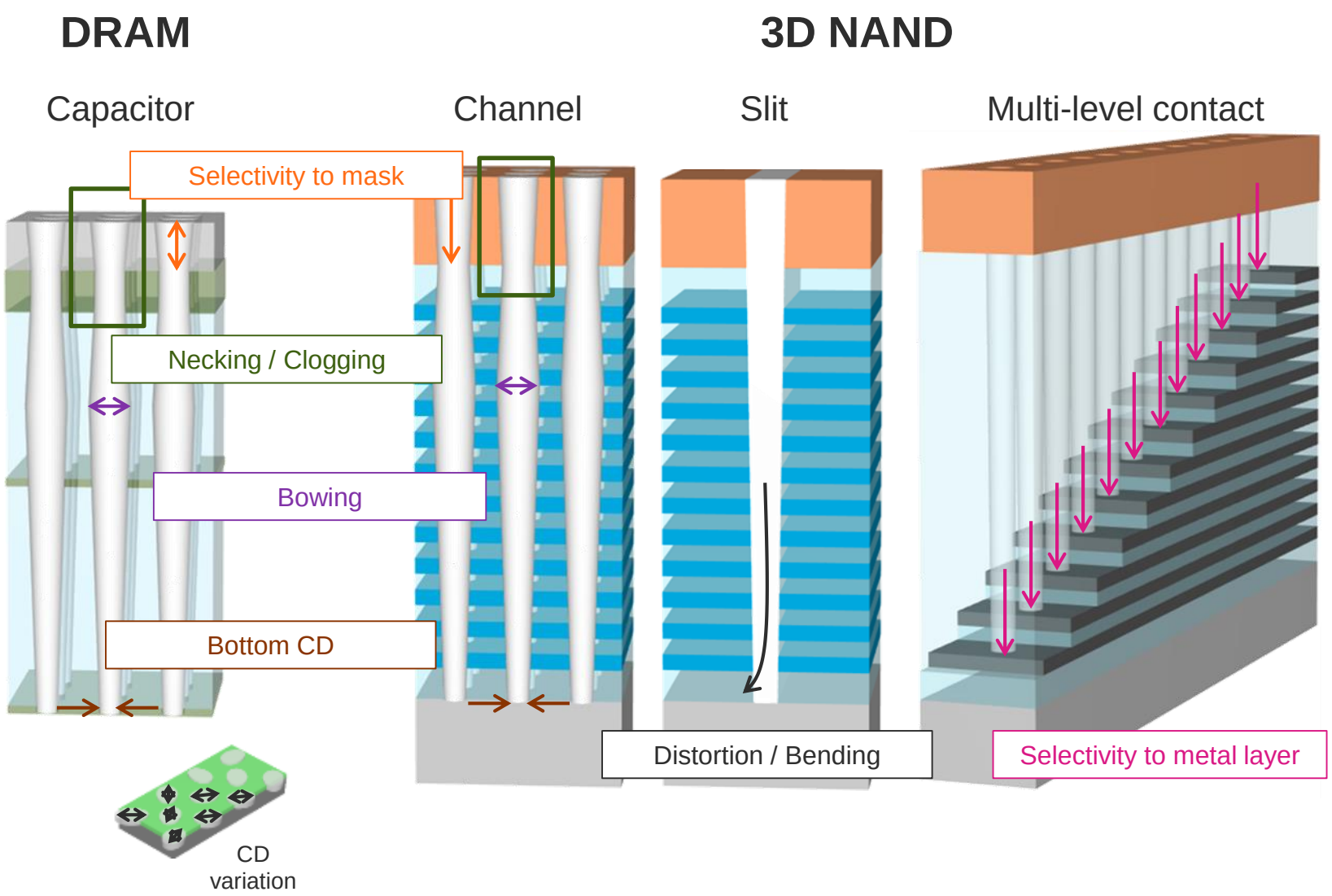
TEL estimates

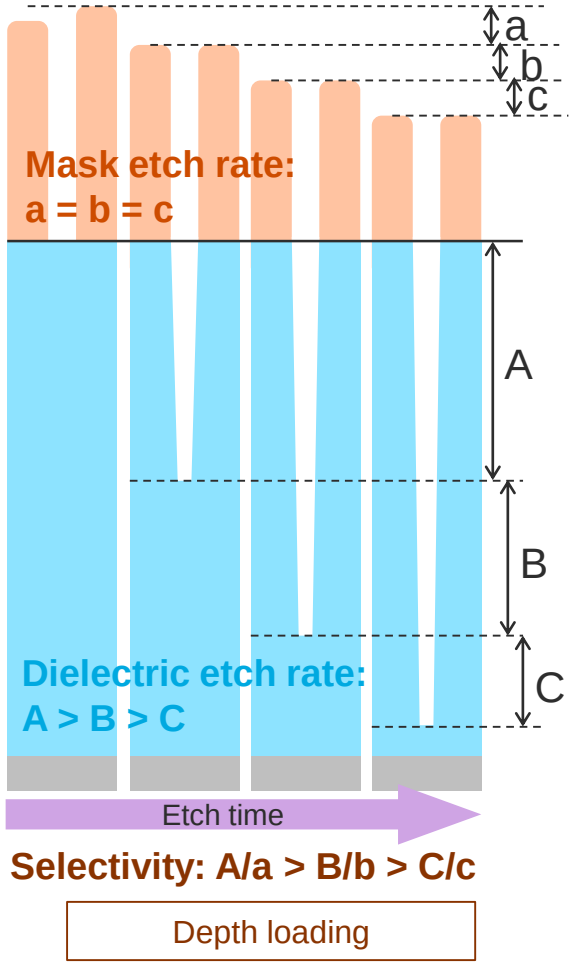
DRAM



Etch market growing due to continuing 3D multi-layering

Challenges in High Aspect Ratio Dielectric Etch

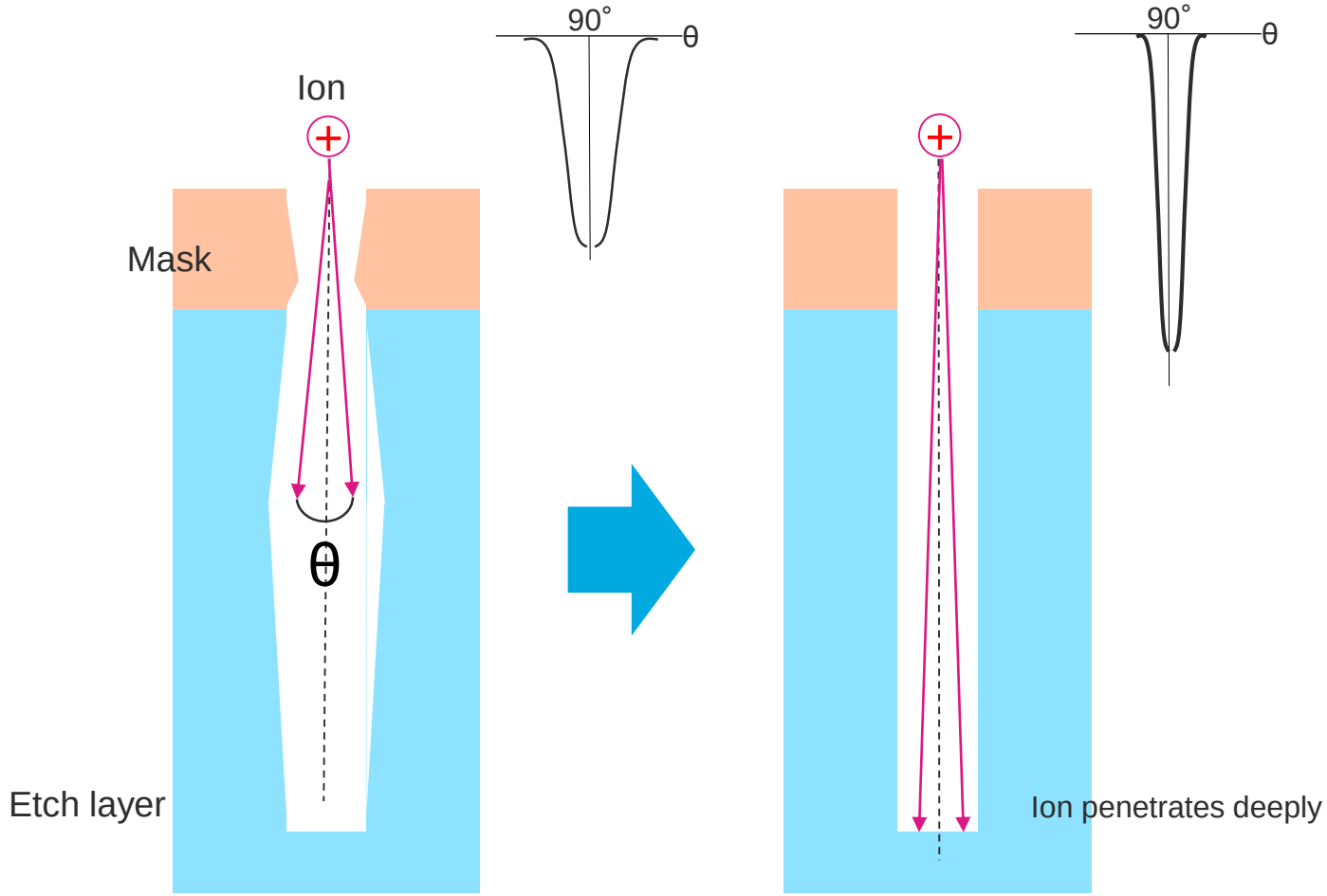




Solution Aspect Ratio Etch

Results of TEL's technology:

- Precise process control for high aspect ratio etch
- Improved etch rate due to reduced depth loading

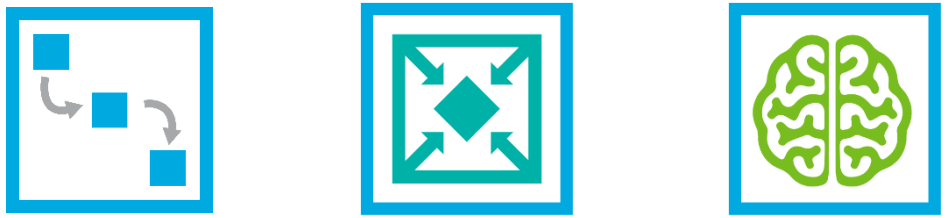


Realize higher aspect ratio etch process through TEL's original ion angular distribution control technology

Enhancing Productivity

Features of the Episode™ UL

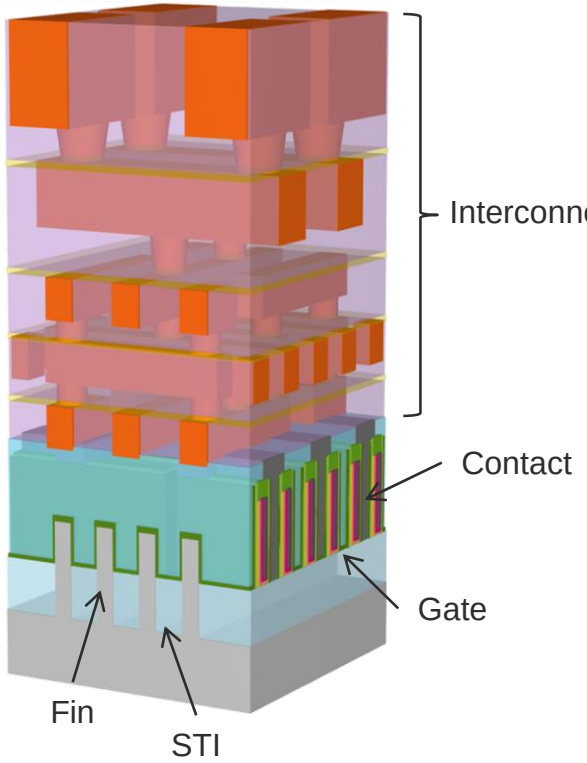
- Flexible layout
  - Select flexibly from 4 to 12 chambers
- Space saving
  - Significantly reduced footprint per chamber
- Smart tool
  - Autonomous process control through big data analysis

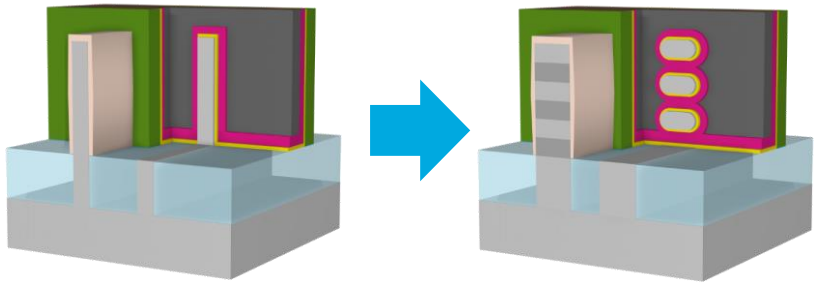


FLEXIBLE LAYOUT SPACE SAVING SMART TOOL

Introduction of new platform (for both memory and logic) contributes to enhancing productivity

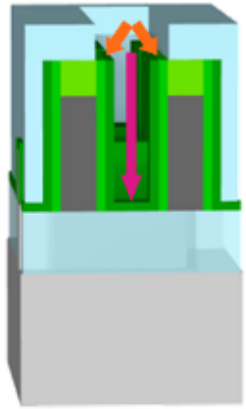
Business Opportunities in Logic



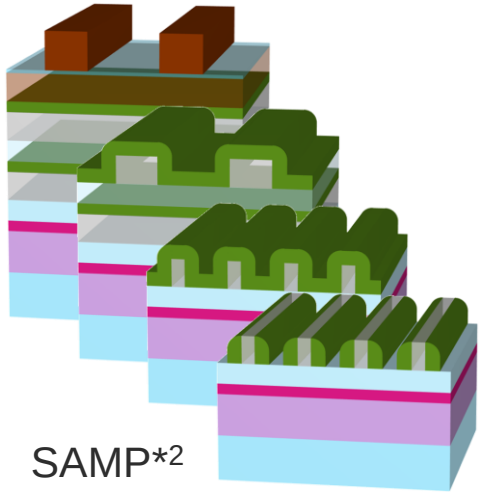


FinFET

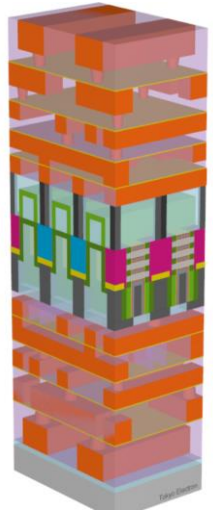
GAA*1 Nanosheet



Self-aligned Contact



SAMP*2



Backside PDN*3

*1 GAA: Gate all around
*2 SAMP: Self-aligned multiple patterning
*3 PDN: Power delivery network

Respond to changes in device manufacturing and EUV lithography for further scaling

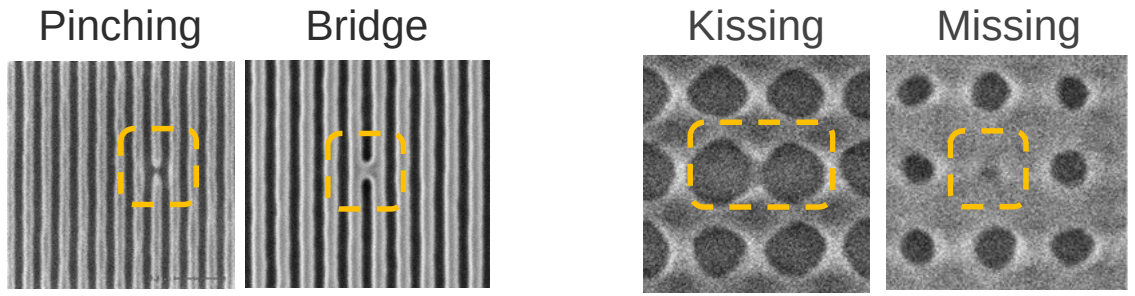
Etch for EUV Lithography

Challenges in etch for EUV

- Large defects and variation compared with ArF
- Extremely thin, low resistance to plasma

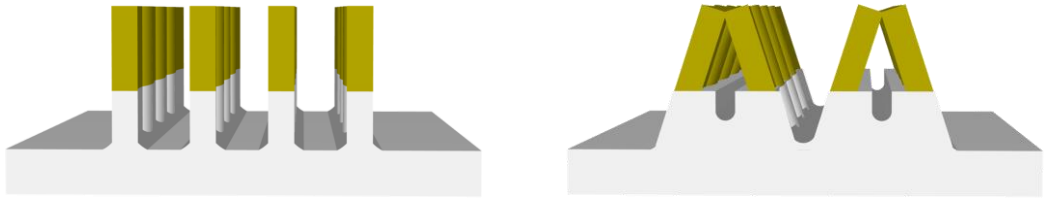
Compensation by etch technology becomes important

Pattern after EUV lithography



Source: S. Morikita, et al., Tokyo Electron Miyagi (DPS2018)

Effect of dry etch on EUV resist

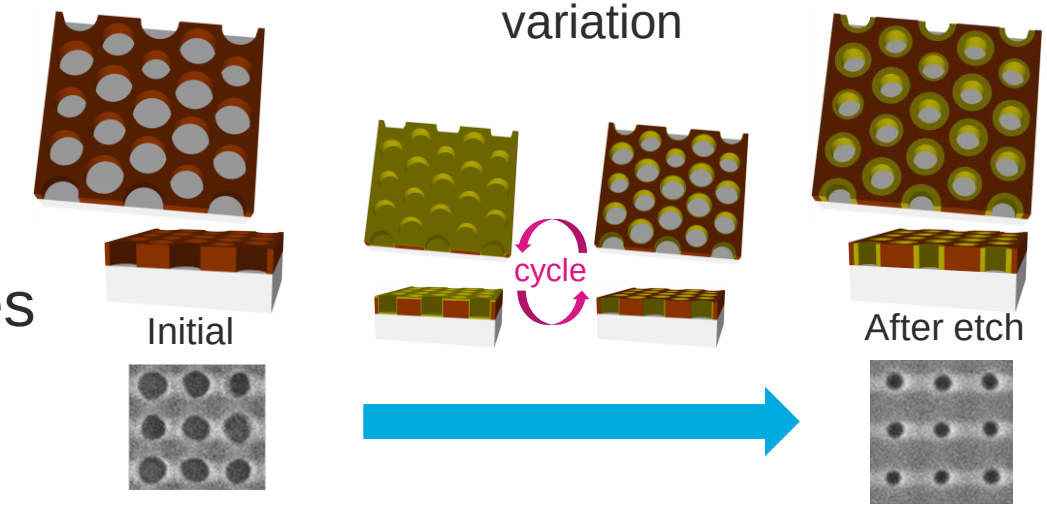


Etch Solution toward EUV Lithography

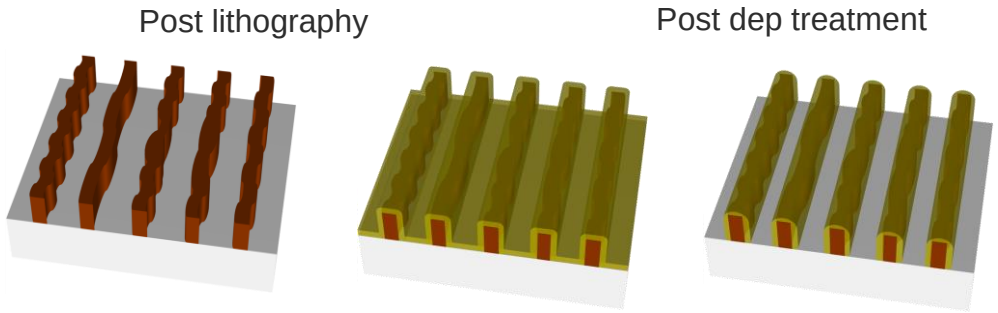
TEL's initiatives

- Improve post-lithography variation by repeating deposition and etch processes
- Improve mask selectivity by leaving film on resist
- Leverage collaborations with imec and ASML and realize patterning solutions for high NA generation

Combining deposition and etch to improve variation



Improved selectivity by deposition on resist followed by plasma treatment

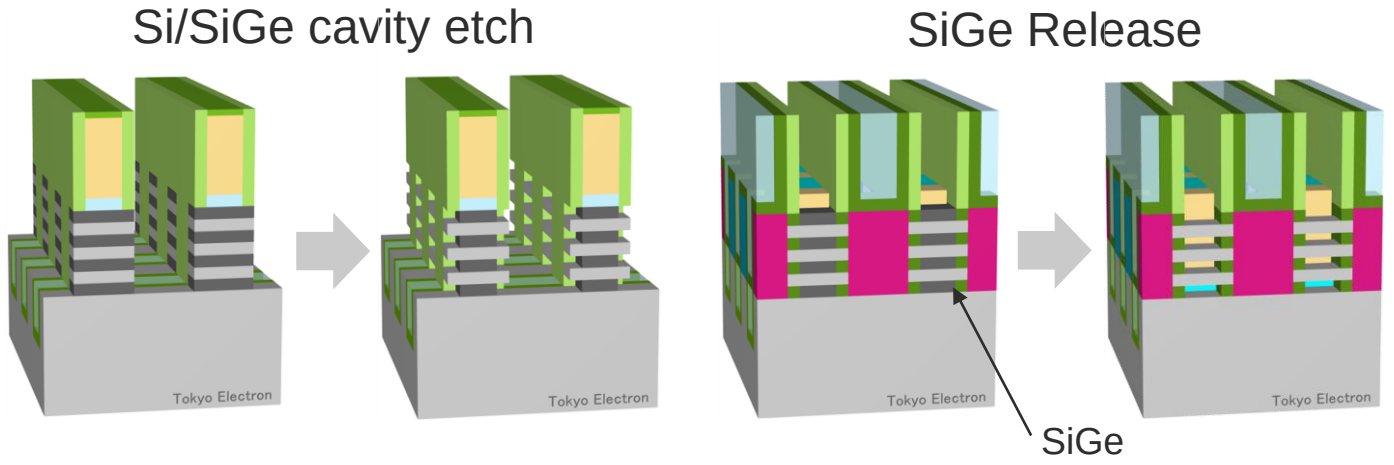


Combining deposition and etching to improve variation and etch selectivity

Initiative for GAA Nano Sheet Structures

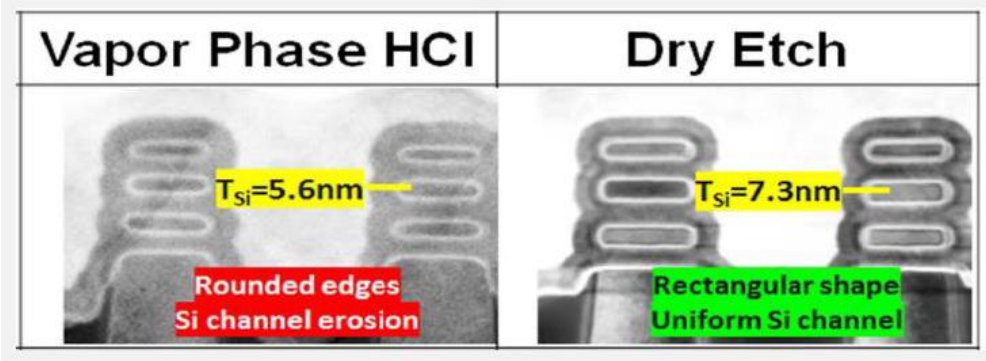
Nano Sheet process challenges:

- Uniformity in rectangle shape
- Mitigation of roughness/residue on patterned surface



TEL's initiative: Gas chemical etch

- High etch selectivity
- High uniformity
- Residue removal/decreased roughness



Source: N. Loubet, et al., IBM, TEL Technology Center, America (IEDM2019)

Leveraging the advantages of gas chemical etch to contribute to leading-edge processes

Enhancement of Development and Production Capabilities

Completed Miyagi Technology Innovation Center on September 22, 2021

- Lab area with partner companies
- Open innovation area
- Customer training center

Tokyo Electron Miyagi's Miyagi Technology Innovation Center

Create innovative technologies and enhance production capabilities through co-creation with partner companies

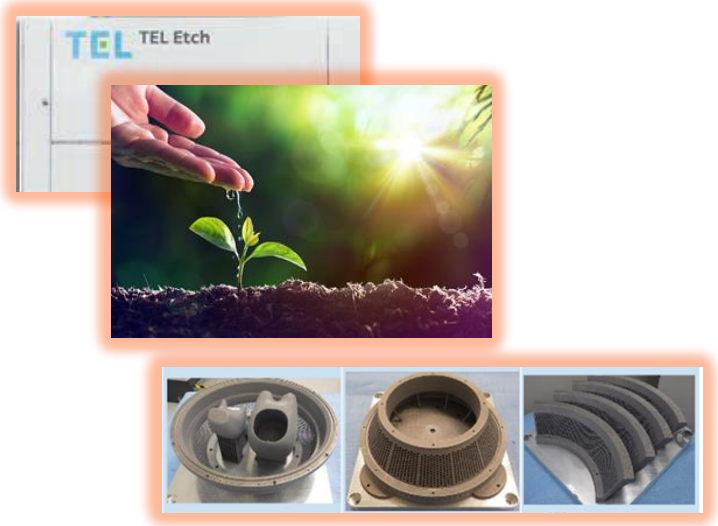
Role of Miyagi Technology Innovation Center

For continuing to provide customers with the finest products and services

FIL
Futuretech Incubation Lab

Create innovative equipment tech

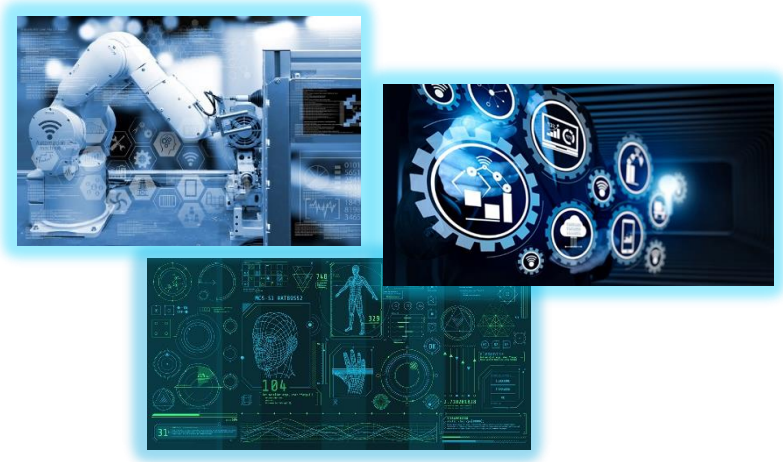
Higher efficiency, lower environmental impact tech, low lead time tech, etc.



PIL
Production Innovatech Lab

Production technology innovation

Next generation production technologies uniting DX and machine assembly



TC
Training Center

Provide world-class training

Raise on-site capabilities for customers and TEL

Promote factory-wide production technology innovation

Summary

- Driven by 3D NAND and patterning, a continued high level of investment in the etch equipment market is expected
- Continue technological innovation for both the memory and logic in response to changes in devices and customer needs
- Work to increase development and production capabilities toward further market growth

TOKYO ELECTRON

TEL's Approach to Next Generation Film Deposition Technology

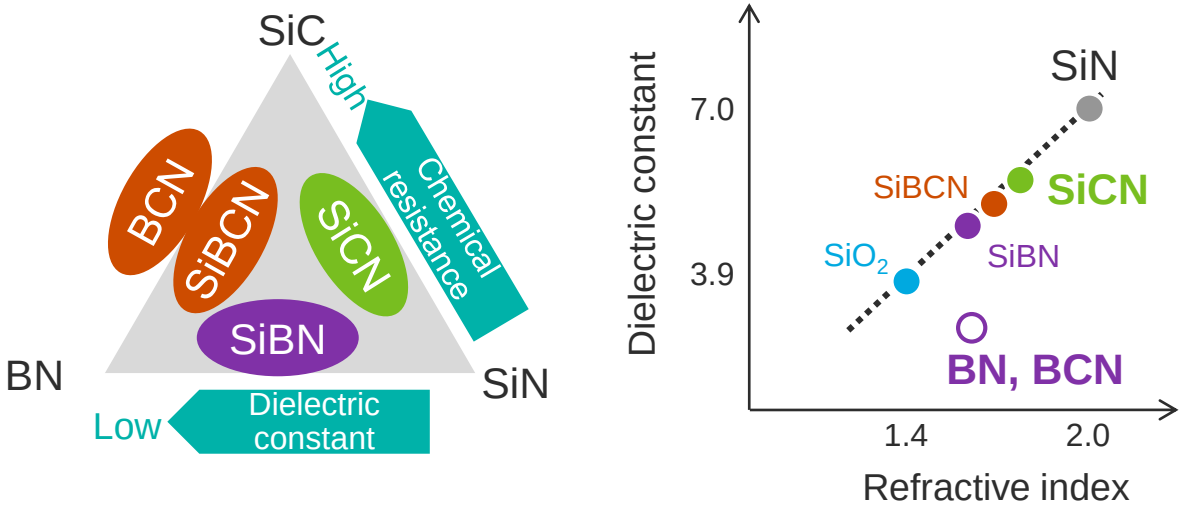
October 12, 2021

Hiroshi Ishida
VP & General Manager, TFF BU

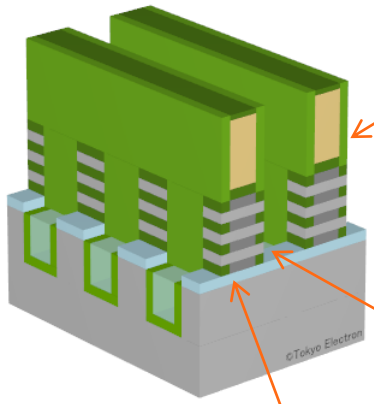
Ultra-thin Film Dielectric Process for Nano Sheet FET

Solution for thin film formation in high aspect ratio narrow spaces

Dielectric characteristics



Ultra-thin film dielectric film deposition for nano sheet



Gate spacer

Insulation between source/drain and gate, control of doping, etc.

Inner spacer

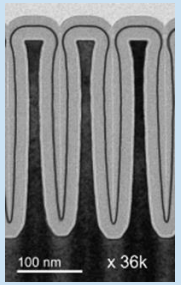
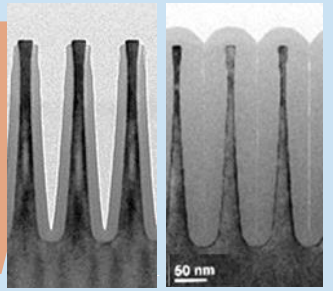
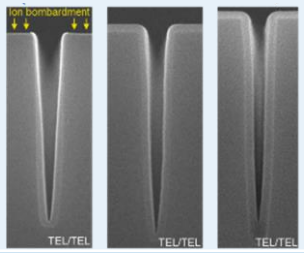
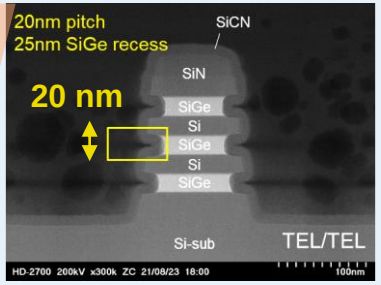
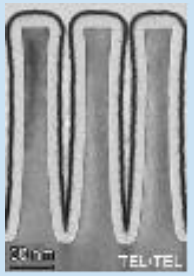
Support sheet with equal interval

Dielectric isolation

Reduce leak currents from Si channel to silicon substrate

Our batch furnaces provide the high quality and ultra-thin dielectric film required in nano sheet formation

Dielectric Film Application Map: Gapfill in Narrow Spaces, Ultra-thin Film Formation

	300 °C	400 °C	500 °C	600 °C
SiN (k ~ 7.5)	Example of dep-etch-dep processes 	Single wafer PECVD (under FS*)	**TELINDY PLUS™ IRad™** Deposition/etch fusion process	
Low-dielectric constant material (k < 4.5)	High H_2 radical Low Example of film formation inhibition technology 	Single wafer PECVD (under FS*)	**TELINDY PLUS™ IRad™** Thickness/film quality/ coverage, integration	
Ultra low-dielectric constant material (k < 3.0)		**TELINDY PLUS™ IRad™** Adoption of new materials (under FS*)		

Expanding product lineup for high quality ultra-thin dielectric film

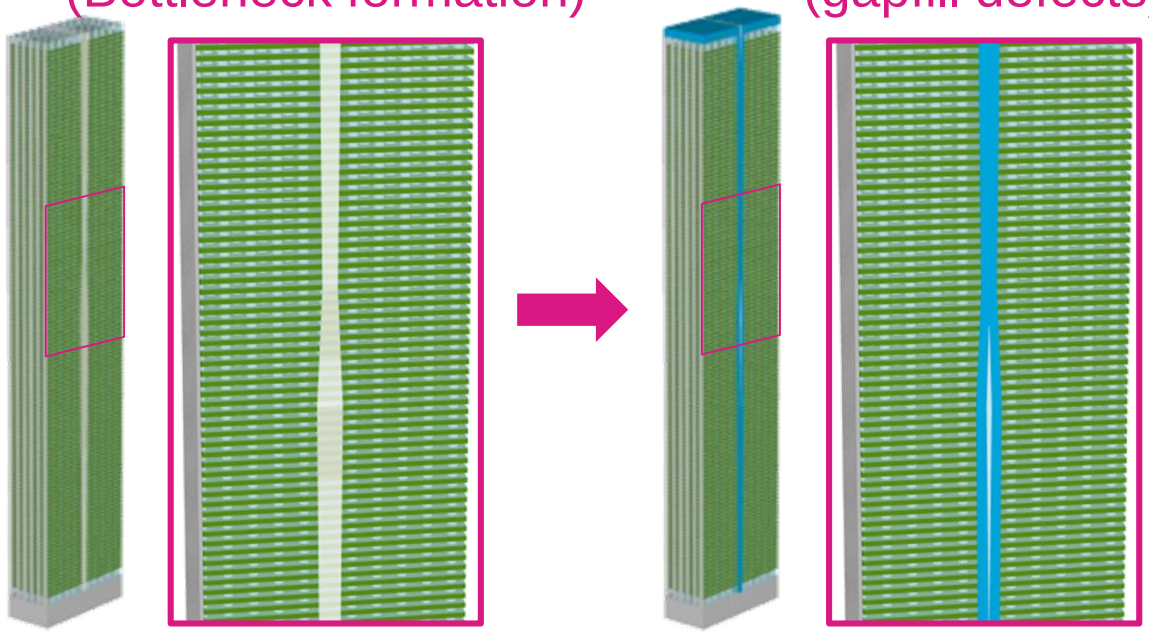
*FS: Feasibility study

Film Formation in Narrow Spaces Utilizing Semi-batch ALD

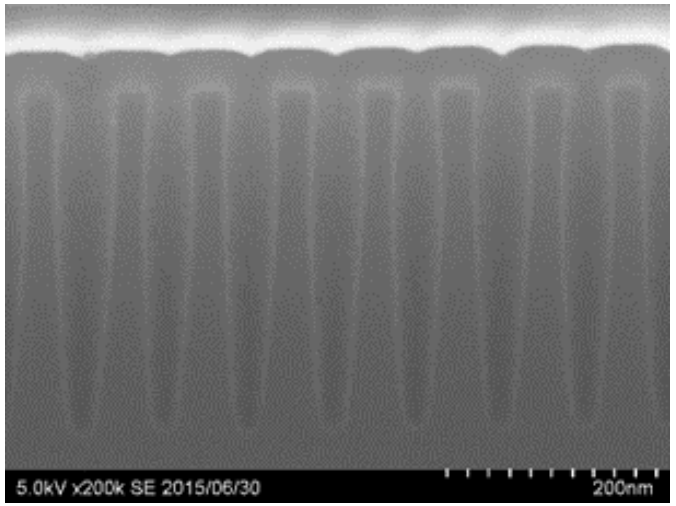
Response to challengers in 3D-NAND multi-layer stacking

Bowing
(Bottleneck formation)

Void
(gapfill defects)



Plasma ALD SiO_2



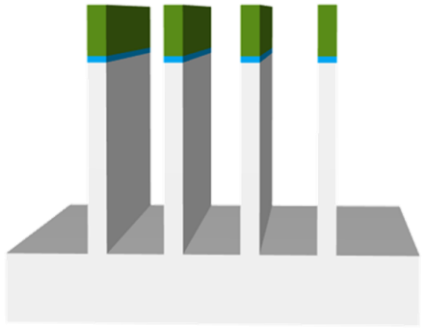
Realize total seamlessness with combination of film formation inhibition and ALD

Semi-batch ALD realizes both high productivity and excellent gapfill performance though multiple continuous processes

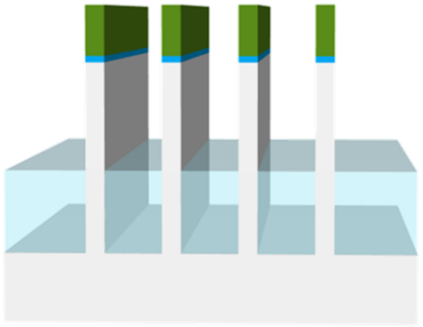
Scaling by Silicon Deposition: New Approach

Cost efficient solution for erosion in fin formation by batch process

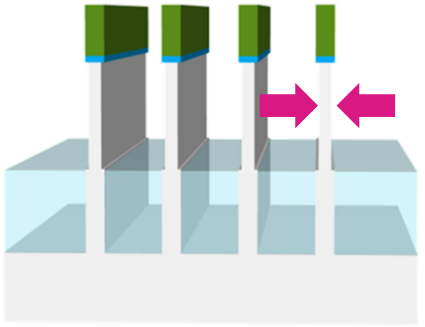
Fin formation



STI formation



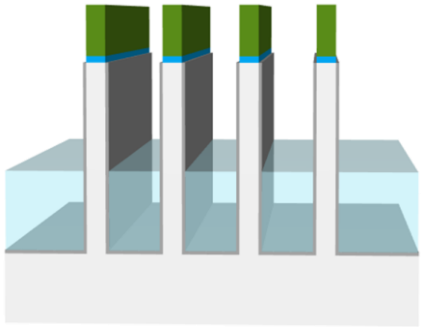
Chemicals cause erosion



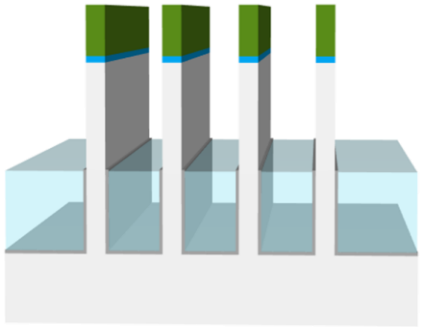
Sacrificial film by Epi

Opportunity for new process to solve fin erosion

STI formation



Realize target pattern

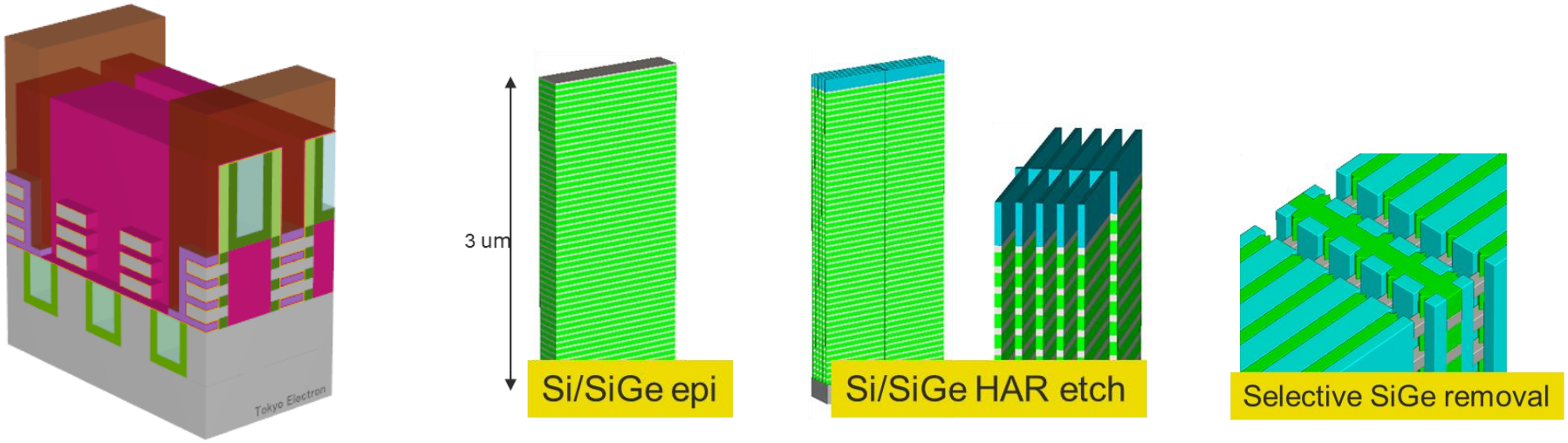


Realize new process by batch deposition through the combination with pre-cleaning

Scaling by Silicon (Si/SiGe) Deposition: Solution for Cost Reduction

Batch deposition to solve the cost challenge of multilayering by epitaxial deposition

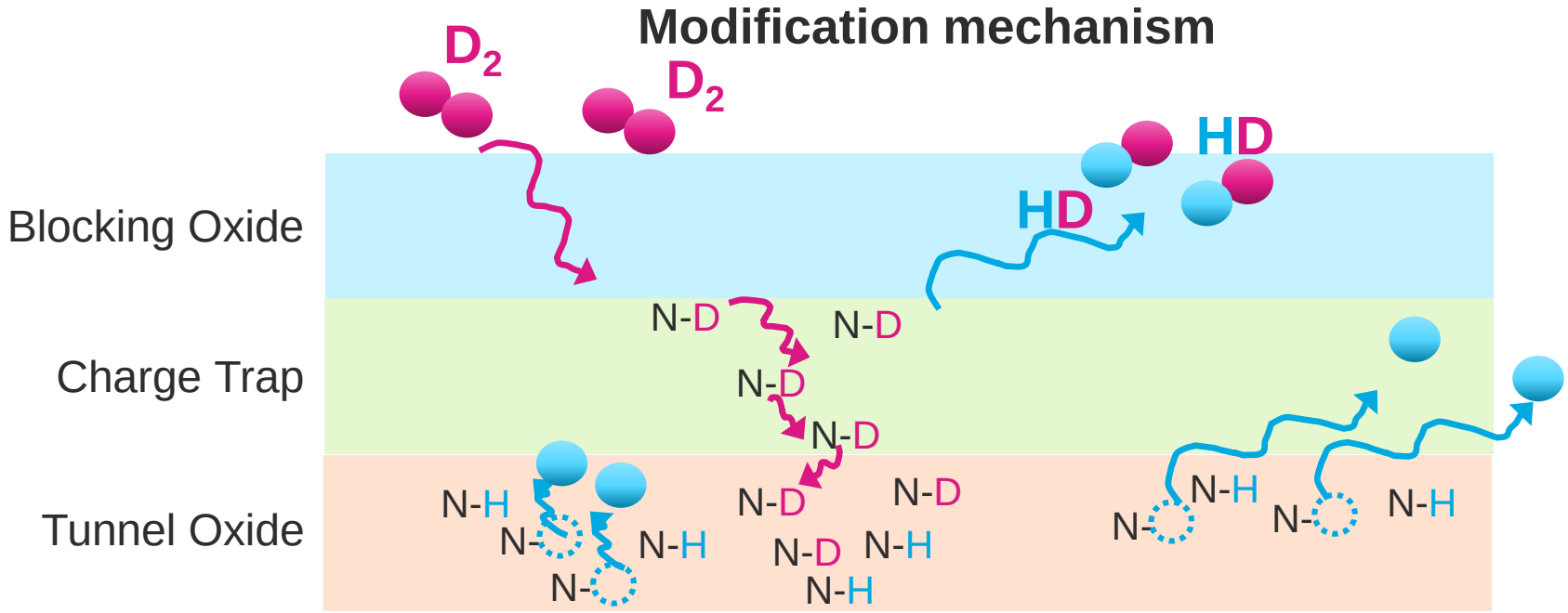
- ✓Logic Nano Sheet: Epi for SiGe/Si multilayering
- ✓Logic Backside PDN: Epi for SiGe for etch stop layer and boron doped Si
- ✓Future DRAM: Epi for SiGe/Si stack



Aiming to expand the application for batch deposition integrated with pre-clean feature

Deuterium Annealing for Enhancing Device Reliability

Improving electrical characteristics and reliability of film in collaboration with customers by utilizing batch furnaces with high productivity



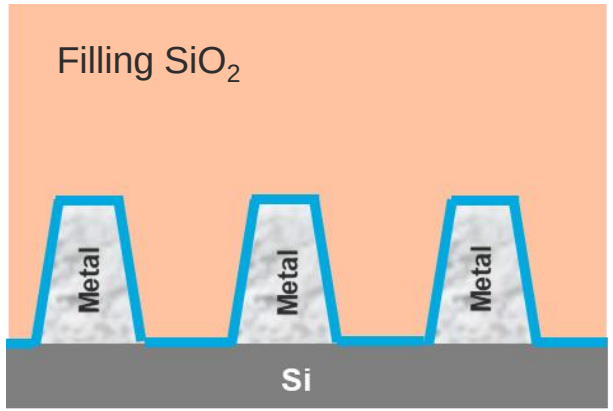
N-H bonding within tunnel oxide film is deteriorated through electric stress caused by write/erase
Improve anti-deterioration by replacing N-H bonding with N-D bonding

Realizing process condition suited to D_2 processes using ultra-large batch

Technology for Surface Modification with Plasma

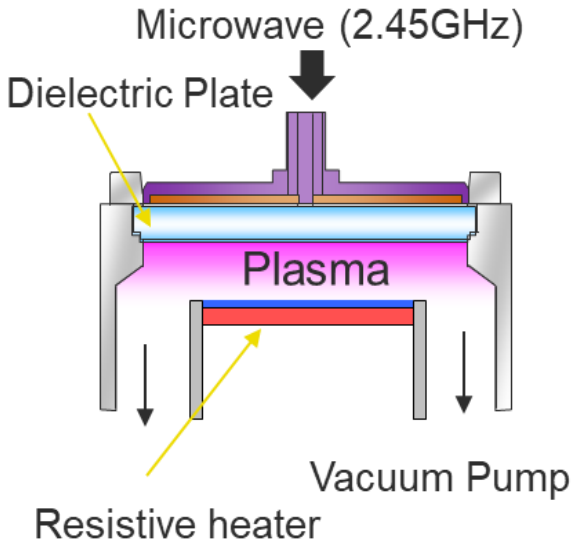
Contribute to process preciseness and device reliability by film modification through low temperature plasma process

Application example

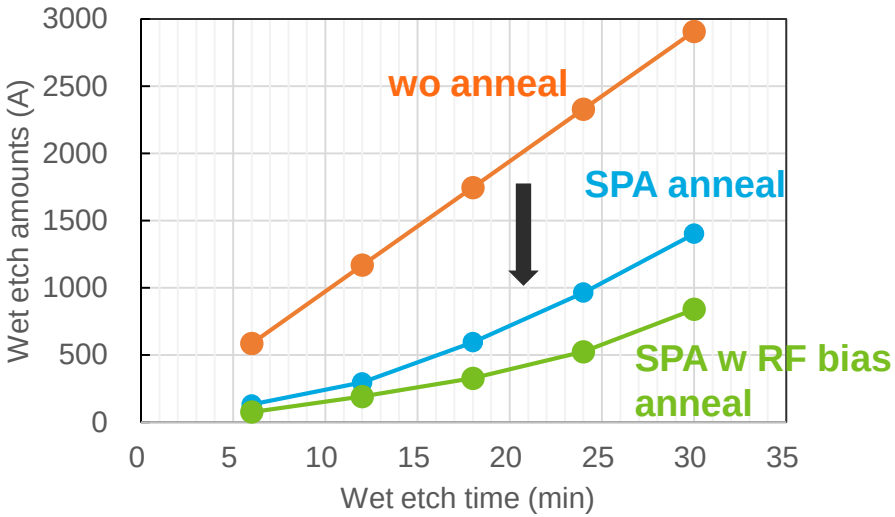


Impurity within the dielectric film formed during the flowable CVD are removed by the thermal oxidization process

Modification from SPA*i*



Chemical resistance



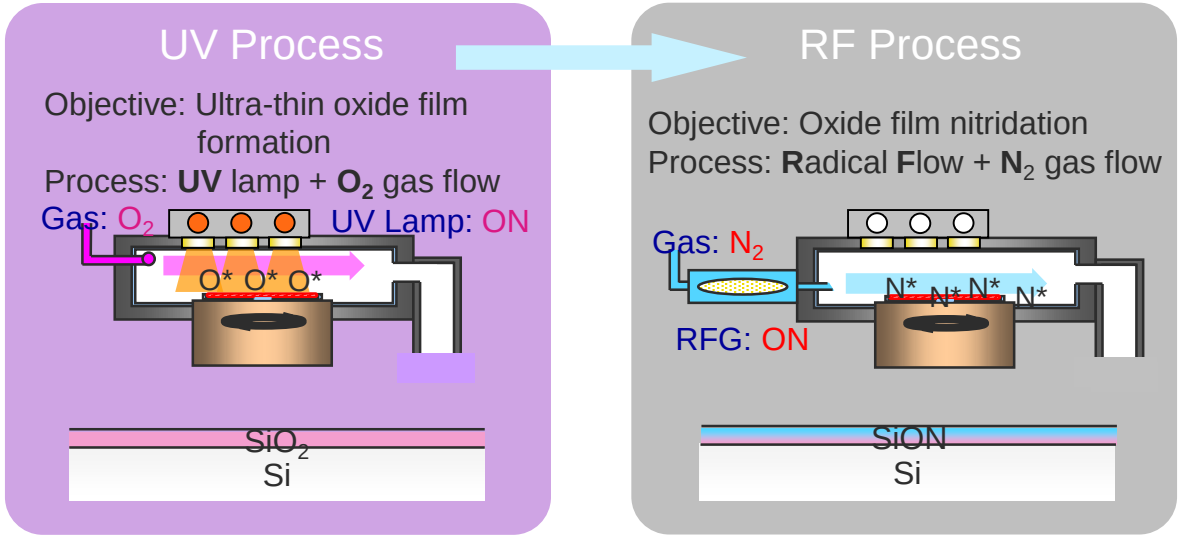
Need low-temperature film modification process for the devices with low temperature resistance

➡ Improve film quality by supplying low electron temperature, high density radicals

Technology for Surface Modification with UV Light

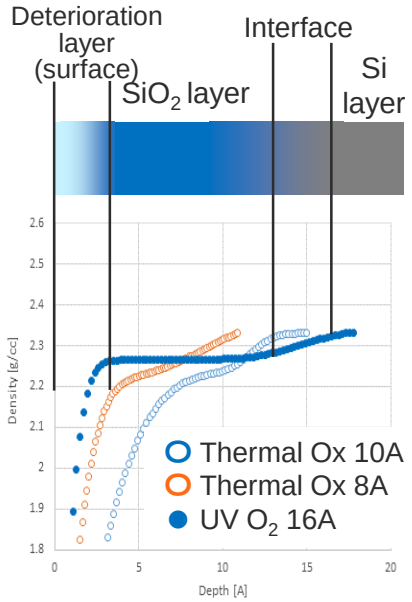
Improve film quality of ultra-thin film by irradiating the surface to be deposited with UV light

UVRF process

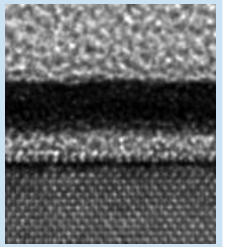
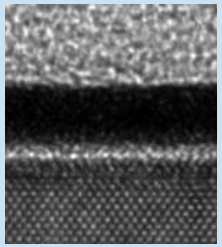


Improved film quality, interface controllability

GIXR measurement



TEM observations

	DHF last	UV O_2
TEM (HfSiO / IL SiO_2 / Si sub.)		
HfSiO thickness	2.3 nm	2.3 nm
IL SiO_2 thickness	0.9 nm	0.6 nm

Expanding application for gate dielectric film etc.,
with its ultra-thin film controllability and high film quality

Hard Mask Module Solutions

Aim to achieve improved LCDU* through collaboration across BUs and products

*LCDU：Local CD Uniformity

Seek optimal solution!

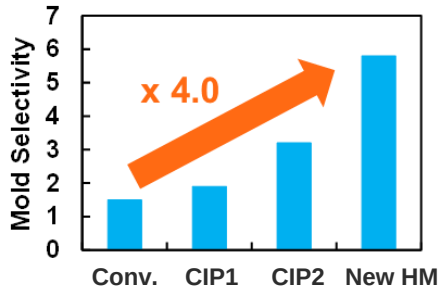
Film quality
Chemical resistance
Adhesion
K value
Material
Composition ratio
Stress
Crystallinity
Temperature

Etching performance
Selectivity
LCDU
Bowing
Bending
Loading
Chemistry
Ion Energy
Temperature
Frequency
Pulse

Removal performance
Selectivity
Damage
Chemical
Temperature
Scheme

Film Property

EXIM™



Mold Etch

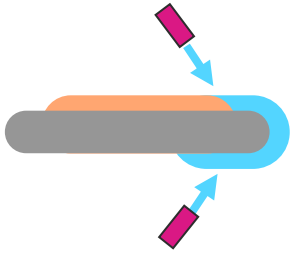
New Hard Mask

Tactras™ Vigus™

1,500 nm-thick

Bevel Strip

Chemical



CELLESTA™-*i*

Summary

- What is being sought from deposition technology in next generation devices is undergoing increasing diversification
- Despite high degree of difficulty, solutions to cost are always being sought
- TEL constantly aims for optimal solutions in both performance and cost from multiple products/technologies
- Combining pre-process, etch and modification treatment with deposition to offer technological solutions
- Expand collaboration across BUs and between products

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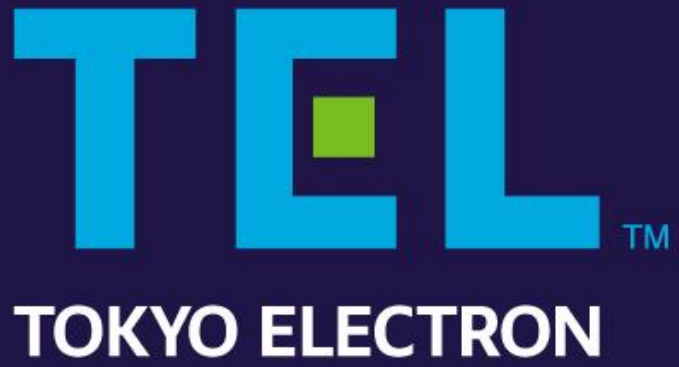
Tokyo Electron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