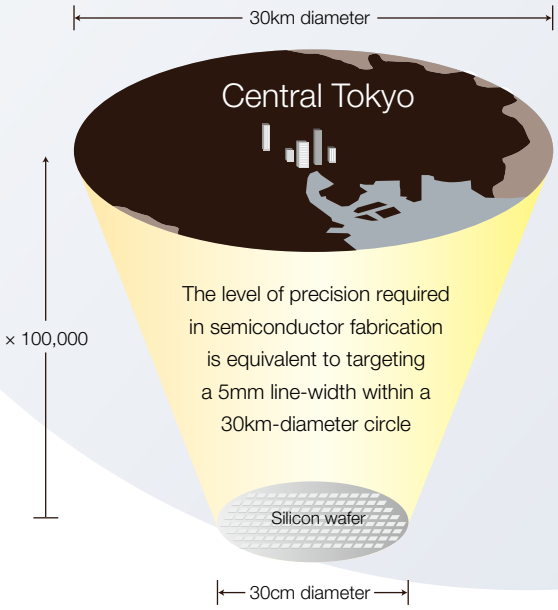
FEATURE

Semiconductor Manufacturing Technology: Bringing Together Science's Best

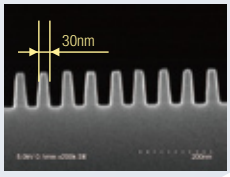
Fabrication of LSI circuits requires precision equivalent to targeting a 5mm line-width within a 30km-diameter circle



LSI circuits of approximately 1cm^2 are formed from disc-shaped silicon wafers 30cm in diameter. The most advanced manufacturing technologies enable fabrication of transistors in an LSI circuit on a scale as small as less than 50 nanometers (nm),*1 allowing several hundred million transistors to be incorporated into one LSI.

In terms of precision, 50nm LSI circuit fabrication on a silicon wafer 30cm in diameter is equivalent to 5mm fabrication on a circle 30km in diameter—an area that would hold the 23 wards of Central Tokyo.

*1 1 nanometer=1 billionth of a meter



Microfabrication

Tokyo Electron develops and supplies semiconductor production

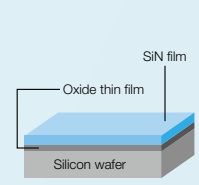
LSI fabrication involves the formation of transistors or interconnects on a silicon wafer through repeated circuit pattern formation processes including lithography, etching, cleaning, deposition, doping, planarization and other processes.

The lithography process involves a series of pattern transcription steps including coating a photoresist (light-sensitive agent) onto a silicon wafer, projecting a mask pattern onto the wafer using a stepper/scanner, exposing the pattern to light, and then developing the exposed pattern. A coater/developer is used in the lithography process to evenly apply the photoresist while spinning the wafer at a high speed and then to develop the pattern.

Following the lithography sequence, the wafer is etched to create circuit elements. Sections of the films not covered by the resist are removed using etching gas in a plasma state in the reaction chamber of an etching system.

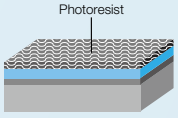
Semiconductor Manufacturing Process Flow

Oxide film formation, Nitride film formation → Patterning*



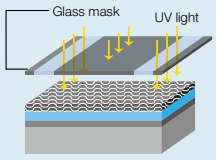
Wafers are placed in a high temperature furnace. O_2 gas is streamed over the wafers to form an SiO_2 film on the surface. Next, an SiN film is formed on top by the CVD method using SiH_4 and NH_3 gases.

Photoresist coating



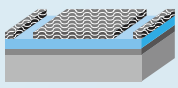
The wafers are then uniformly coated with photoresist via a high-speed spin in a coater. The resist characteristics change when the coating is exposed to ultraviolet (UV) light.

Exposure



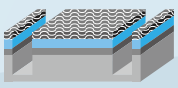
Glass masks with IC patterns are aligned over the wafers. UV light is then applied using a stepper to transfer the patterns to the photoresist.

Development



In a developer module, the wafers are uniformly covered with developing agent. With a positive photoresist, only the portions exposed to UV light dissolve in the developer solution, forming a mask pattern.

Etching



A plasma dry etch system is used to strip the films in accordance with the mask pattern. The portion protected by the photoresist remains intact, thus preserving the original pattern structure under the resist.

* Patterning: The process of forming circuit patterns by means of a photolithography method. Patterning takes place at a number of stages during front-end processing.

Semiconductors, LCD Panels and Photovoltaic Cells— Different Products, Similar Fabrication Technologies

The front-end processing (wafer processing) that takes place in semiconductor manufacturing is highly similar to that performed when manufacturing LCD panels (TFT*1 array processing). Lithography, etching, and thin-film formation and other techniques used in semiconductor production are also used in the manufacturing of LCD panels.

The difference is that while semiconductors are formed on a substrate consisting of a 300mm round silicon wafer, LCD panels are formed on quite large sheets of rectangular glass that can be up to two meters on each side. Moreover, semiconductors, which require high integration, are fabricated on an ultra-precise nanometer*2 scale, while LCD panels are fabricated on a micrometer*3 level.

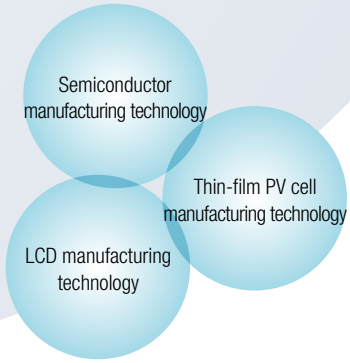
The manufacturing method for these LCD panels is also similar to that for producing thin-film silicon photovoltaic (PV) cells, which are drawing significant attention as a clean energy technology. Processing these PV cells does not require fine patterning, but it is based on a technique in which a thin film of silicon is formed on a glass substrate via a plasma CVD method, which uses almost the same materials.

In semiconductors, technological themes are miniaturization, higher speed, and lower energy consumption. Themes for LCD panels are larger sizes and higher resolution, while high conversion efficiency is the key objective with PV cells. Making these attributes possible in a highly reliable manner is the role of production equipment manufacturers, and these themes will also be the driving force for growth in each respective equipment market.

Going forward, in addition to semiconductor and FPD production equipment, Tokyo Electron will look to PV cell production equipment as another new pillar for growth.

*1 TFT: Thin Film Transistor
*2 1 nanometer=1 billionth of a meter
*3 1 micrometer=1 millionth of a meter

Common production technologies



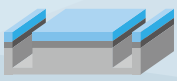
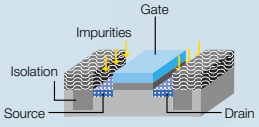
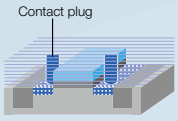
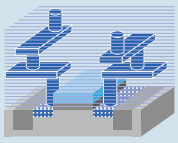
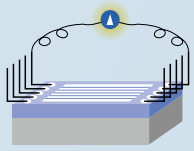
equipment capable of nanoscale microfabrication

Oxidation/diffusion systems or LPCVD (low-pressure chemical vapor deposition) systems, thermal processing systems, are used to form oxide or nitride dielectric films on the wafer.

A cleaning system is used to remove residual materials or particles following the processes of photoresist strip, CVD and others.

Single wafer CVD systems create metal films that form the contacts between the transistors and interconnects using titanium (Ti or TiN) or tungsten (W), for example. CVD is a method of forming layers of thin films on a wafer using heat or plasma energy to cause a chemical reaction with the gas materials used.

Focusing on the wafer fabrication processes, Tokyo Electron supplies a wide range of products that play key roles in manufacturing advanced semiconductors.

	Gate formation, Source/Drain formation	Contact formation	Interconnect formation	Wafer test
Ashing / Cleaning				Probe testing
				
After the etch process, the photoresist is removed by plasma oxidation. The wafers are then dipped in chemical solvents to remove particles and impurities.	A gate dielectric is formed through oxidation, followed by plasma nitridation. A gate electrode is then deposited and patterned to create source/drain regions. The impurities are implanted into these regions, and then uniformly diffused through annealment.	A pre-metal dielectric is deposited by CVD and then planarized. Contact holes are formed using a patterning process and filled with metal film using CVD. Excess metal is removed by polishing.	A low-dielectric-constant film is deposited. Trenches are formed in the film through a patterning process. The trenches are filled with metal film, and the excess metal is polished away. These processes are repeated to create a multi-level interconnect.	Each fabricated wafer contains several hundred identical LSI chips. Prober pins make contact with chips and transmit an electrical signal to test their electrical characteristics.